# 1. Description

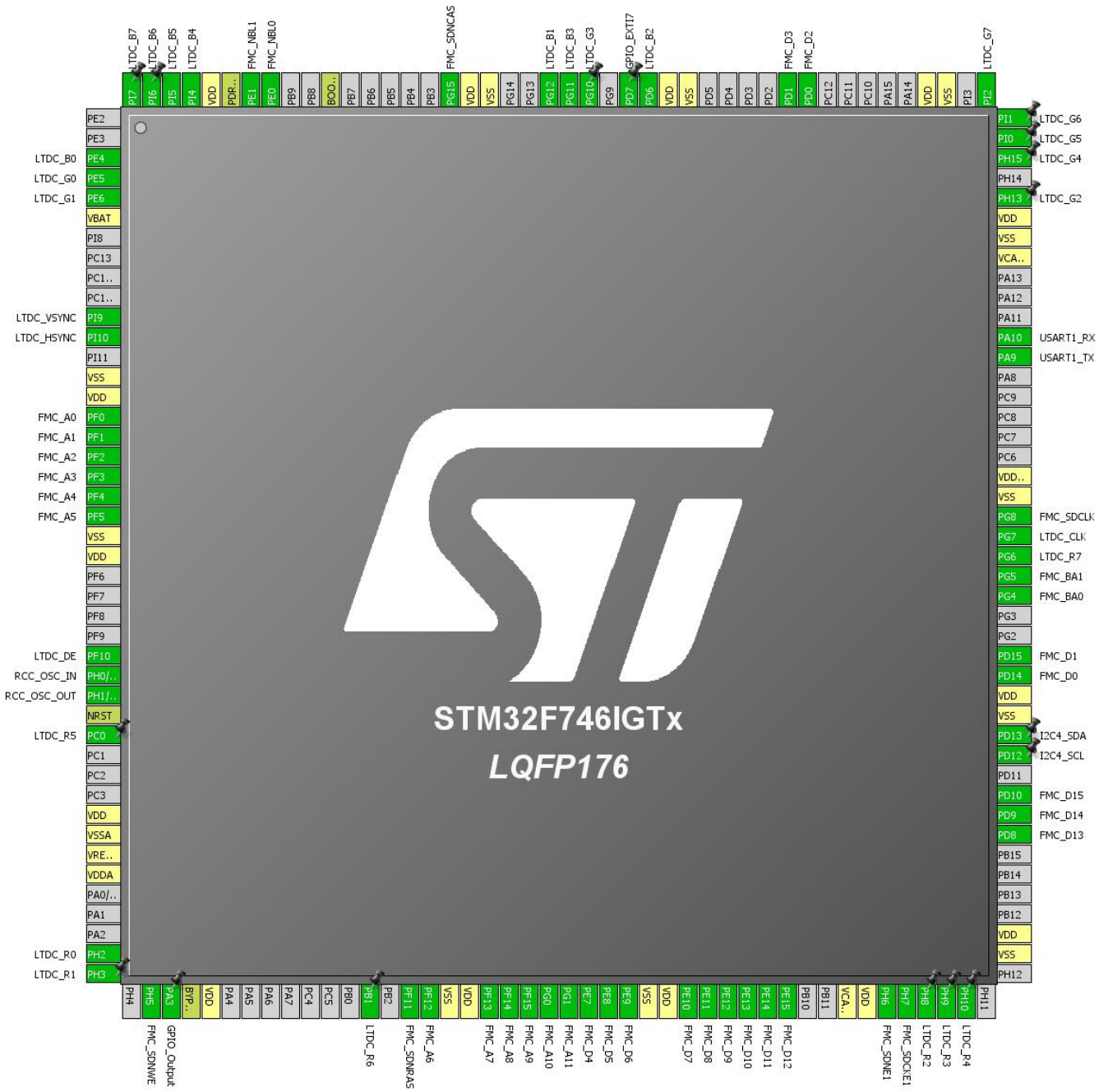
## 1.1. Project

| | |
|---|---|
| Project Name | UART1_746 |
| Board Name | UART1_746 |
| Generated with: | STM32CubeMX 4.12.0 |
| Date | 12/25/2015 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F7 |
| MCU Line | STM32F7x6 |
| MCU name | STM32F746IGTx |
| MCU Package | LQFP176 |
| MCU Pin number | 176 |

# 2. Pinout Configuration



# 3. Pins Configuration

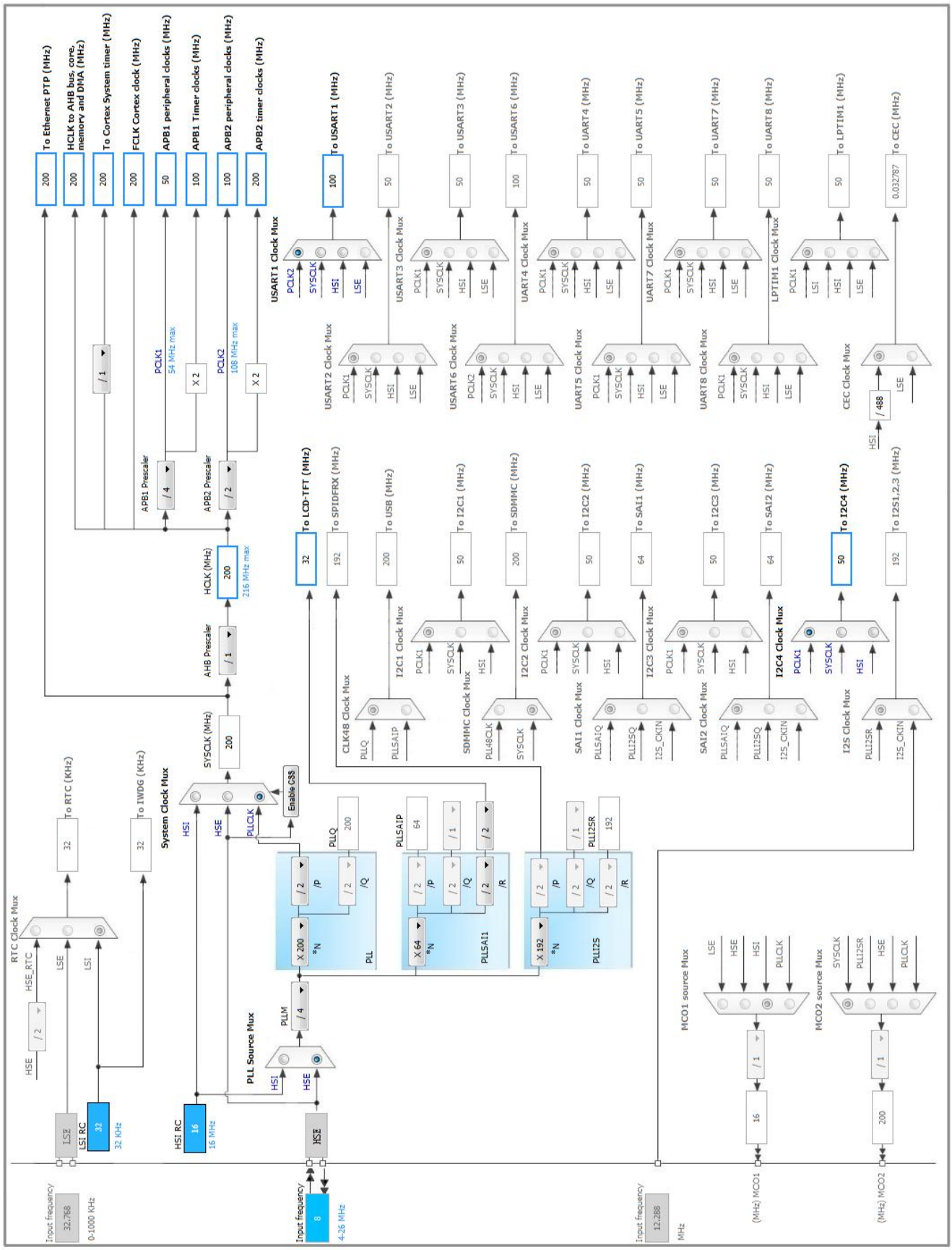
| Pin Number LQFP176 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 3 | PE4 | I/O | LTDC_B0 | |
| 4 | PE5 | I/O | LTDC_G0 | |
| 5 | PE6 | I/O | LTDC_G1 | |
| 6 | VBAT | Power | | |
| 11 | PI9 | I/O | LTDC_VSYNC | |
| 12 | PI10 | I/O | LTDC_HSYNC | |
| 14 | VSS | Power | | |
| 15 | VDD | Power | | |
| 16 | PF0 | I/O | FMC_A0 | |
| 17 | PF1 | I/O | FMC_A1 | |
| 18 | PF2 | I/O | FMC_A2 | |
| 19 | PF3 | I/O | FMC_A3 | |
| 20 | PF4 | I/O | FMC_A4 | |
| 21 | PF5 | I/O | FMC_A5 | |
| 22 | VSS | Power | | |
| 23 | VDD | Power | | |
| 28 | PF10 | I/O | LTDC_DE | |
| 29 | PH0/OSC_IN | I/O | RCC_OSC_IN | |
| 30 | PH1/OSC_OUT | I/O | RCC_OSC_OUT | |
| 31 | NRST | Reset | | |
| 32 | PC0 | I/O | LTDC_R5 | |
| 36 | VDD | Power | | |
| 37 | VSSA | Power | | |
| 38 | VREF+ | Power | | |
| 39 | VDDA | Power | | |
| 43 | PH2 | I/O | LTDC_R0 | |
| 44 | PH3 | I/O | LTDC_R1 | |
| 46 | PH5 | I/O | FMC_SDNWE | |
| 47 | PA3 * | I/O | GPIO_Output | |
| 48 | BYPASS_REG | Reset | | |
| 49 | VDD | Power | | |
| 57 | PB1 | I/O | LTDC_R6 | |
| 59 | PF11 | I/O | FMC_SDNRAS | |
| 60 | PF12 | I/O | FMC_A6 | |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |

| Pin Number LQFP176 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 63 | PF13 | I/O | FMC_A7 | |
| 64 | PF14 | I/O | FMC_A8 | |
| 65 | PF15 | I/O | FMC_A9 | |
| 66 | PG0 | I/O | FMC_A10 | |
| 67 | PG1 | I/O | FMC_A11 | |
| 68 | PE7 | I/O | FMC_D4 | |
| 69 | PE8 | I/O | FMC_D5 | |
| 70 | PE9 | I/O | FMC_D6 | |
| 71 | VSS | Power | | |
| 72 | VDD | Power | | |
| 73 | PE10 | I/O | FMC_D7 | |
| 74 | PE11 | I/O | FMC_D8 | |
| 75 | PE12 | I/O | FMC_D9 | |
| 76 | PE13 | I/O | FMC_D10 | |
| 77 | PE14 | I/O | FMC_D11 | |
| 78 | PE15 | I/O | FMC_D12 | |
| 81 | VCAP_1 | Power | | |
| 82 | VDD | Power | | |
| 83 | PH6 | I/O | FMC_SDNE1 | |
| 84 | PH7 | I/O | FMC_SDCKE1 | |
| 85 | PH8 | I/O | LTDC_R2 | |
| 86 | PH9 | I/O | LTDC_R3 | |
| 87 | PH10 | I/O | LTDC_R4 | |
| 90 | VSS | Power | | |
| 91 | VDD | Power | | |
| 96 | PD8 | I/O | FMC_D13 | |
| 97 | PD9 | I/O | FMC_D14 | |
| 98 | PD10 | I/O | FMC_D15 | |
| 100 | PD12 | I/O | I2C4_SCL | |
| 101 | PD13 | I/O | I2C4_SDA | |
| 102 | VSS | Power | | |
| 103 | VDD | Power | | |
| 104 | PD14 | I/O | FMC_D0 | |
| 105 | PD15 | I/O | FMC_D1 | |
| 108 | PG4 | I/O | FMC_BA0 | |
| 109 | PG5 | I/O | FMC_BA1 | |
| 110 | PG6 | I/O | LTDC_R7 | |
| 111 | PG7 | I/O | LTDC_CLK | |
| 112 | PG8 | I/O | FMC_SDCLK | |

| Pin Number LQFP176 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 113 | VSS | Power | | |
| 114 | VDDUSB | Power | | |
| 120 | PA9 | I/O | USART1_TX | |
| 121 | PA10 | I/O | USART1_RX | |
| 125 | VCAP_2 | Power | | |
| 126 | VSS | Power | | |
| 127 | VDD | Power | | |
| 128 | PH13 | I/O | LTDC_G2 | |
| 130 | PH15 | I/O | LTDC_G4 | |
| 131 | PI0 | I/O | LTDC_G5 | |
| 132 | PI1 | I/O | LTDC_G6 | |
| 133 | PI2 | I/O | LTDC_G7 | |
| 135 | VSS | Power | | |
| 136 | VDD | Power | | |
| 142 | PD0 | I/O | FMC_D2 | |
| 143 | PD1 | I/O | FMC_D3 | |
| 148 | VSS | Power | | |
| 149 | VDD | Power | | |
| 150 | PD6 | I/O | LTDC_B2 | |
| 151 | PD7 | I/O | GPIO_EXTI7 | |
| 153 | PG10 | I/O | LTDC_G3 | |
| 154 | PG11 | I/O | LTDC_B3 | |
| 155 | PG12 | I/O | LTDC_B1 | |
| 158 | VSS | Power | | |
| 159 | VDD | Power | | |
| 160 | PG15 | I/O | FMC_SDNCAS | |
| 166 | BOOT0 | Boot | | |
| 169 | PE0 | I/O | FMC_NBL0 | |
| 170 | PE1 | I/O | FMC_NBL1 | |
| 171 | PDR_ON | Reset | | |
| 172 | VDD | Power | | |
| 173 | PI4 | I/O | LTDC_B4 | |
| 174 | PI5 | I/O | LTDC_B5 | |
| 175 | PI6 | I/O | LTDC_B6 | |
| 176 | PI7 | I/O | LTDC_B7 | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. IPs and Middleware Configuration

## 5.1. DMA2D

**mode: Activated**

### 5.1.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Transfer Mode | Memory to Memory |
| Color Mode | **RGB565 *** |
| Output Offset | 0 |

**Foreground layer Configuration:**

| | |
|---|---|
| DMA2D Input Color Mode | RGB565 |
| DMA2D ALPHA MODE | No modification of the alpha channel value |
| Input Alpha | 0 |
| Input Offset | 0 |

## 5.2. FMC

*SDRAM 1*

**Clock and chip enable: SDCKE1+SDNE1**

**Internal bank number: 4 banks**

**Address: 12 bits**

**Data: 16 bits**

**Byte enable: 16-bit byte enable**

### 5.2.1. SDRAM 1:

**SDRAM control:**

| | |
|---|---|
| Bank | SDRAM bank 2 |
| Column bit number | 8 bits |
| Row bit number | **12 bits *** |
| CAS latency | **3 memory clock cycles *** |
| Write protection | Disabled |
| SDRAM common clock | **2 HCLK clock cycles *** |
| SDRAM common burst read | Disabled |

| | |
|---|---|
| SDRAM common read pipe delay | **1 HCLK clock cycle *** |

**SDRAM timing in memory clock cycles:**

| | |
|---|---|
| Load mode register to active delay | **2 *** |
| Exit self-refresh delay | **7 *** |
| Self refresh time | **4 *** |
| SDRAM common row cycle delay | **6 *** |
| Write recovery time | **2 *** |
| SDRAM common row precharge delay | **2 *** |
| Row to column delay | **2 *** |

## *5.3. I2C4*

**I2C: I2C**

### 5.3.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | **700 *** |
| Fall Time (ns) | **100 *** |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x20F04155 *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## *5.4. LTDC*

**Display Type: RGB888 (24 bits)**

### 5.4.1. Parameter Settings:

### Synchronization for Width:

| | |
|---|---|
| Horizontal Synchronization Width | **20 *** |
| Horizontal Back Porch | **140 *** |
| Active Width | **1024 *** |
| Horizontal Front Porch | **160 *** |
| HSync Width | 19 |
| Accumulated Horizontal Back Porch Width | 159 |
| Accumulated Active Width | 1183 |
| Total Width | 1343 |

### Synchronization for Height:

| | |
|---|---|
| Vertical Synchronization Height | **3 *** |
| Vertical Back Porch | **20 *** |
| Active Height | **600 *** |
| Vertical Front Porch | **12 *** |
| VSync Height | 2 |
| Accumulated Vertical Back Porch Height | 22 |
| Accumulated Active Height | 622 |
| Total Height | 634 |

### Signal Polarity:

| | |
|---|---|
| Horizontal Synchronization Polarity | Active Low |
| Vertical Synchronization Polarity | Active Low |
| Data Enable Polarity | Active Low |
| Pixel Clock Polarity | Normal Input |

### BackGround Color:

| | |
|---|---|
| Red | 0 |
| Green | 0 |
| Blue | 0 |

## 5.4.2. Layer Settings:

### BackGround Color:

| | |
|---|---|
| Layer 0 - Blue | 0 |
| Layer 0 - Green | 0 |
| Layer 0 - Red | 0 |
| Layer 1 - Blue | 0 |
| Layer 1 - Green | 0 |
| Layer 1 - Red | 0 |

### Windows Position:

| | |
|---|---|
| Layer 0 - Window Horizontal Start | 0 |
| Layer 0 - Window Horizontal Stop | **1024 *** |
| Layer 0 - Window Vertical Start | 0 |
| Layer 0 - Window Vertical Stop | **600 *** |
| Layer 1 - Window Horizontal Start | 0 |
| Layer 1 - Window Horizontal Stop | **1024 *** |
| Layer 1 - Window Vertical Start | 0 |
| Layer 1 - Window Vertical Stop | **600 *** |

**Pixel Parameters:**

| | |
|---|---|
| Layer 0 - Pixel Format | **RGB565 *** |
| Layer 1 - Pixel Format | **RGB565 *** |

**Blending:**

| | |
|---|---|
| Layer 0 - Alpha constant for blending | **0xFF *** |
| Layer 0 - Default Alpha value | 0 |
| Layer 0 - Blending Factor1 | **Alpha constant x Pixel Alpha *** |
| Layer 0 - Blending Factor2 | **Alpha constant x Pixel Alpha *** |
| Layer 1 - Alpha constant for blending | 0 |
| Layer 1 - Default Alpha value | 0 |
| Layer 1 - Blending Factor1 | **Alpha constant x Pixel Alpha *** |
| Layer 1 - Blending Factor2 | **Alpha constant x Pixel Alpha *** |

**Frame Buffer:**

| | |
|---|---|
| Layer 0 - Color Frame Buffer Start Adress | **0xD0000000 *** |
| Layer 0 - Color Frame Buffer Line Length (Image Width) | **1024 *** |
| Layer 0 - Color Frame Buffer Number of Lines (Image Height) | **600 *** |
| Layer 1 - Color Frame Buffer Start Adress | **0xD0200000 *** |
| Layer 1 - Color Frame Buffer Line Length (Image Width) | **1024 *** |
| Layer 1 - Color Frame Buffer Number of Lines (Image Height) | **600 *** |

## *5.5. RCC*

### High Speed Clock (HSE): Crystal/Ceramic Resonator

### 5.5.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Flash Latency(WS) | 6 WS (7 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| TIM Prescaler Selection | Disabled |

**Power Parameters:**

| | |
|---|---|
| Power Over Drive | Enabled |
| Power Regulatror Voltage Scale | Power Regulator Voltage Scale 1 |

## *5.6. USART1*

**Mode: Asynchronous**

### 5.6.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | **8 Bits (including Parity) *** |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

# 6. System Configuration

## 6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| FMC | PF0 | FMC_A0 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF1 | FMC_A1 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF2 | FMC_A2 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF3 | FMC_A3 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF4 | FMC_A4 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF5 | FMC_A5 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PH5 | FMC_SDNWE | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF11 | FMC_SDNRAS | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF12 | FMC_A6 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF13 | FMC_A7 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF14 | FMC_A8 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PF15 | FMC_A9 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PG0 | FMC_A10 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PG1 | FMC_A11 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE7 | FMC_D4 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE8 | FMC_D5 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE9 | FMC_D6 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE10 | FMC_D7 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE11 | FMC_D8 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE12 | FMC_D9 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE13 | FMC_D10 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE14 | FMC_D11 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE15 | FMC_D12 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PH6 | FMC_SDNE1 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PH7 | FMC_SDCKE1 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PD8 | FMC_D13 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PD9 | FMC_D14 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PD10 | FMC_D15 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PD14 | FMC_D0 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PD15 | FMC_D1 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PG4 | FMC_BA0 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PG5 | FMC_BA1 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PG8 | FMC_SDCLK | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PD0 | FMC_D2 | Alternate Function Push Pull | No pull-up and no pull-down | High | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PD1 | FMC_D3 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PG15 | FMC_SDNCAS | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE0 | FMC_NBL0 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| | PE1 | FMC_NBL1 | Alternate Function Push Pull | No pull-up and no pull-down | High | |
| I2C4 | PD12 | I2C4_SCL | Alternate Function Open Drain | Pull-up | **High *** | |
| | PD13 | I2C4_SDA | Alternate Function Open Drain | Pull-up | **High *** | |
| LTDC | PE4 | LTDC_B0 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PE5 | LTDC_G0 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PE6 | LTDC_G1 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PI9 | LTDC_VSYNC | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PI10 | LTDC_HSYNC | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PF10 | LTDC_DE | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PC0 | LTDC_R5 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PH2 | LTDC_R0 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PH3 | LTDC_R1 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PB1 | LTDC_R6 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PH8 | LTDC_R2 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PH9 | LTDC_R3 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PH10 | LTDC_R4 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PG6 | LTDC_R7 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PG7 | LTDC_CLK | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PH13 | LTDC_G2 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PH15 | LTDC_G4 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PI0 | LTDC_G5 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PI1 | LTDC_G6 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PI2 | LTDC_G7 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PD6 | LTDC_B2 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PG10 | LTDC_G3 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PG11 | LTDC_B3 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PG12 | LTDC_B1 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PI4 | LTDC_B4 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PI5 | LTDC_B5 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PI6 | LTDC_B6 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PI7 | LTDC_B7 | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| RCC | PH0/OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1/OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| USART1 | PA9 | USART1_TX | Alternate Function Push Pull | Pull-up | **High *** | |
| | PA10 | USART1_RX | Alternate Function Push Pull | Pull-up | **High *** | |
| GPIO | PA3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PD7 | GPIO_EXTI7 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | |

## 6.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| MEMTOMEM | DMA2_Stream0 | Memory To Memory | **High *** |

*MEMTOMEM: DMA2_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | **Enable *** |
| FIFO Threshold: | Full |
| Src Memory Increment: | **Enable *** |
| Dst Memormy Increment: | **Enable *** |
| Src Memory Data Width: | **Word *** |
| Dst Memormy Data Width: | **Word *** |
| Src Memory Burst Size: | Single |
| Dst Memormy Burst Size: | Single |

## 6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| System tick timer | true | 0 | 0 |
| EXTI line[9:5] interrupts | true | 0 | 0 |
| Non maskable interrupt | unused | | |
| Hard fault interrupt | unused | | |
| Memory management fault | unused | | |
| Pre-fetch fault, memory access fault | unused | | |
| Undefined instruction or illegal state | unused | | |
| Debug monitor | unused | | |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| USART1 global interrupt | unused | | |
| FMC global interrupt | unused | | |
| DMA2 stream0 global interrupt | unused | | |
| LTDC global interrupt | unused | | |
| LTDC global error interrupt | unused | | |
| DMA2D global interrupt | unused | | |
| I2C4 event interrupt | unused | | |
| I2C4 error interrupt | unused | | |

*** User modified value**

# 7. Power Plugin report

## 7.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F7 |
| Line | STM32F7x6 |
| MCU | STM32F746IGTx |
| Datasheet | 027590_Rev1 |

## 7.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

# 8. Software Project

## 8.1. Project Settings

| Name | Value |
|---|---|
| Project Name | UART1_746 |
| Project Folder | C:\task\05 cube\UART1_746 +printf + sdram |
| Toolchain / IDE | MDK-ARM V5 |
| Firmware Package Name and Version | STM32Cube FW_F7 V1.3.1 |

## 8.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube Firmware Library Package | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |