

RM500Q-AE&RM502Q-AE

Hardware Design

5G Module Series

Version: 1.0

Date: 2021-03-06

Status: Released



Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

Quectel Wireless Solutions Co., Ltd.

Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China

Tel: +86 21 5108 6236

Email: info@quectel.com

Or our local office. For more information, please visit:

<http://www.quectel.com/support/sales.htm>.

For technical support, or to report documentation errors, please visit:

<http://www.quectel.com/support/technical.htm>

Or email to support@quectel.com.

General Notes

Quectel offers the information as a service to its customers. The information provided is based upon customers' requirements. Quectel makes every effort to ensure the quality of the information it makes available. Quectel does not make any warranty as to the information contained herein, and does not accept any liability for any injury, loss or damage of any kind incurred by use of or reliance upon the information. All information supplied herein is subject to change without prior notice.

Disclaimer

While Quectel has made efforts to ensure that the functions and features under development are free from errors, it is possible that these functions and features could contain errors, inaccuracies and omissions. Unless otherwise provided by valid agreement, Quectel makes no warranties of any kind, implied or express, with respect to the use of features and functions under development. To the maximum extent permitted by law, Quectel excludes all liability for any loss or damage suffered in connection with the use of the functions and features under development, regardless of whether such loss or damage may have been foreseeable.

Duty of Confidentiality

The Receiving Party shall keep confidential all documentation and information provided by Quectel, except when the specific permission has been granted by Quectel. The Receiving Party shall not access or use Quectel's documentation and information for any purpose except as expressly provided herein. Furthermore, the Receiving Party shall not disclose any of the Quectel's documentation and information to any third party without the prior written consent by Quectel. For any noncompliance to the above requirements, unauthorized use, or other illegal or malicious use of the documentation and information, Quectel will reserve the right to take legal action.

Copyright

The information contained here is proprietary technical information of Quectel. Transmitting, reproducing, disseminating, and editing this document as well as using the content without permission are forbidden. Offenders will be held liable for payment of damages. All rights are reserved in the event of a patent grant or registration of a utility model or design.

Copyright © Quectel Wireless Solutions Co., Ltd. 2021. All rights reserved.

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.



In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as mobile phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2020-10-22	Jared WANG /Hank LIU	Creation of the document
1.0	2021-03-06	Jared WANG/ Hogan SHENG/ /Hank LIU	First official release

Contents

Safety Information	3
About the Document	4
Contents	5
Table Index	8
Figure Index	10
1 Introduction	12
1.1. Introduction.....	12
1.2. Reference Standard.....	12
1.3. Special Mark.....	13
2 Product Concept	14
2.1. General Description.....	14
2.2. Key Features.....	15
2.3. Evaluation Board.....	18
2.4. Functional Diagram.....	18
2.5. Pin Assignment.....	19
2.6. Pin Description.....	20
3 Operating Characteristics	25
3.1. Operating Modes.....	25
3.1.1. Sleep Mode.....	25
3.1.2. Airplane Mode.....	27
3.2. Communication Interface with a Host.....	27
3.3. Power Supply.....	28
3.3.1. Decrease Voltage Drop.....	28
3.3.2. Reference Design for Power Supply.....	29
3.3.3. Monitor the Power Supply.....	30
3.4. Turn on.....	30
3.5. Turn off.....	32
3.5.1. Turn off the Module through FCPO#.....	32
3.5.2. Turn off the Module through AT Command.....	33
3.6. Reset.....	34
4 Application Interfaces	36
4.1. (U)SIM Interface.....	36
4.1.1. Pin definition of (U)SIM.....	36
4.1.2. (U)SIM Hot-plug.....	37
4.1.3. Normally Closed (U)SIM Card Connector.....	38
4.1.4. Normally Open (U)SIM Card Connector.....	38
4.1.5. (U)SIM Card Connector Without Hot-plug.....	39
4.1.6. (U)SIM Design Notices.....	40
4.2. USB Interface.....	40

4.3.	PCIe Interface	42
4.3.1.	PCIe Operating Mode	42
4.3.2.	Pin Definition of PCIe	43
4.3.3.	Reference Design for PCIe	44
4.3.4.	PCIe Timing.....	45
4.4.	PCM Interface	46
4.5.	Control and Indication Interfaces	48
4.5.1.	W_DISABLE1#.....	48
4.5.2.	W_DISABLE2#.....	49
4.5.3.	WWAN_LED#.....	50
4.5.4.	WAKE_ON_WAN#.....	51
4.5.5.	DPR*	52
4.5.6.	STATUS*.....	52
4.6.	Cellular/WLAN COEX Interface*	52
4.7.	Antenna Tuner Control Interface*	53
4.8.	Configuration Pins.....	53
5	RF Characteristics	55
5.1.	Cellular Antenna Interfaces.....	55
5.1.1.	Pin Definition	55
5.1.2.	Port Mapping	56
5.1.3.	Operating Frequency	56
5.1.4.	Receiving Sensitivity	58
5.1.5.	Output Power	61
5.2.	GNSS Antenna Interface	61
5.2.1.	General Description	61
5.2.2.	GNSS Frequency	62
5.2.3.	GNSS Performance	62
5.3.	Antenna Connectors	63
5.3.1.	Antenna Connector Location	63
5.3.2.	Antenna Connector Size	64
5.3.3.	Antenna Connector Installation.....	65
5.3.4.	Recommended RF Connector Installation.....	67
5.3.4.1.	Assemble Coaxial Cable Plug Manually	67
5.3.4.2.	Assemble Coaxial Cable Plug with Jig	68
5.3.5.	Recommended Manufacturers of RF Connector and Cable	69
5.4.	Antenna Requirements	69
6	Electrical Characteristics and Reliability	70
6.1.	Power Supply Requirements	70
6.2.	Current Consumption.....	70
6.3.	Digital I/O Characteristic	75
6.4.	Electrostatic Discharge	76
6.5.	Thermal Dissipation	77
6.6.	Absolute Maximum Ratings	78

6.7.	Operating and Storage Temperatures	79
7	Mechanical Dimensions and Packaging	80
7.1.	Mechanical Dimensions of the Module	80
7.2.	Top and Bottom Views of the Module.....	81
7.3.	M.2 Connector.....	82
7.4.	Packaging	82
8	Appendix References	84

Table Index

Table 1: Special Mark.....	13
Table 2: Frequency Bands and GNSS Type of RM500Q-AE&RM502Q-AE Module.....	14
Table 3: Key Features of RM500Q-AE&RM502Q-AE	15
Table 4: Definition of I/O Parameters.....	20
Table 5: Pin Description	20
Table 6: Overview of Operating Modes	25
Table 7: Definition of VCC and GND Pins	28
Table 8: Definition of FCPO#	30
Table 9: Trun-on Timing of the Module.....	31
Table 10: Turn-off Timing of the Module through FCPO#	32
Table 11: Turn-off Timing of the Module through AT Command and FCPO#.....	33
Table 12: Definition of RESET# Pin.....	34
Table 13: Reset Timing of the Module	35
Table 14: Pin Definition of (U)SIM Interface	36
Table 15: Pin Definition of USB Interface	40
Table 16: Pin Definition of PCIe Interface.....	43
Table 17: PCIe Power-up Timing of M.2 Specification	45
Table 18: PCIe Turn-on Timing of the Module.....	46
Table 19: Pin Definition of PCM Interface.....	47
Table 20: Pin Definition of Control and Indication Interfaces.....	48
Table 21: RF Function Status	49
Table 22: GNSS Function Status	49
Table 23: Network Status Indications of WWAN_LED#	51
Table 24: State of the WAKE_ON_WAN#	51
Table 25: Function of the DPR Signal.....	52
Table 26: Pin Definition of COEX Interface	52
Table 27: Pin Definition of Antenna Tuner Control Interface	53
Table 28: Configuration Pins List of M.2 Specification	53
Table 29: Configuration Pins of the Module.....	54
Table 30: RM500Q-AE&RM502Q-AE Pin Definition of Antenna Interfaces.....	55
Table 31: RM500Q-AE & RM502Q-AE Antenna Mapping	56
Table 32: RM500Q-AE&RM502Q-AE Operating Frequencies.....	56
Table 33: RM500Q-AE&RM502Q-AE Conducted Receiving Sensitivity (Unit: dBm)	58
Table 34: Cellular Output Power	61
Table 35: GNSS Frequency	62
Table 36: GNSS Performance	62
Table 37: Major Specifications of the RF Connector	65
Table 38: Antenna Requirements	69
Table 39: Power Supply Requirements	70
Table 40: RM500Q-AE&RM502Q-AE Current Consumption	70
Table 41: Logic Levels of Digital I/O (1.8 V)	75

Table 42: (U)SIM 1.8V I/O Requirements	76
Table 43: (U)SIM 3.0V I/O Requirements	76
Table 44: Electrostatic Discharge Characteristics (Temperature: 25 °C, Humidity: 40 %)	76
Table 45: Absolute Maximum Ratings	78
Table 46: Operating and Storage Temperatures	79
Table 47: Related Documents.....	84
Table 48: Terms and Abbreviations	84

Figure Index

Figure 1: Functional Diagram.....	18
Figure 2: Pin Assignment.....	19
Figure 3: DRX Run Time and Current Consumption in Sleep Mode.....	26
Figure 4: Sleep Mode Application with USB Remote Wakeup.....	26
Figure 5: Power Supply Limits during Radio Transmission.....	28
Figure 6: Reference Circuit for VCC.....	29
Figure 7: Reference Circuit for Power Supply.....	29
Figure 8: Turn on the Module with a Host GPIO.....	31
Figure 9: Turn-on Timing of the Module.....	31
Figure 10: Turn-off Timing through FCPO#.....	32
Figure 11: Turn-off Timing through AT Command and FCPO#.....	33
Figure 12: Reference Circuit of RESET# with NPN Driver Circuit.....	34
Figure 13: Reference Circuit of RESET# with a Button.....	35
Figure 14: Reset Timing of the Module.....	35
Figure 15: Reference Circuit for Normally Closed (U)SIM Card Connector.....	38
Figure 16: Reference Circuit for Normally Open (U)SIM Card Connector.....	39
Figure 17: Reference Circuit for a 6-Pin (U)SIM Card Connector.....	39
Figure 18: Reference Circuit of USB 3.1 & 2.0 Interface.....	41
Figure 19: PCIe Interface Reference Circuit.....	44
Figure 20: PCIe Power-up Timing of M.2 Specification.....	45
Figure 21: PCIe Power-up Timing of the Module.....	45
Figure 22: Primary Mode Timing.....	47
Figure 23: Auxiliary Mode Timing.....	47
Figure 24: W_DISABLE1# and W_DISABLE2# Reference Circuit.....	50
Figure 25: WWAN_LED# Reference Circuit.....	50
Figure 26: WAKE_ON_WAN# Signal Reference Circuit.....	51
Figure 27: Recommended Circuit of Configuration Pins.....	54
Figure 28: RM500Q-AE Antenna Connectors.....	63
Figure 29: RM502Q-AE Antenna Connectors.....	64
Figure 30: RF Connector Dimensions (Unit: mm).....	64
Figure 31: Specifications of Mating Plugs Using Ø 0.81 mm Coaxial Cables.....	65
Figure 32: Connection Between RF Connector and Mating Plug Using Ø 0.81 mm Coaxial Cable.....	66
Figure 33: Connection Between RF Connector and Mating Plug Using Ø 1.13 mm Coaxial Cable.....	66
Figure 34: Plug in a Coaxial Cable Plug.....	67
Figure 35: Pull out a Coaxial Cable Plug.....	68
Figure 36: Install the Coaxial Cable Plug with A Jig.....	68
Figure 37: Thermal Dissipation Area Inside and on Bottom Side of the Module.....	77
Figure 38: Mechanical Dimensions of the Module (Unit: mm).....	80
Figure 39: RM500Q-AE Top View and Bottom View.....	81
Figure 40: RM502Q-AE Top View and Bottom View.....	81
Figure 41: Tray Size (Unit: mm).....	82

Figure 42: Tray Packaging Procedure 83

1 Introduction

1.1. Introduction

The hardware design defines RM500Q-AE and RM502Q-AE and describes the air and hardware interfaces which are connected to customers' applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of RM500Q-AE and RM502Q-AE. To facilitate its application in different fields, reference design is also provided for reference. Associated with application notes and user guides, customers can use the module to design and set up mobile applications easily.

This document is applicable to RM500Q-AE and RM502Q-AE modules.

1.2. Reference Standard

The module complies with the following standards:

- *PCI Express M.2 Specification Revision 3.0, Version 1.2*
- *PCI Express Base Specification Revision 3.0*
- *Universal Serial Bus Specification, Revision 3.1*
- *ISO/IEC 7816-3*
- *MIPI Alliance Specification for RF Front-End Control Interface version 2.0*
- *3GPP TS 27.007 and 3GPP TS 27.005*

1.3. Special Mark

Table 1: Special Mark

Mark	Definition
*	When an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin name, AT command, or argument is under development and currently not supported, unless otherwise specified.
[...]	Brackets ([...]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, ANTCTL[1:2] refers to both two ANTCTL pins, ANTCTL1 and ANTCTL2.

2 Product Concept

2.1. General Description

RM500Q-AE and RM502Q-AE are 5G NR/LTE-FDD/LTE-TDD/WCDMA wireless communication modules with receive diversity. They provide data connectivity on 5G NR SA and NSA, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA networks. They are standard M.2 Key-B WWAN modules. For more details, see *PCI Express M.2 Specification Revision 3.0, Version 1.2*

RM500Q-AE and RM502Q-AE are industrial-grade modules for industrial and commercial applications only.

They support embedded operating systems such as Windows, Linux and Android, and also provide GNSS and voice* functionality to meet specific application demands.

The following table shows the frequency bands and GNSS type of the module.

Table 2: Frequency Bands and GNSS Type of RM500Q-AE&RM502Q-AE Module

Mode	RM500Q-AE&RM502Q-AE
5G NR SA	n1/n2/n3/n5/n7/n8/n12/n20/n25/n28/n38/n40/n41/n48*/n66/n71/n77/n78/n79
5G NR NSA	n1/n2/n3/n5/n7/n8/n12/n20/n25/n28/n38/n40/n41/n48*/n66/n71/n77/n78/n79
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12(B17)/B13/B14/B18/B19/B20/B25/B26/B28/B29/B30/B32/B66/B71
LTE-TDD	B34/B38/B39/B40/B41/B42/B43/B48
LAA	B46
WCDMA	B1/B2/B3/B4/B5/B6/B8/B19
GNSS	GPS/GLONASS/QZSS/BeiDou (COMPASS)/Galileo

The module can be applied to the following fields:

- Rugged tablet PC and laptop computer
- Remote monitor system
- Smart metering system
- Wireless CPE
- Smart TV
- Outdoor live devices
- Wireless router and switch
- Other wireless terminal devices

2.2. Key Features

The following table describes key features of RM500Q-AE and RM502Q-AE.

Table 3: Key Features of RM500Q-AE&RM502Q-AE

Feature	Details
Function Interface	PCI Express M.2 Interface
Power Supply	<ul style="list-style-type: none"> ● Supply voltage: 3.135–4.4 V ● Typical supply voltage: 3.7 V
(U)SIM Interface	<ul style="list-style-type: none"> ● Compliant with <i>ISO/IEC 7816-3</i> ● Supported (U)SIM card: Class B (3.0 V) and Class C (1.8 V) ● Single (U)SIM Slot
USB Interface	<ul style="list-style-type: none"> ● Compliant with USB 3.1 and 2.0 specifications, with maximum transmission rates up to 10 Gbps on USB 3.1 and 480 Mbps on USB 2.0. ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output and voice* over USB. ● Supported USB serial drivers: Windows 7/8/8.1/10, Linux 2.6–5.4, Android 4.x/5.x/6.x/7.x/8.x/9.x/10
PCIe Interface	<ul style="list-style-type: none"> ● Complaint with PCIe Gen 3, ● PCIe x 1, supporting 8 Gbps per lane. ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output
PCM Interface	<ul style="list-style-type: none"> ● Used for audio function with external codec ● Supports 16-bit linear data format ● Supports long and short frame synchronization ● Supports master and slave modes, but must be the master in long frame synchronization

Transmitting Power	<ul style="list-style-type: none"> ● 5G NR bands: Class 3 (23 dBm ±2 dB) ● 5G NR n41/n77/n78/n79 bands HPUE: Class 2 (26 dBm +2/-3 dB) ● LTE bands: Class 3 (23 dBm ±2 dB) ● LTE B38/B40/B41/B42/B43 bands HPUE ¹⁾: Class 2 (26 dBm ±2 dB) ● WCDMA bands: Class 3 (24 dBm +1/-3 dB)
5G NR Features	<ul style="list-style-type: none"> ● Supports 3GPP Rel-15 ● Supported Modulations: <ul style="list-style-type: none"> - Uplink: $\pi/2$-BPSK, QPSK, 16QAM, 64QAM and 256QAM - Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supported MIMO: <ul style="list-style-type: none"> - Uplink: 2 × 2 MIMO ²⁾ on n41 - Downlink: 4 × 4 MIMO on n1/n2/n3/n7/25/n38/n40/n41/n48*/n66/n77/n78/n79 ● Supports SCS 15 kHz ³⁾ and 30 kHz ³⁾ ● Supports SA ⁴⁾ and NSA ⁴⁾ operation modes on all the 5G band ● Supports Option 3x, 3a, 3 and Option 2 ● Max. transmission data rates ⁵⁾: <p>RM500Q-AE NSA: 2.5 Gbps (DL)/ 650 Mbps (UL) SA: 2.1 Gbps (DL)/ 450 Mbps (UL)</p> <p>RM502Q-AE NSA: 5 Gbps (DL)/ 650 Mbps (UL) SA: 4.2 Gbps (DL)/ 450 Mbps (UL)</p>
LTE Features	<ul style="list-style-type: none"> ● Supports 3GPP Rel-15 ● LTE Category: <p>RM500Q-AE: DL Cat 16/ UL Cat 18 RM502Q-AE: DL Cat 20/ UL Cat 18</p> ● Supported modulations: <ul style="list-style-type: none"> - Uplink: QPSK, 16QAM and 64QAM and 256QAM* - Downlink: QPSK, 16QAM and 64QAM and 256QAM ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports downlink 4 × 4 MIMO on: B1/B2/B3/B4/B7/B25/B30/B38/B39/B40/B41/B42/B43/B48/B66 ● Max. transmission data rates ⁵⁾: <p>RM500Q-AE LTE: 1.0 Gbps (DL)/ 200 Mbps (UL)</p> <p>RM502Q-AE LTE: 2.0 Gbps (DL)/ 200 Mbps (UL)</p>
UMTS Features	<ul style="list-style-type: none"> ● Supports 3GPP Rel-9 DC-HSDPA, HSPA +, HSDPA, HSUPA and WCDMA ● Supports QPSK, 16QAM and 64QAM modulation ● Max. transmission data rates ⁵⁾: <ul style="list-style-type: none"> - DC-HSDPA: 42 Mbps (DL) - HSUPA: 5.76 Mbps (UL) - WCDMA: 384 kbps (DL)/ 384 kbps (UL)

Rx-diversity	<ul style="list-style-type: none"> ● Supports 5G NR/LTE/WCDMA Rx-diversity
GNSS Features	<ul style="list-style-type: none"> ● Protocol: NMEA 0183 ● Data Update Rate: 1 Hz
Antenna Interfaces	<ul style="list-style-type: none"> ● ANT0, ANT1, ANT2, and ANT3_GNSS1
AT Commands	<ul style="list-style-type: none"> ● Compliant with 3GPP TS 27.007 and 3GPP TS 27.005 ● Quectel enhanced AT commands
Internet Protocol Features	<ul style="list-style-type: none"> ● Supports QMI/NTP* protocols ● Supports the protocols PAP and CHAP usually used for PPP connections
Firmware Upgrade	<ul style="list-style-type: none"> ● USB 2.0 interface ● PCIe interface ● DFOTA
SMS	<ul style="list-style-type: none"> ● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
Physical Characteristics	<ul style="list-style-type: none"> ● M.2 Key-B ● Size: (30.0 ±0.15) mm × (52.0 ±0.15) mm × (2.3 ±0.2) mm ● Weight: approx. 8.7 g
Temperature Range	<ul style="list-style-type: none"> ● Operating temperature range: -30 °C to +70 °C ⁶⁾ ● Extended temperature range: -40 °C to +85 °C ⁷⁾ ● Storage temperature range: -40 °C to +90°C
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

- ¹⁾ HPUE is only for single carrier.
- ²⁾ Uplink 2 × 2 MIMO is only supported in 5G SA mode.
- ³⁾ 5G NR FDD bands only support 15 kHz SCS, and NR TDD bands only support 30 kHz SCS.
- ⁴⁾ See **document [1]** for bandwidth supported by each frequency band in the NSA and SA modes.
- ⁵⁾ The maximum rates are theoretical and the actual values refer to the network configuration.
- ⁶⁾ To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications.
- ⁷⁾ To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice*, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

2.3. Evaluation Board

To help you develop applications conveniently with the module, Quectel supplies an evaluation board (PCIe Card EVB), a USB to RS-232 converter cable, a USB type-B cable, antennas, and other peripherals to control or test the module. For more details, please refer to **document [2]**.

2.4. Functional Diagram

The following figure shows a block diagram of RM500Q-AE and RM502Q-AE.

- Power management
- Baseband
- LPDDR4X SDRAM + NAND Flash
- Radio frequency
- M.2 Key-B interface

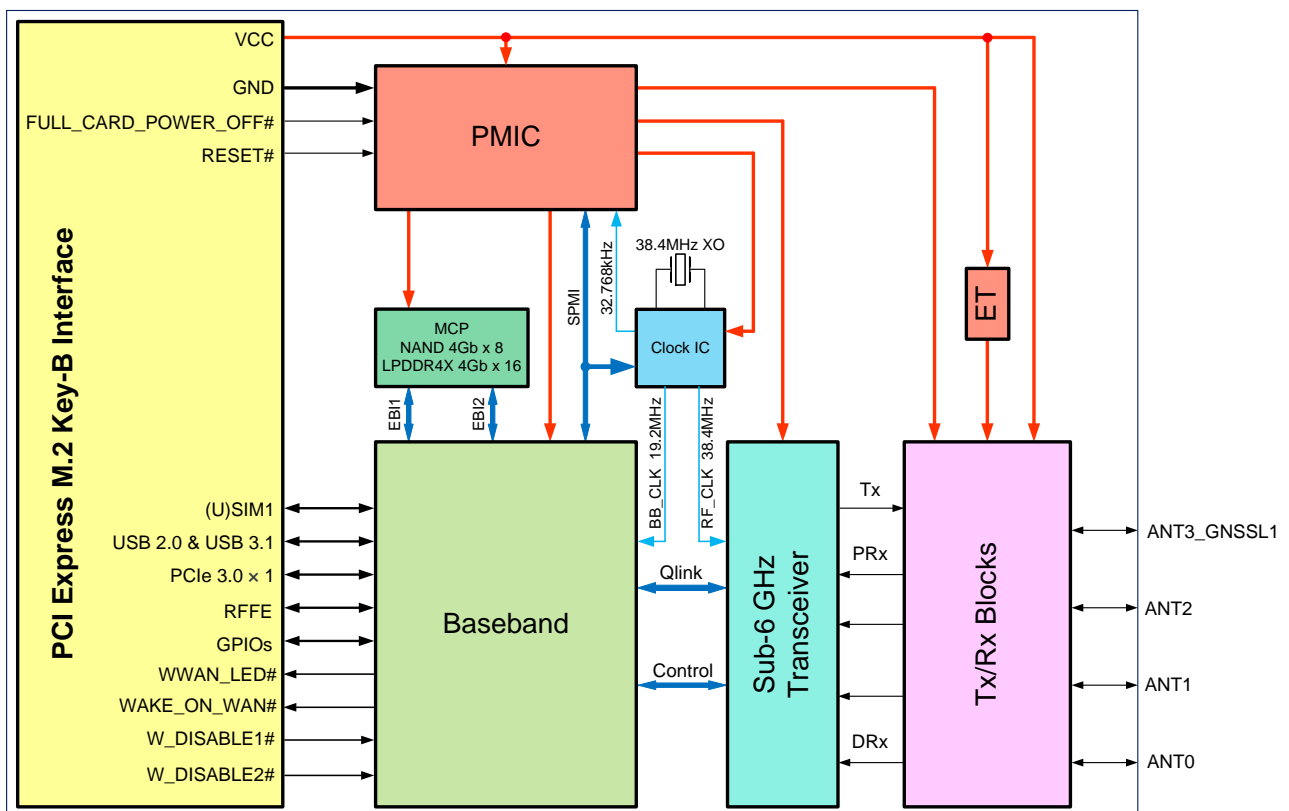


Figure 1: Functional Diagram

2.5. Pin Assignment

The following figure shows the pin assignment of the module. The top side contains the antenna connectors.

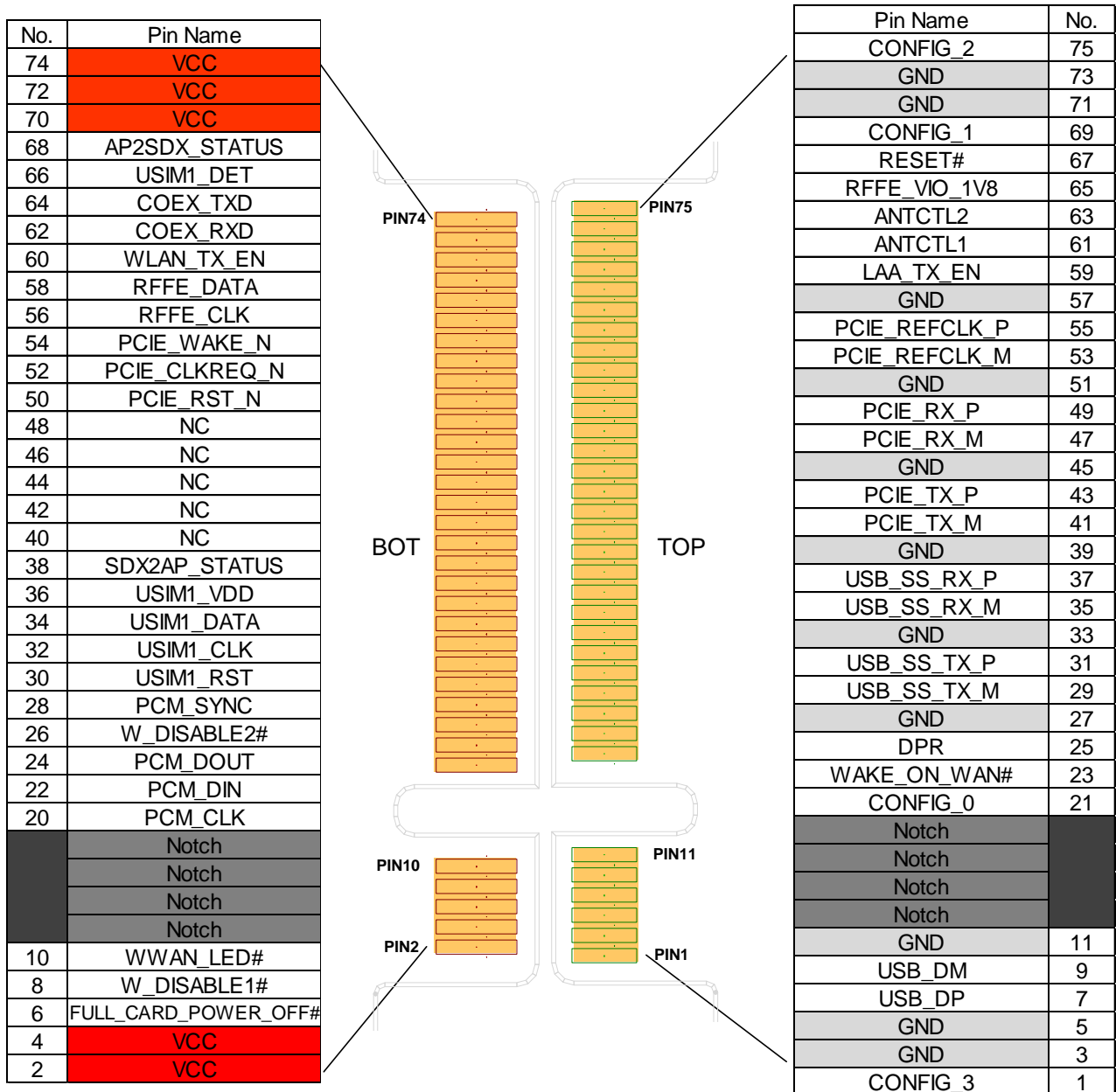


Figure 2: Pin Assignment

2.6. Pin Description

Table 4: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PU	Pull Up
PD	Pull Down

The following table shows the pin definition and description of the module.

Table 5: Pin Description

Pin No.	Pin Name	I/O	Description	DC Characteristic	Comment
1	CONFIG_3	DO	Not connected internally		
2	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
3	GND		Ground		
4	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	

5	GND		Ground		
6	FULL_CARD_POWER_OFF#	DI, PD	Turn on/off the module. High level: Turn on Low level: Turn off	$V_{IHmax} = 4.4\text{ V}$ $V_{IHmin} = 1.19\text{ V}$ $V_{ILmax} = 0.2\text{ V}$	Internally pulled down with a 100 k Ω resistor.
7	USB_DP	AIO	USB 2.0 differential data (+)		
8	W_DISABLE1#	DI, OD	Airplane mode control. Active LOW	1.8/3.3 V	
9	USB_DM	AIO	USB 2.0 differential data (-)		
10	WWAN_LED#	DO, OD	RF status indication LED. Active LOW	VCC	
11	GND		Ground		
12	Notch		Notch		
13	Notch		Notch		
14	Notch		Notch		
15	Notch		Notch		
16	Notch		Notch		
17	Notch		Notch		
18	Notch		Notch		
19	Notch		Notch		
20	PCM_CLK	DIO, PD	PCM data bit clock	1.8 V	
21	CONFIG_0	DO	Not connected internally		
22	PCM_DIN	DI, PD	PCM data input	1.8 V	
23	WAKE_ON_WAN#	DO, OD	Wake up the host. Active LOW	1.8/3.3 V	
24	PCM_DOUT	DO, PD	PCM data output	1.8 V	
25	DPR*	DI, PU	Dynamic power reduction. High level by default.	1.8 V	
26	W_DISABLE2#	DI, OD	GNSS disable control. Active LOW	1.8/3.3 V	

27	GND		Ground	
28	PCM_SYNC	DIO, PD	PCM data frame sync	1.8 V
29	USB_SS_TX_M	AO	USB 3.1 super-speed transmit (-)	
30	USIM1_RST	DO, PD	(U)SIM card reset	USIM1_VDD 1.8/3.0 V
31	USB_SS_TX_P	AO	USB 3.1 super-speed transmit (+)	
32	USIM1_CLK	DO, PD	(U)SIM clock	USIM1_VDD 1.8/3.0 V
33	GND		Ground	
34	USIM1_DATA	DIO, PU	(U)SIM card data	USIM1_VDD 1.8/3.0 V
35	USB_SS_RX_M	AI	USB 3.1 super-speed receive (-)	
36	USIM1_VDD	PO	(U)SIM card power supply	USIM1_VDD 1.8/3.0 V
37	USB_SS_RX_P	AI	USB 3.1 super-speed receive (+)	
38	SDX2AP_STATUS*	DO, PD	Status indication to AP	1.8 V
39	GND		Ground	
40	NC		NC	
41	PCIE_TX_M	AO	PCIe transmit (-)	
42	NC		NC	
43	PCIE_TX_P	AO	PCIe transmit (+)	
44	NC		NC	
45	GND		Ground	
46	NC		NC	
47	PCIE_RX_M	AI	PCIe receive (-)	
48	NC		NC	
49	PCIE_RX_P	AI	PCIe receive (+)	
50	PCIE_RST_N	DI, OD	PCIe reset.	

			Active LOW		
51	GND		Ground		
52	PCIE_CLKREQ_N	DO, OD	PCIe clock request. Active LOW		
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)		
54	PCIE_WAKE_N	DO, OD	PCIe wake up Active LOW		
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)		
56	RFFE_CLK ¹⁾	DO, PD	Used for external MIPI IC control	1.8 V	
57	GND		Ground		
58	RFFE_DATA ¹⁾	DIO, PD	Used for external MIPI IC control	1.8 V	
59	LAA_TX_EN*	DO	Notification from SDR to WLAN when LTE transmitting	1.8 V	
60	WLAN_TX_EN*	DI	Notification from WLAN to SDR while transmitting	1.8 V	
61	ANTCTL1*	DO, PD	Antenna GPIO control	1.8 V	
62	COEX_RXD*	DI, PD	LTE/WLAN coexistence receive data	1.8 V	
63	ANTCTL2*	DO, PD	Antenna GPIO control	1.8 V	
64	COEX_TXD*	DO, PD	LTE/WLAN coexistence transmit data	1.8 V	
65	RFFE_VIO_1V8 ¹⁾	PO	Power supply for antenna tuner	1.8 V. Maximum output current: 50 mA	
66	USIM1_DET	DI, PU	(U)SIM1 card hot-plug detect	1.8 V	Internally pulled up to 1.8 V ²⁾
67	RESET#	DI, PU	Reset the module. Active LOW	V _{IH} max = 1.575 V V _{IH} min = 1.25 V V _{IL} max = 0.45 V	Internally pulled up to 1.5 V with a 100 kΩ resistor
68	AP2SDX_STATUS*	DI, PD	Status indication from AP	1.8 V	
69	CONFIG_1	DO	Connected to GND internally		

70	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
71	GND		Ground	
72	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
73	GND		Ground	
74	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
75	CONFIG_2	DO	Not connected internally	

NOTES

- ¹⁾ If this function is required, please contact Quectel for more details.
- ²⁾ This pin is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.
- Keep all NC, reserved and unused pins unconnected.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes of RM500Q-AE and RM502Q-AE.

Table 6: Overview of Operating Modes

Mode	Details
Normal Operation Mode	Idle Software is active. The module has registered on the network, and it is ready to send and receive data.
	Data Network connected. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	AT+CFUN=0 command sets the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.
Airplane Mode	AT+CFUN=4 command or driving W_DISABLE1# pin LOW will set the module to airplane mode. In this mode, the RF function is invalid.
Sleep Mode	The module keeps receiving paging messages, SMS, voice calls* and TCP/UDP data from the network with its current consumption reducing to the minimal level.
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is inactive, all application interfaces are inaccessible, and the operating voltage (connected to VCC) remains applied.

3.1.1. Sleep Mode

DRX of module is able to reduce the current consumption to a minimum value during the sleep mode, and DRX cycle index values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the current consumption in sleep mode. The longer the DRX cycle is, the lower the current consumption will be.

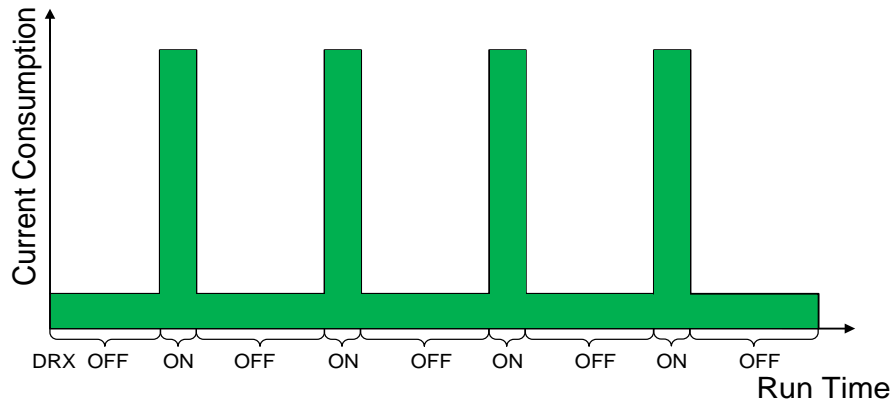


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

The following part of this section presents the power saving procedure and sleep mode of the module.

If the host supports USB suspend/resume and remote wakeup function, the following two conditions must be met to make the module enter sleep mode.

- **AT+QSCLK=1** command is executed to enable the sleep mode.
- Then, the host's USB bus, which is connected to the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

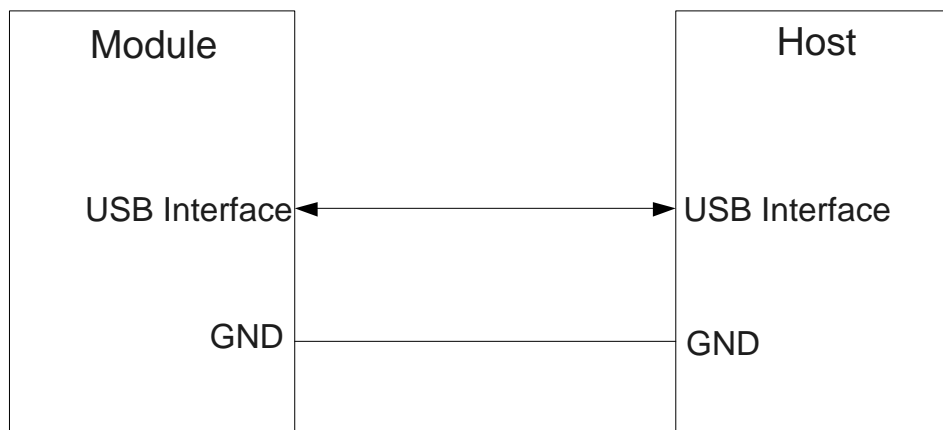


Figure 4: Sleep Mode Application with USB Remote Wakeup

The module and the host will wake up in the following conditions:

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, it will send remote wake-up signals via USB bus to wake up the host.

3.1.2. Airplane Mode

The module provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. See **Chapter 4.5.1** for more details.

3.2. Communication Interface with a Host

The module supports to communicate through both USB and PCIe interfaces, respectively referring to the USB mode and the PCIe mode as described below:

USB Mode

- Supports all USB 2.0/3.1 features
- Supports MBIM/QMI/QRTR/AT
- Communication can be switched to PCIe mode by AT command

USB is the default communication interface between the module and the host. To use PCIe interface for the communication between a host, an AT command under USB mode can be used. For more details about the AT command, see **document [3]**.

It is suggested that USB 2.0 interface be reserved for firmware upgrade.

USB-AT-based PCIe Mode

- Supports MBIM/QMI/QRTR/AT
- Communication can be switched back to USB mode by AT command

When the module works at the USB-AT-based (switched from USB mode by AT command) PCIe mode, it supports MBIM/QMI/QRTR/AT, and can be switched back to USB mode by AT command. But the firmware upgrade via PCIe interface is not supported, so USB 2.0 interface must be reserved for the firmware upgrade.

eFuse-based PCIe Mode

- Supports MBIM/QMI/QRTR/AT
- Supports Non-X86 systems and X86 system (supports BIOS PCIe early initial)

RM500Q-AE and RM502Q-AE can also be reprogrammed to PCIe mode based on eFuse. If switched to PCIe mode by burnt eFuse, the communication cannot be switched back to USB mode.

3.3. Power Supply

The following table shows pin definition of VCC pins and ground pins.

Table 7: Definition of VCC and GND Pins

Pin	Pin Name	I/O	Description	DC Characteristics
2, 4, 70, 72, 74	VCC	PI	Power supply	3.135–4.4 V 3.7 V typical DC supply
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND		Ground	

3.3.1. Decrease Voltage Drop

The power supply range of the module is from 3.135 V to 4.4 V. Please ensure that the input voltage will never drop below 3.135 V, otherwise the module will be powered off automatically. The voltage ripple of the input power supply should be less than 100 mV, and the voltage drop should be less than 165 mV.

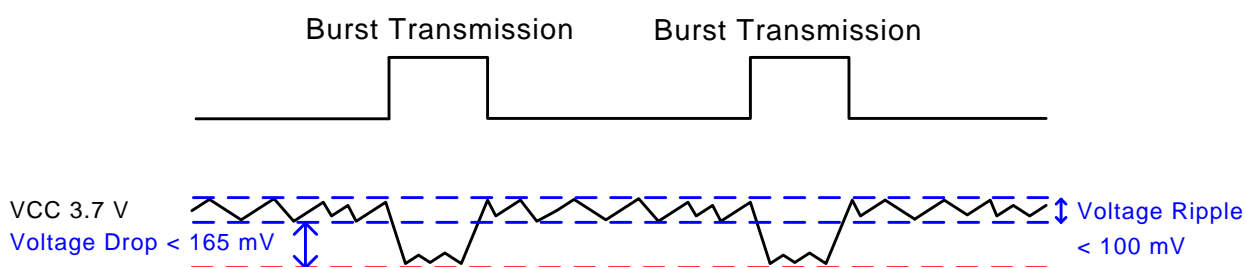


Figure 5: Power Supply Limits during Radio Transmission

Ensure the continuous current capability of the power supply is 3.0 A. To decrease the voltage drop, two bypass capacitor of about 220 μF with low ESR (ESR = 0.7 Ω) should be used. To decrease the power supply is disturbed, a multi-layer ceramic chip capacitor (MLCC) array also should be used due to its ultra-low ESR. It is recommended to use four ceramic capacitors (1 μF , 100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VCC pins. The width of VCC trace should be no less than 2.5 mm. In principle, the longer the VCC trace is, the wider it should be.

In addition, to get a stable power source, it is recommended to use a zener diode with reverse zener voltage of 5.1 V and dissipation power of more than 0.5 W.

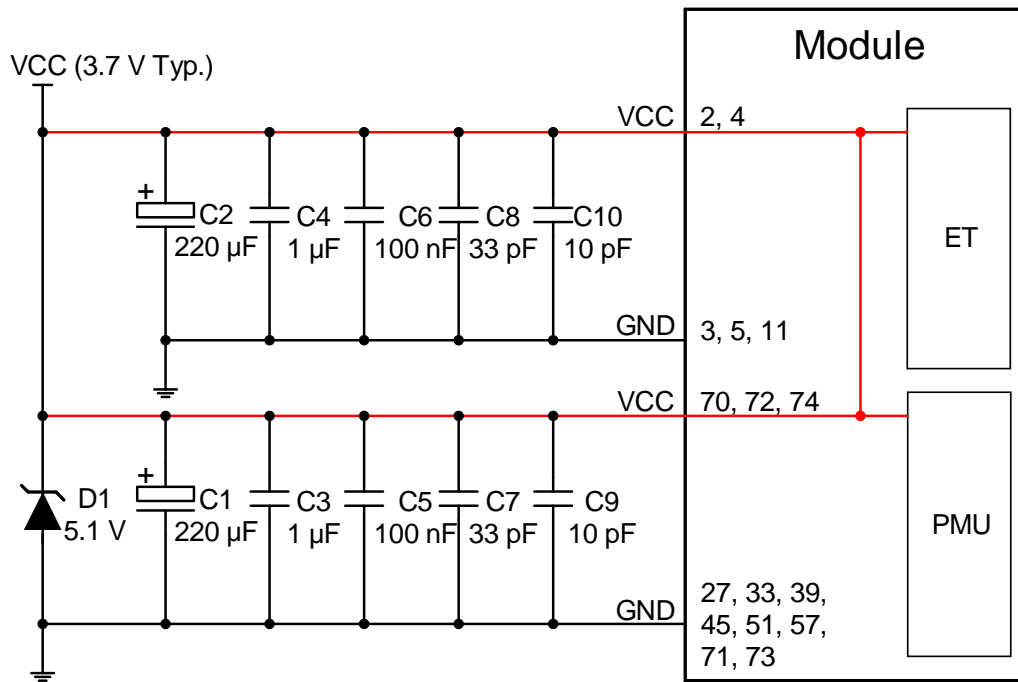


Figure 6: Reference Circuit for VCC

3.3.2. Reference Design for Power Supply

Power design is critical as the module's performance largely depends on its power source. If the voltage difference between the input and output is not too big, it is suggested that an LDO is used when supplying power for the module. If there is a big voltage difference between the input source and the desired output (VCC = 3.7 V Typ.), a buck DC-DC converter is preferred.

The following figure shows a reference design for +5.0 V input power source based on a DC-DC converter. The typical output of the power supply is about 3.7 V and the maximum load current is 3.0 A.

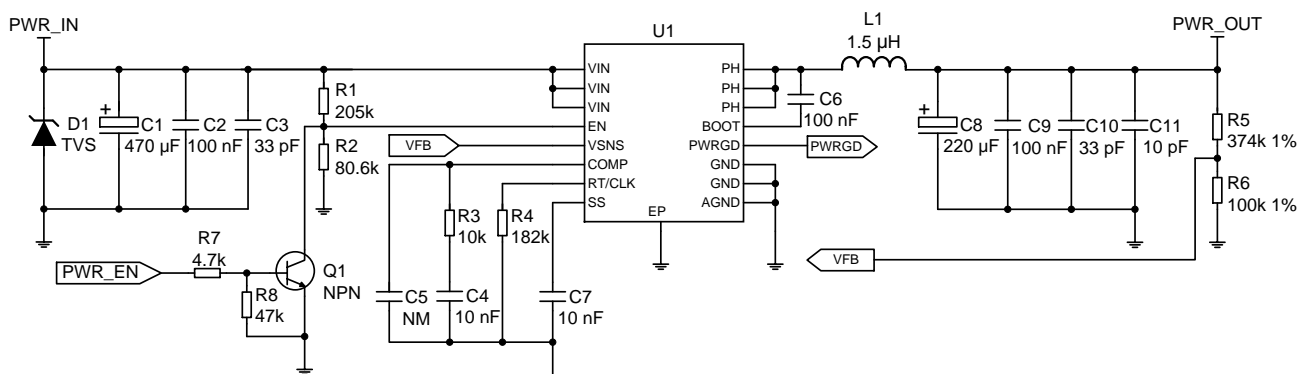


Figure 7: Reference Circuit for Power Supply

NOTE

To avoid damages to the internal flash, DON'T cut off the power supply before the module is completely turned off by pulling down FULL_CARD_POWER_OFF# pin for more than 7 s, and DON'T cut off power supply directly when the module is working.

3.3.3. Monitor the Power Supply

AT+CBC command can be used to monitor the voltage value of VCC. For more details, please refer to *document [3]*.

3.4. Turn on

FULL_CARD_POWER_OFF# (abbreviated as “FCPO#” in this document) asynchronous signal is used to turn on/off the module. When the input signal is driven HIGH (≥ 1.19 V), the module will turn on.

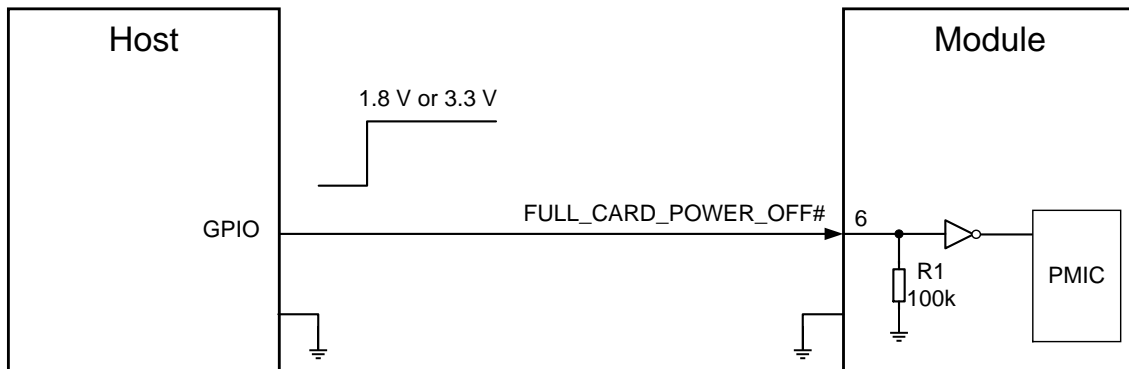
This input signal is 3.3 V tolerant and can be driven by either 1.8 V or 3.3 V GPIO. Also, it has internally pulled down with a 100 k Ω resistor.

The following table shows the definition of FULL_CARD_POWER_OFF#.

Table 8: Definition of FCPO#

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
6	FULL_CARD_POWER_OFF#	DI, PD	Turn on/off the module. High level: Turn on Low level: Turn off	$V_{IHmax} = 4.4$ V $V_{IHmin} = 1.19$ V $V_{ILmax} = 0.2$ V	Pull down with a 100 k Ω resistor.

It is recommended to use a host GPIO to control FULL_CARD_POWER_OFF#. A simple reference circuit is illustrated in the following figure.



NOTE: The voltage of pin 6 should be no less than 1.19V when it is at HIGH level.

Figure 8: Turn on the Module with a Host GPIO

The timing of turn-on scenario is illustrated by the following figure.

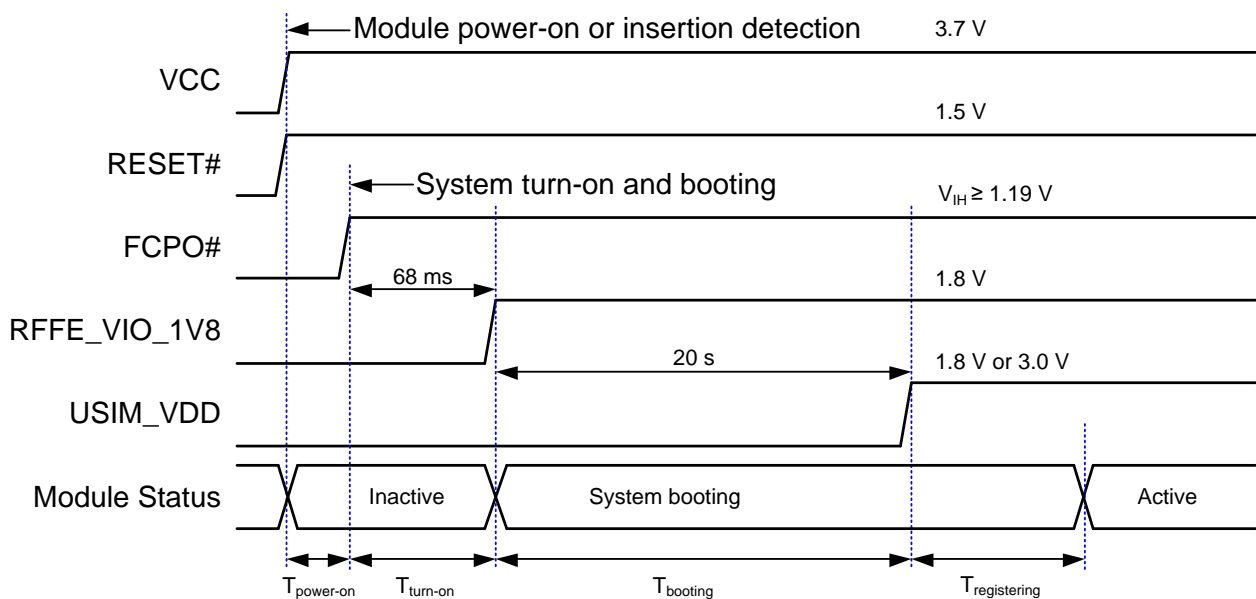


Figure 9: Turn-on Timing of the Module

Table 9: Trun-on Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
$T_{power-on}$	0 ms	20 ms	-	System power-on time depending on the host.

$T_{\text{turn-on}}$	-	68 ms	-	Module system turn-on time.
T_{booting}	20 s	22 s	-	Module system booting time.
$T_{\text{registering}}$	-	-	-	Network registering time related to network CSQ.

3.5. Turn off

3.5.1. Turn off the Module through FCPO#

For the design that turns on the module with a host GPIO, when the power is supplied to VCC, driving FULL_CARD_POWER_OFF# pin LOW ($\leq 0.2\text{ V}$) or tri-stating the pin will turn off the module.

The timing of turning-off scenario is illustrated by the following figure.

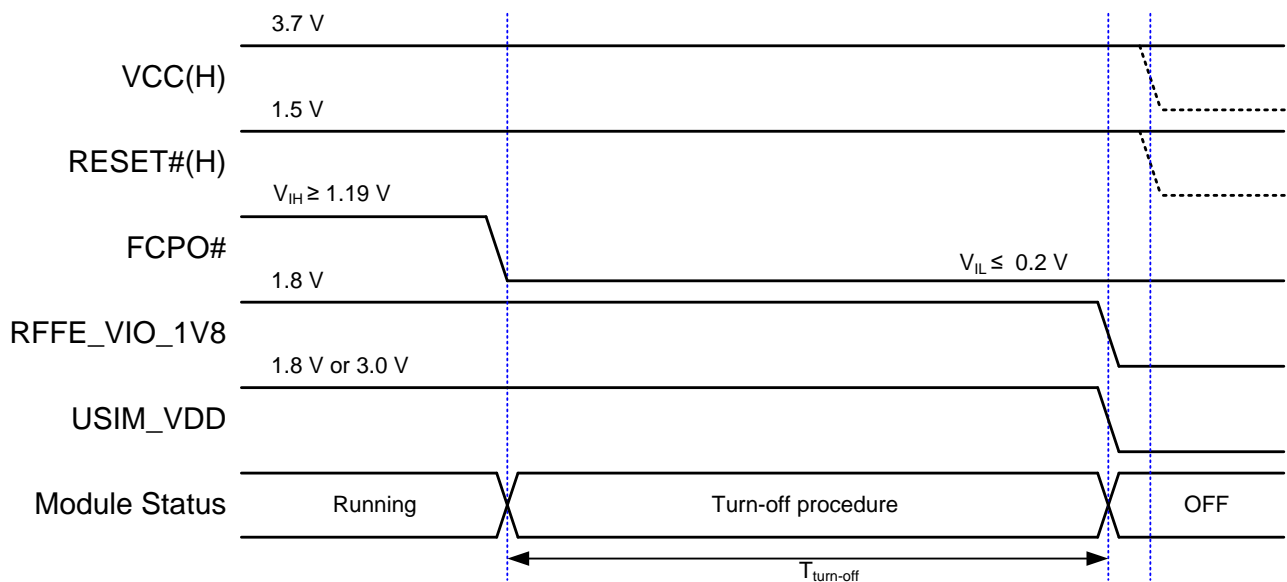


Figure 10: Turn-off Timing through FCPO#

Table 10: Turn-off Timing of the Module through FCPO#

Symbol	Min.	Typ.	Max.	Comment
$T_{\text{turn-off}}$	6.84 s	-	-	Module system turn-off time.

3.5.2. Turn off the Module through AT Command

It is also a safe method to turn off the module by **AT+QPOWD** command. For more details about the command, see **document [3]**.

The module is designed to be turned on with a host GPIO. Pull down FULL_CARD_POWER_OFF# pin after the module's USB/PCIe is removed. Otherwise, the module will be turned on again.

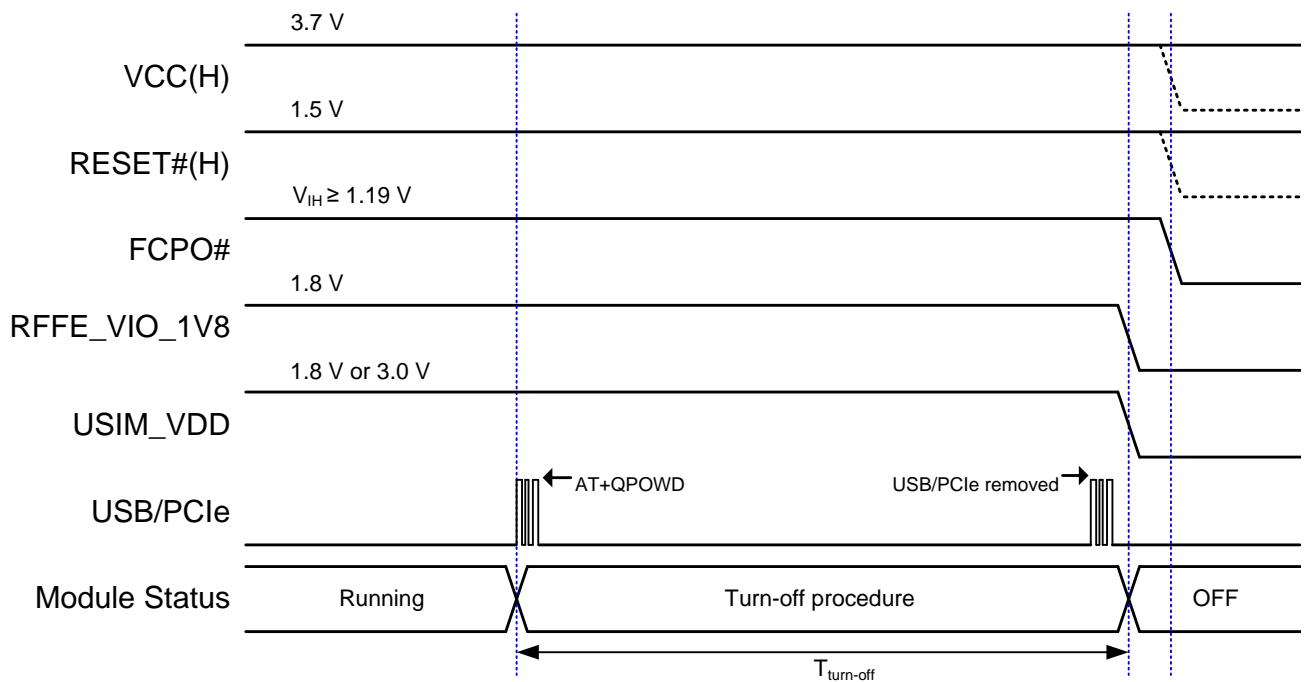


Figure 11: Turn-off Timing through AT Command and FCPO#

Table 11: Turn-off Timing of the Module through AT Command and FCPO#

Symbol	Min.	Typ.	Max.	Comment
$T_{\text{turn-off}}$	6.84 s	-	-	Module system turn-off time.

NOTES

1. Please pull down FULL_CARD_POWER_OFF# pin immediately or cut off the power supply VCC when the host detects that the module USB/PCIe is removed.
2. It is recommended to cut off the VCC after the module is turned off.

3.6. Reset

RESET# is an asynchronous and active LOW signal (1.5 V logic level). Whenever this pin is active, the module will immediately enter Power On Reset (POR) condition.

Please note that triggering the RESET# signal will lead to loss of all data in the modem and removal of system drivers. It will also disconnect the modem from the network.

Table 12: Definition of RESET# Pin

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
67	RESET#	DI, PU	Reset the module. Active LOW	$V_{IHmax} = 1.575\text{ V}$ $V_{IHmin} = 1.25\text{ V}$ $V_{ILmax} = 0.45\text{ V}$	Internally pulled up to 1.5 V with a 100 k Ω resistor.

The module can be reset by pulling down the RESET# pin for 250–600 ms. An open collector/drain driver or a button can be used to control the RESET# pin.

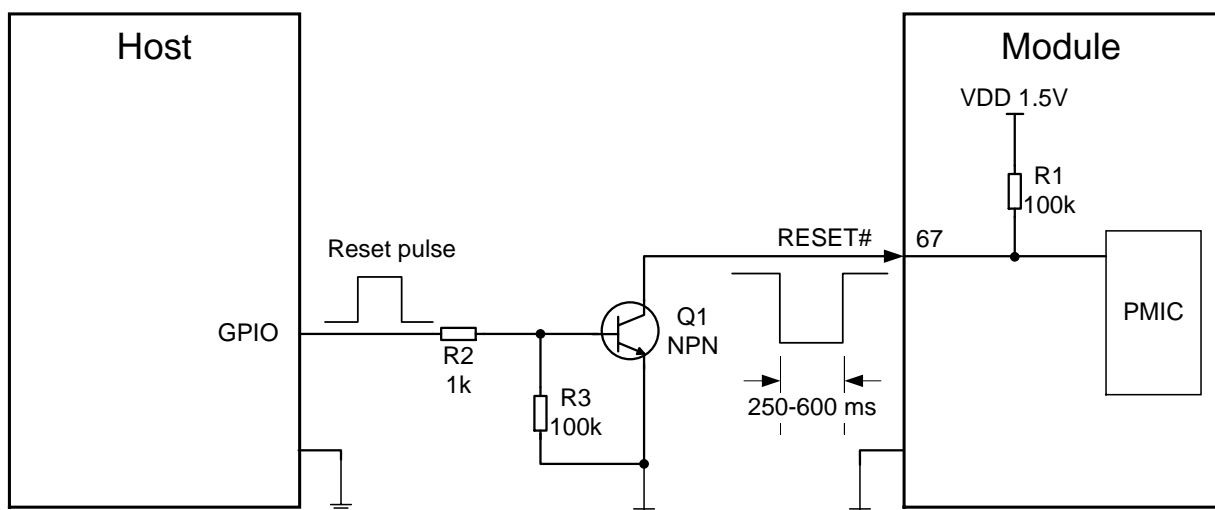
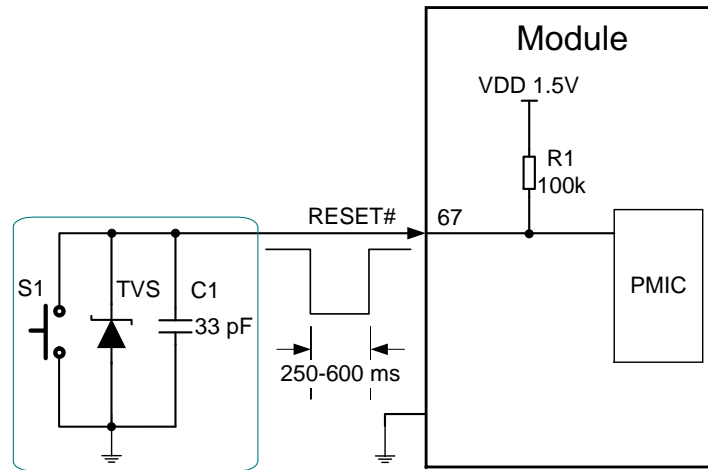


Figure 12: Reference Circuit of RESET# with NPN Driver Circuit



NOTE: The capacitor C1 is recommended to be less than 47 pF.

Figure 13: Reference Circuit of RESET# with a Button

The timing of reset scenario is illustrated in the following figure.

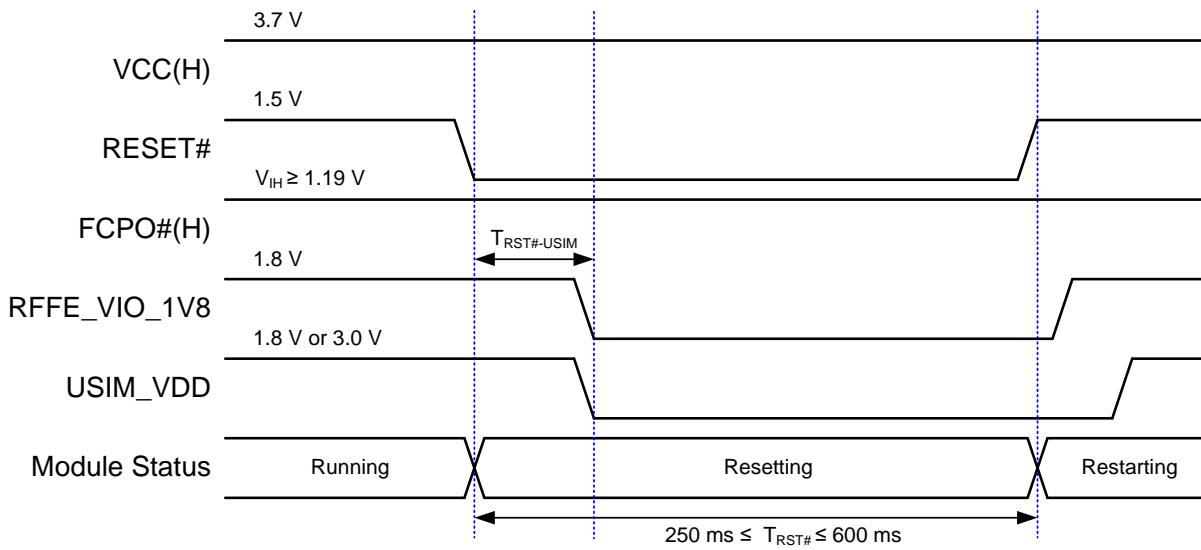


Figure 14: Reset Timing of the Module

Table 13: Reset Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
$T_{RST\#-USIM}$	200 ms	-	-	(U)SIM card turn-off time.
$T_{RST\#}$	250 ms	400 ms	600 ms	More than 600 ms will lead to repeated module reset.

4 Application Interfaces

The physical connections and signal levels of RM500Q-AE and RM502Q-AE comply with the PCI Express M.2 specification. This chapter mainly describes the definition and application of the following interfaces/pins of the module:

- (U)SIM interfaces
- USB interface
- PCIe interface
- PCM interface
- Control and indication interfaces
- Cellular/WLAN COEX interface*
- Antenna tuner control interface*
- Configuration pins

4.1. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported.

4.1.1. Pin definition of (U)SIM

RM500Q-AE and RM502Q-AE support single (U)SIM slot.

Table 14: Pin Definition of (U)SIM Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
36	USIM1_VDD	PO	Power supply for (U)SIM1 card	1.8/3.0 V
34	USIM1_DATA	DIO, PU	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V
32	USIM1_CLK	DO, PD	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V
30	USIM1_RST	DO, PD	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V

66 USIM1_DET DI, PU (U)SIM1 card hot-plug detect Internally pulled up to 1.8 V ¹⁾

NOTE

¹⁾ This pin is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

4.1.2. (U)SIM Hot-plug

The module supports (U)SIM card hot-plug via the (U)SIM card hot-plug detection pin (USIM1_DET). (U)SIM card insertion is detected by high/low level. (U)SIM card hot-plug is disabled by default.

The following command enables (U)SIM card hot-plug function.

AT+QSIMDET (U)SIM Card Detection	
Test Command AT+QSIMDET=?	Response +QSIMDET: (list of supported <enable>s),(list of supported <insert_level>s) OK
Read Command AT+QSIMDET?	Response +QSIMDET: <enable> , <insert_level> OK
Write Command AT+QSIMDET=<enable>,<insert_level>	Response OK If there is any error: ERROR
Maximum Response Time	300 ms
Characteristics	The command takes effect after the module is restarted. The configuration will be saved automatically.

Parameter

<enable>	Integer type. Enable or disable (U)SIM card detection. 0 Disable 1 Enable
<insert_level>	Integer type. The level of (U)SIM detection pin when a (U)SIM card is inserted. 0 Low level 1 High level

NOTES

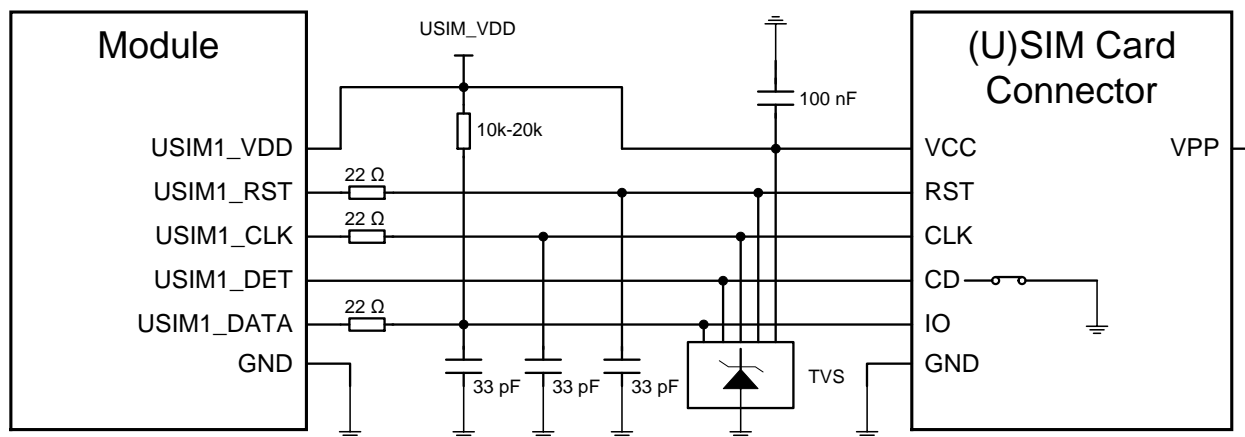
- Hot-plug function is invalid if the configured value of `<insert_level>` is inconsistent with hardware design.
- Hot-plug function setting takes effect after the module is restarted.
- The underlined value is the default parameter value.
- USIM1_DET is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

4.1.3. Normally Closed (U)SIM Card Connector

With a normally closed (U)SIM card connector, USIM1_DET pin is shorted to ground when there is no (U)SIM card inserted. (U)SIM card detection by high level is applicable to this type of connector. After executing **AT+QSIMDET=1,1** to enable the (U)SIM hot-plug: when a (U)SIM card is inserted, USIM1_DET will change from low to high level; when the (U)SIM card is removed, USIM1_DET will change from high to low level.

- When the (U)SIM is absent, CD is shorted to ground and USIM1_DET is at low level.
- When the (U)SIM is present, CD is open from ground and USIM1_DET is at high level.

The following figure shows a reference design for (U)SIM interface with a normally closed (U)SIM card connector.



NOTE: All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

Figure 15: Reference Circuit for Normally Closed (U)SIM Card Connector

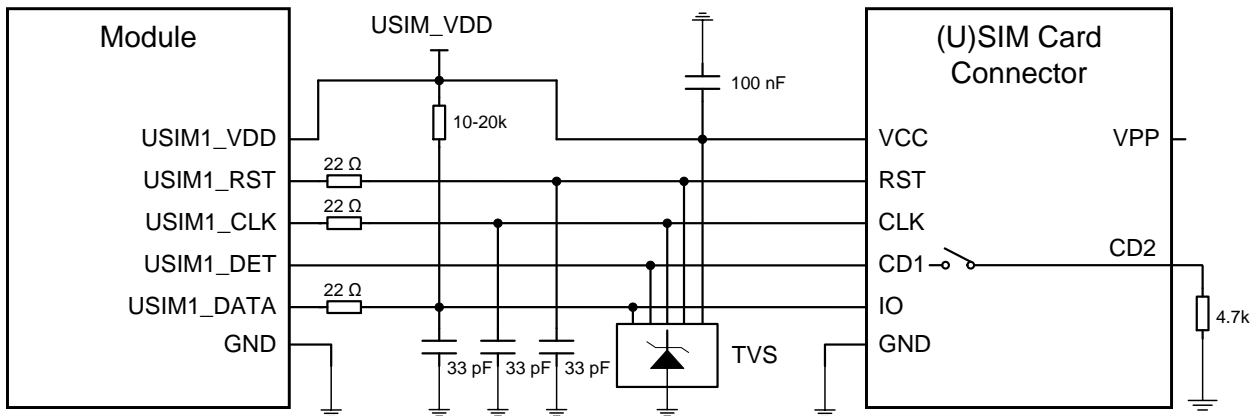
4.1.4. Normally Open (U)SIM Card Connector

With a normally open (U)SIM card connector, CD1 and CD2 of the connector are disconnected when there is no (U)SIM card inserted. (U)SIM card detection by low level is applicable to this type of connector. After executing **AT+QSIMDET=1,0** to enable the (U)SIM hot-plug: when a (U)SIM card is inserted,

USIM1_DET will change from high to low level; when the (U)SIM card is removed, USIM1_DET will change from low to high level.

- When the (U)SIM is absent, CD1 is open from CD2 and USIM1_DET is at high level.
- When the (U)SIM is present, CD1 is pull down to ground and USIM1_DET is at low level.

The following figure shows a reference design for (U)SIM interface with a normally open (NO) (U)SIM card connector.

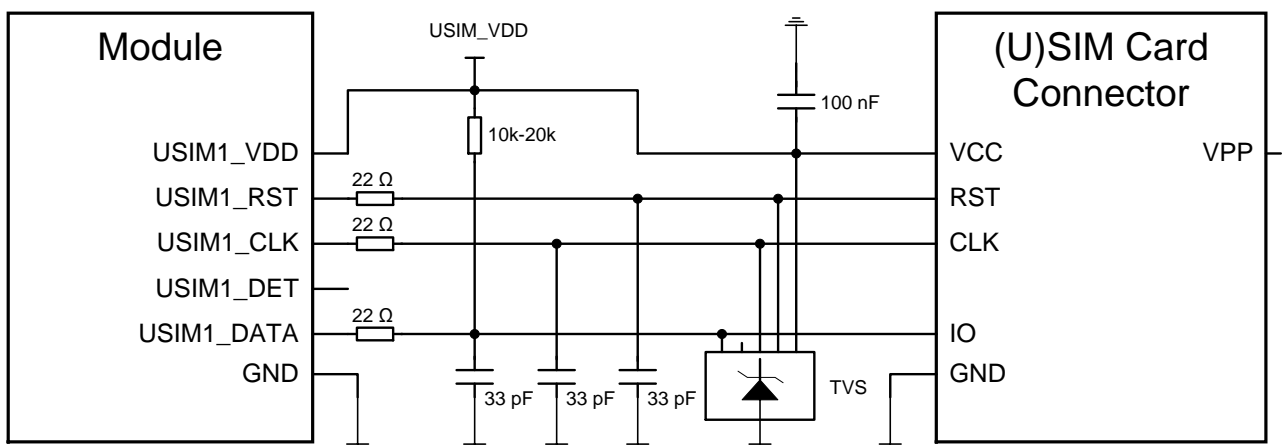


NOTE: All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

Figure 16: Reference Circuit for Normally Open (U)SIM Card Connector

4.1.5. (U)SIM Card Connector Without Hot-plug

If (U)SIM card hot-plug is not needed, please keep USIM1_DET unconnected. A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated by the following figure.



NOTE: All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

Figure 17: Reference Circuit for a 6-Pin (U)SIM Card Connector

4.1.6. (U)SIM Design Notices

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm.
- Keep (U)SIM card signals away from RF and VCC traces.
- Make sure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS diode array of which the parasitic capacitance should be not higher than 10 pF. Add 22 Ω resistors in series between the module and the (U)SIM card connector to suppress EMI such as spurious transmission, and to enhance ESD protection. The 33 pF capacitors are used to filter out RF interference.
- For USIM_DATA, a 10–20 k Ω pull-up resistor must be added near the (U)SIM card connector.

4.2. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.1 & 2.0 specifications and supports super speed (10 Gbps) on USB 3.1 and high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade.

Please note that only USB 2.0 can be used for firmware upgrade currently.

The following table shows the pin definition of USB interface.

Table 15: Pin Definition of USB Interface

Pin No.	Pin Name	I/O	Description	Comment
7	USB_DP	AIO	USB differential data bus (+)	Require differential impedance of 90 Ω
9	USB_DM	AIO	USB differential data bus (-)	
29	USB_SS_TX_M	AO	USB 3.1 super-speed transmit (-)	
31	USB_SS_TX_P	AO	USB 3.1 super-speed transmit (+)	

35	USB_SS_RX_M	AI	USB 3.1 super-speed receive (-)
37	USB_SS_RX_P	AI	USB 3.1 super-speed receive (+)

For more details about the USB 3.1 & 2.0 specifications, please visit <http://www.usb.org/home>.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in designs. The following figure shows a reference circuit of USB 3.1 & 2.0 interface.

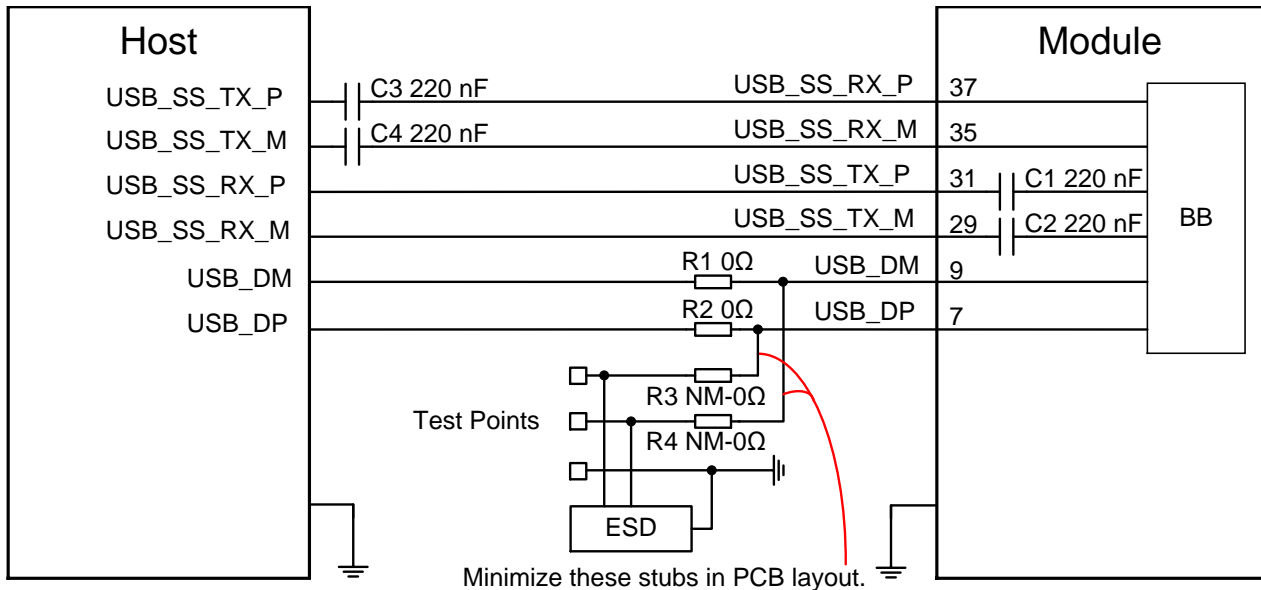


Figure 18: Reference Circuit of USB 3.1 & 2.0 Interface

AC coupling capacitors C3 and C4 must be placed close to the host and close to each other. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB. To ensure the signal integrity of USB 2.0 data traces, R1, R2, R3 and R4 must be placed close to the module, and the stubs must be minimized in PCB layout.

You should follow the principles below when designing for the USB interface to meet USB 3.1 and 2.0 specifications:

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of differential trace of USB 2.0 and 3.1 is 90 Ω.
- For USB 2.0 signal traces, the trace length should be less than 120 mm, and the differential data pair matching should be less than 2 mm. For USB 3.1 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 0.7 mm, while the matching between Tx and Rx should be less than 10 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.

- Junction capacitance of the ESD protection device might cause influences on USB data lines, so you should pay attention to the selection of the device. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.15 pF for USB 3.1.
- Keep the ESD protection devices as close to the USB connector as possible.
- If possible, reserve 0 Ω resistors on USB_DP and USB_DM lines respectively.

4.3. PCIe Interface

The module provides one integrated PCIe (Peripheral Component Interconnect Express) interface.

- PCI Express Base Specification Revision 3.0 compliant
- Data rate up to 8 Gbps per lane

4.3.1. PCIe Operating Mode

The module supports endpoint (EP) mode and root complex (RC) mode. In EP mode, the module is configured as a PCIe EP device. In RC mode, the module is configured as a PCIe root complex.

AT+QCFG="pcie/mode" is used to set PCIe RC/EP mode.

AT+QCFG="pcie/mode" Set PCIe RC/EP Mode	
Write Command AT+QCFG="pcie/mode"[,<mode>]	Response If the optional parameter is omitted, query the current setting: +QCFG: "pcie/mode",<mode> OK If the optional parameter is specified, set PCIe RC/EP mode: OK If there is any error: ERROR
Maximum Response Time	300 ms
Characteristics	The command takes effect after the module is restarted. The configuration will be saved automatically.

Parameter

<mode>	Integer type. Set PCIe RC or EP mode. 0 PCIe EP mode.
--------	--

1 PCIe RC mode.

NOTES

1. The underlined value is the default parameter value.
2. For more details about the command, see **document [3]**.

4.3.2. Pin Definition of PCIe

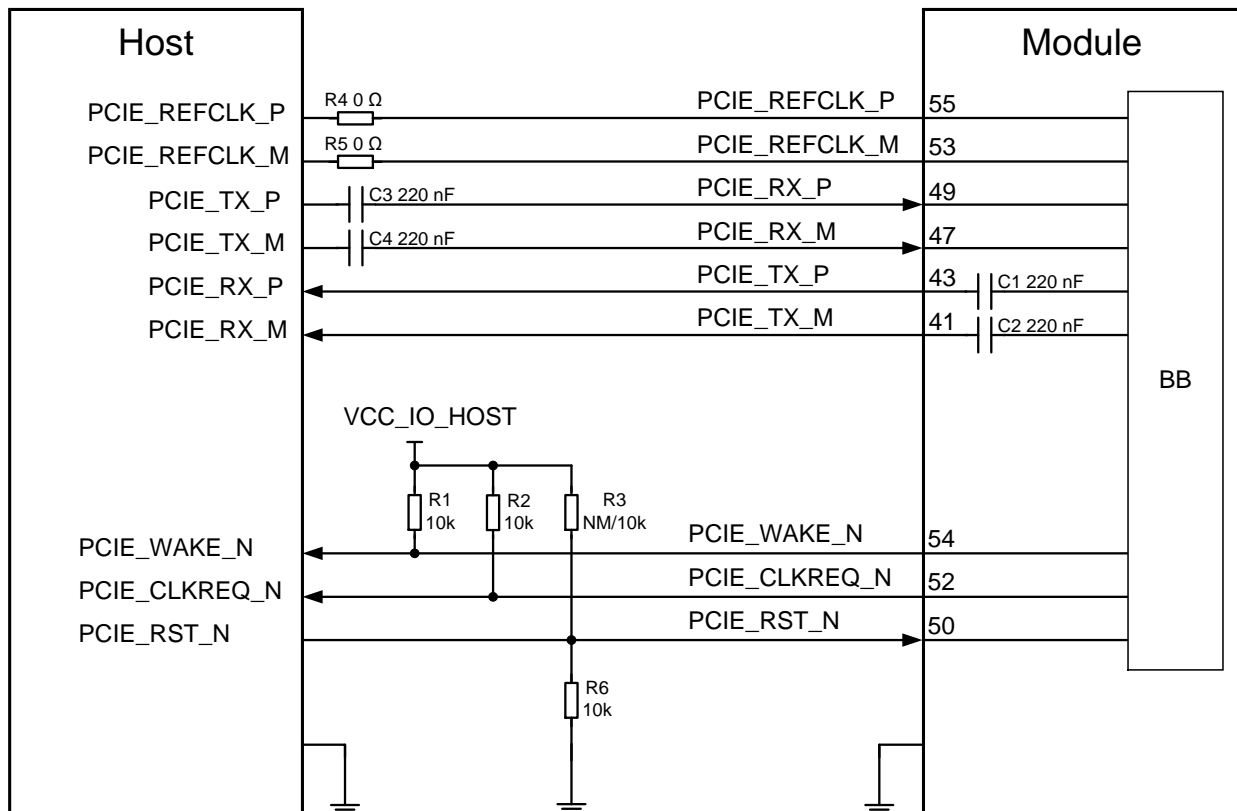
The following table shows the pin definition of PCIe interface.

Table 16: Pin Definition of PCIe Interface

Pin No.	Pin Name	I/O	Description	Comment
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)	100 MHz.
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	Require differential impedance of 85 Ω
49	PCIE_RX_P	AI	PCIe receive (+)	Require differential impedance of 85 Ω
47	PCIE_RX_M	AI	PCIe receive (-)	
43	PCIE_TX_P	AO	PCIe transmit (+)	Require differential impedance of 85 Ω
41	PCIE_TX_M	AO	PCIe transmit (-)	
50	PCIE_RST_N	DI, OD	PCIe reset. Active LOW	
52	PCIE_CLKREQ_N	DO, OD	PCIe clock request. Active LOW	
54	PCIE_WAKE_N	DO, OD	PCIe wake up. Active LOW	

4.3.3. Reference Design for PCIe

The following figure shows a reference circuit for the PCIe interface.



NOTE: The voltage level VCC_IO_HOST of these three signals depend on the host side due to open drain.

Figure 19: PCIe Interface Reference Circuit

To ensure the signal integrity of PCIe interface, AC coupling capacitors C3 and C4 should be placed close to the host on PCB. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB.

The following principles of PCIe interface design should be complied with to meet PCIe specification.

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, crystal, and oscillator signals.
- Add a capacitor in series on Tx/Rx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length matching of each differential data pair (Tx/Rx) less than 0.7 mm for PCIe routing traces.
- Keep the differential impedance of PCIe data trace as $85 \Omega \pm 10 \%$.
- You must not route PCIe data traces under components or cross them with other traces.

4.3.4. PCIe Timing

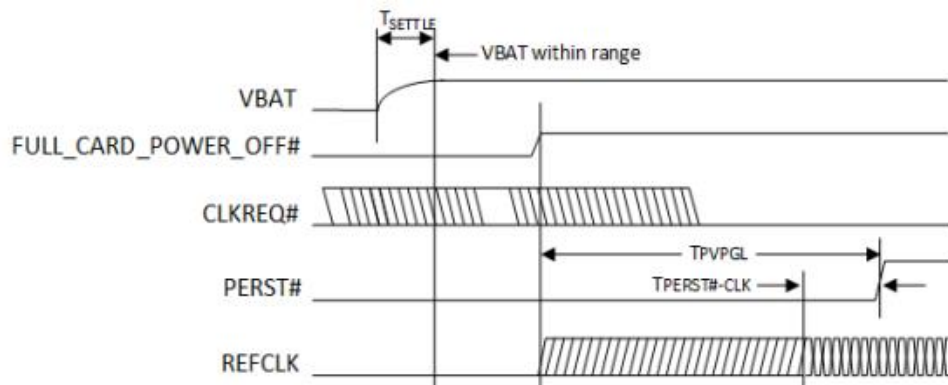


Figure 20: PCIe Power-up Timing of M.2 Specification

Table 17: PCIe Power-up Timing of M.2 Specification

Symbol	Min.	Typ.	Max.	Comment
TPV PGL	50 ms	-	-	Power valid to PERST# Input inactive
T _{PERST#-CLK}	100 μs	-	-	REFCLK stable before PERST# inactive

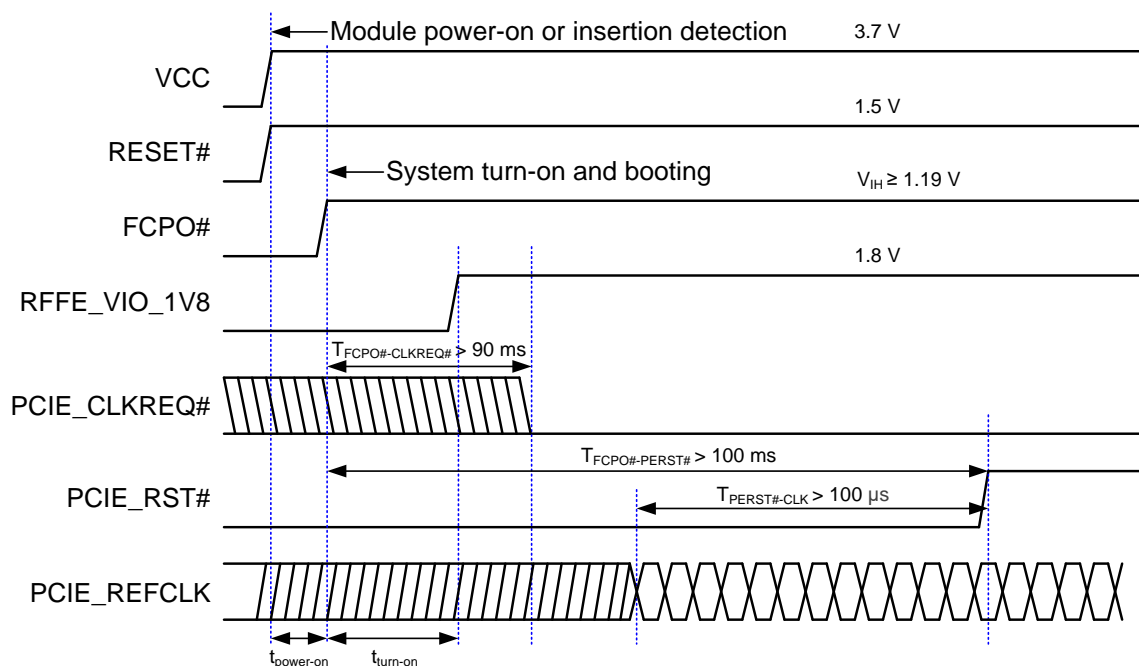


Figure 21: PCIe Power-up Timing of the Module

Table 18: PCIe Turn-on Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
T _{power-on}	0 ms	20 ms	-	Module power-on time depending on the host.
T _{turn-on}	-	68 ms	-	Module system turn on time.
T _{FCPO#-CLKREQ#}	90 ms	100 ms	-	PCIe clock request.
T _{FCPO#-PERST#}	100 ms	-	-	PCIe reset.
T _{PERST#-CLK}	100 μs	-	-	The time period during which REFCLK is stable before PERST# is inactive.

4.4. PCM Interface

The module supports audio communication via Pulse Code Modulation (PCM) digital interface. The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave.
- Auxiliary mode (long frame synchronization): the module works as master only.

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

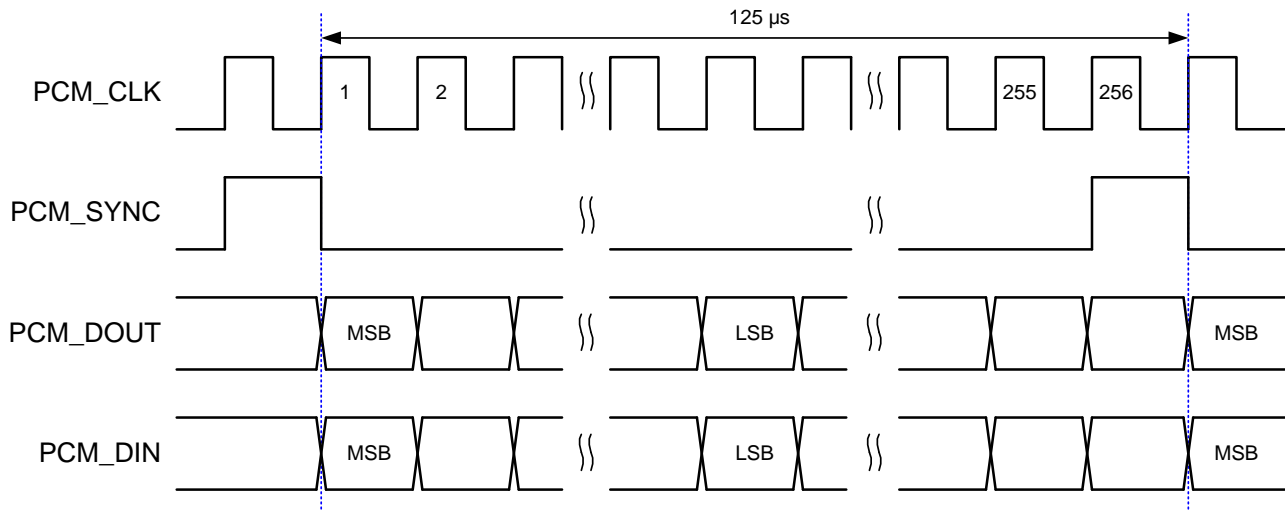


Figure 22: Primary Mode Timing

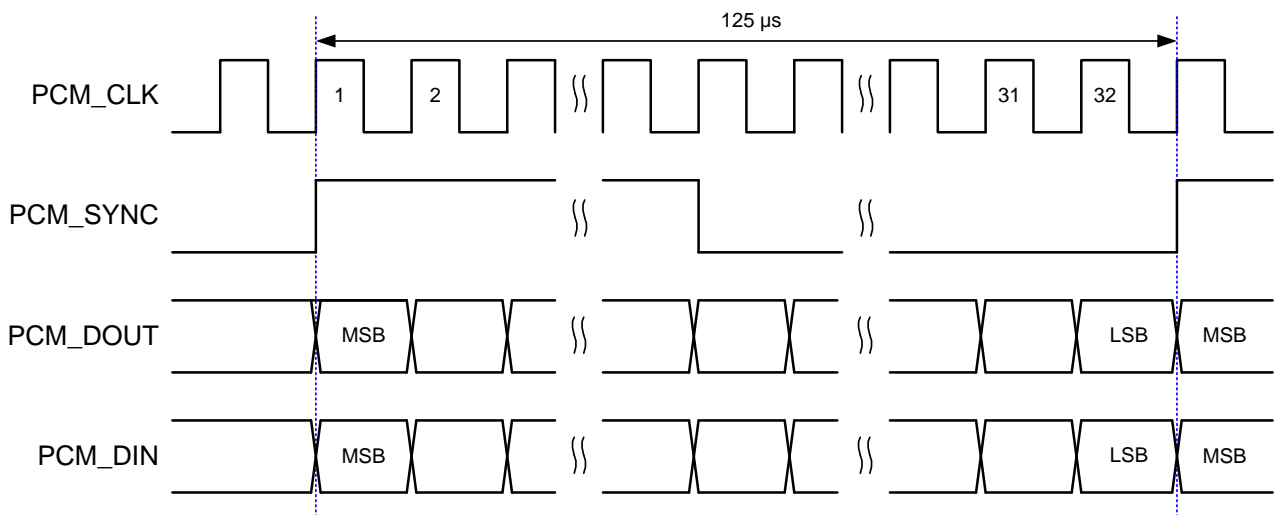


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM interface which can be applied to audio codec design.

Table 19: Pin Definition of PCM Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
20	PCM_CLK	DIO, PD	PCM data bit clock	1.8 V
22	PCM_DIN	DI, PD	PCM data input	1.8 V
24	PCM_DOUT	DO, PD	PCM data output	1.8 V

28	PCM_SYNC	DIO, PD	PCM data frame sync	1.8 V
----	----------	---------	---------------------	-------

The clock and mode can be configured by AT command, and the default configuration is slave mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See [document \[3\]](#) for details about **AT+QDAI** command.

4.5. Control and Indication Interfaces

The following table shows the pin definition of control and indication pins.

Table 20: Pin Definition of Control and Indication Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristics
8	W_DISABLE1#	DI, OD	Airplane mode control. Pulled up by default. Active LOW	1.8/3.3 V
26	W_DISABLE2#	DI, OD	GNSS disable control. Pulled up by default. Active LOW	1.8/3.3 V
10	WWAN_LED#	DO, OD	Indicate RF status of the module. Open drain.	VCC
23	WAKE_ON_WAN#	DO, OD	Wake up the host. Open drain.	1.8/3.3 V
25	DPR*	DI, PU	Dynamic power reduction. High level by default.	1.8 V
38	SDX2AP_STATUS*	DO, PD	Status indication to AP	1.8 V
68	AP2SDX_STATUS*	DI, PD	Status indication from AP	1.8 V

4.5.1. W_DISABLE1#

The module provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. W_DISABLE1# is pulled up by default. Driving it LOW will set the module to airplane mode. In airplane mode, the RF function will be disabled.

The RF function can also be enabled or disabled through AT commands. The following table shows the AT command and corresponding RF function status of the module.

Table 21: RF Function Status

W_DISABLE1# Level	AT Commands	RF Function Status
High Level	AT+CFUN=1	Enabled
	AT+CFUN=0 AT+CFUN=4	Disabled
Low Level	AT+CFUN=0 AT+CFUN=1 AT+CFUN=4	Disabled

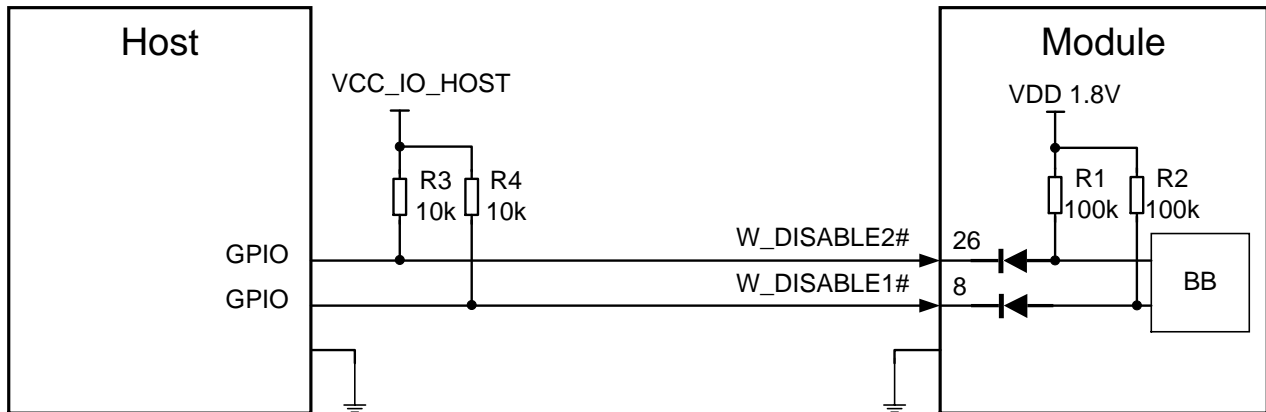
4.5.2. W_DISABLE2#

The module provides a W_DISABLE2# pin to disable or enable the GNSS function. The W_DISABLE2# pin is pulled up by default. Driving it LOW will disable the GNSS function. The combination of W_DISABLE2# pin and AT commands can control the GNSS function.

Table 22: GNSS Function Status

W_DISABLE2# Level	AT Commands	GNSS Function Status
High Level	AT+QGPS=1	Enabled
High Level	AT+QGSEND	Disabled
Low Level	AT+QGPS=1	Disabled
Low Level	AT+QGSEND	

A simple level shifter based on diodes is used on W_DISABLE1# pin and W_DISABLE2# pin which are pulled up to a 1.8 V voltage in the module, as shown in the following figure. So, the control signals (GPIO) of the host device could be at 1.8 V or 3.3 V voltage level. W_DISABLE1# and W_DISABLE2# are active LOW signals, and a reference circuit is shown as below.



NOTE: The voltage level of VCC_IO_HOST could be 1.8 V or 3.3 V typically.

Figure 24: W_DISABLE1# and W_DISABLE2# Reference Circuit

4.5.3. WWAN_LED#

The WWAN_LED# signal is used to indicate RF status of the module, and its sink current is up to 10 mA.

To reduce current consumption of the LED, a current-limited resistor must be placed in series with the LED, as illustrated in the figure below. The LED is ON when the WWAN_LED# signal is at low level.

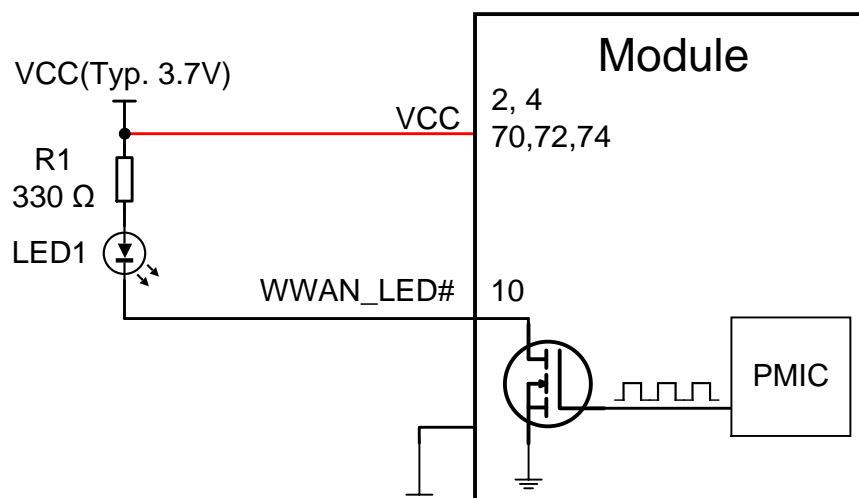


Figure 25: WWAN_LED# Reference Circuit

The following table shows the RF status indicated by WWAN_LED#.

Table 23: Network Status Indications of WWAN_LED#

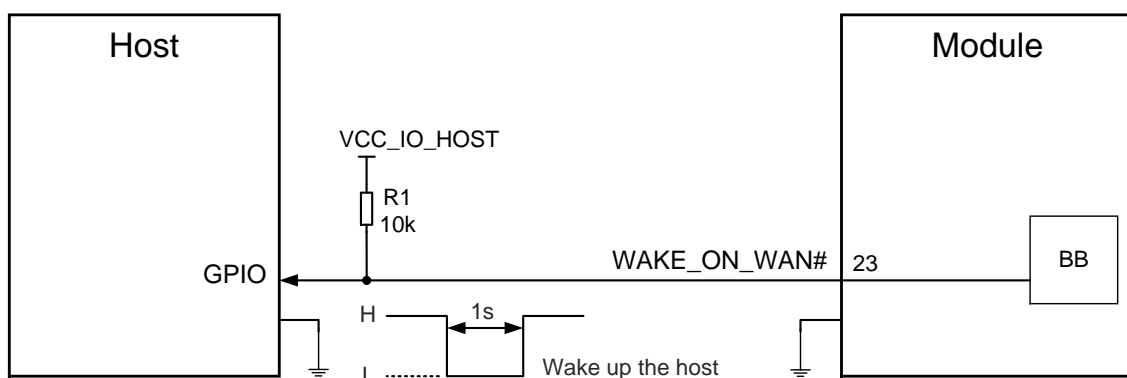
WWAN_LED# Level	Description
Low Level (LED ON)	RF function is turned on
High Level (LED OFF)	RF function is turned off if any of the following occurs: <ul style="list-style-type: none"> ● The (U)SIM card is not powered. ● W_DISABLE1# is at low level (airplane mode enabled). ● AT+CFUN=4 (RF function disabled).

4.5.4. WAKE_ON_WAN#

The WAKE_ON_WAN# is an open drain pin, which requires a pull-up resistor on the host. When a URC returns, a 1 s low level pulse signal will be outputted to wake up the host. The module operation status indicated by WAKE_ON_WAN# is shown as below.

Table 24: State of the WAKE_ON_WAN#

WAKE_ON_WAN# State	Module Operation Status
Output a 1 s low level pulse signal	Data is incoming (to wake up the host)
Always at high level	Idle/Sleep



NOTE:
The voltage level on VCC_IO_HOST depends on the host side due to the open drain in pin 23.

Figure 26: WAKE_ON_WAN# Signal Reference Circuit

4.5.5. DPR*

The module provides the DPR (Dynamic Power Reduction) pin for body SAR (Specific Absorption Rate) detection. The signal is sent from a host system proximity sensor to the module to provide an input trigger, which will reduce the output power in radio transmission.

Table 25: Function of the DPR Signal

DPR Level	Function
High/Floating	NO max. transmitting power backoff
Low	Max. transmitting power backoff by AT+QCFG="sarcfg"

NOTE

See *document [3]* for more details about **AT+QCFG="sarcfg"** command.

4.5.6. STATUS*

The module provides two status indication pins for communication with IPQ807x device. Pin 38 (SDX2AP_STATUS) outputs the status indication signal to IPQ807x device, and pin 68 (AP2SDX_STATUS) inputs the status indication signal from IPQ807x device. For more details, see *document [4]*.

4.6. Cellular/WLAN COEX Interface*

The module provides the cellular/WLAN COEX interface, the following table shows the pin definition of this interface.

Table 26: Pin Definition of COEX Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
59	LAA_TX_EN*	DO	Notification from SDR to WLAN when LTE transmitting	1.8 V
60	WLAN_TX_EN*	DI	Notification from WLAN to SDR while transmitting	1.8 V

62	COEX_RXD*	DI, PD	LTE/WLAN coexistence receive	1.8 V
64	COEX_TXD*	DO, PD	LTE/WLAN coexistence transmit	1.8 V

4.7. Antenna Tuner Control Interface*

ANTCTL[1:2] and RFFE interface are used for antenna tuner control and should be routed to an appropriate antenna control circuit. More details about the interface will be added in the future version of this document.

Table 27: Pin Definition of Antenna Tuner Control Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
56	RFFE_CLK ¹⁾	DO, PD	Used for external MIPI IC control	1.8 V
58	RFFE_DATA ¹⁾	DIO, PD		1.8 V
65	RFFE_VIO_1V8 ¹⁾	PO	Power supply for antenna tuner	1.8 V. Maximum output current: 50 mA
61	ANTCTL1*	DO, PD	Antenna GPIO Control	1.8 V
63	ANTCTL2*	DO, PD		1.8 V

NOTE

¹⁾ If this function is required, please contact Quectel for more details.

4.8. Configuration Pins

The module provides four configuration pins, which are defined as below.

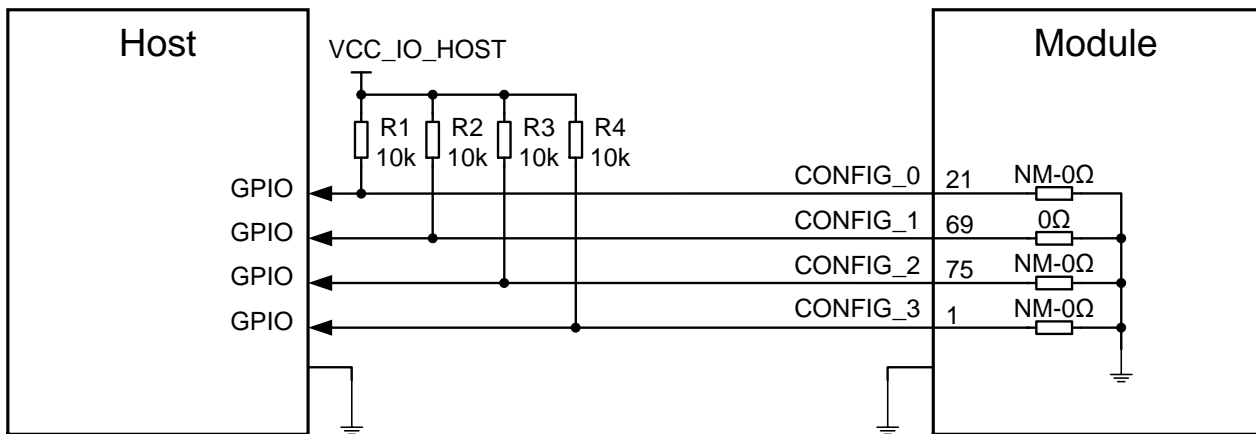
Table 28: Configuration Pins List of M.2 Specification

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	Quectel defined	2

Table 29: Configuration Pins of the Module

Pin No.	Pin Name	I/O	Description
21	CONFIG_0	DO	Not connected internally
69	CONFIG_1	DO	Connected to GND internally
75	CONFIG_2	DO	Not connected internally
1	CONFIG_3	DO	Not connected internally

The following figure shows a reference circuit of these four pins.



NOTE: The voltage level of VCC_IO_HOST depends on the host side and could be 1.8 V or 3.3 V.

Figure 27: Recommended Circuit of Configuration Pins

5 RF Characteristics

This chapter mainly describes RF characteristics of the module.

5.1. Cellular Antenna Interfaces

5.1.1. Pin Definition

The pin definition of antenna interfaces is shown below.

Table 30: RM500Q-AE&RM502Q-AE Pin Definition of Antenna Interfaces

Pin Name	I/O	Description	Comment
ANT0	AIO	Antenna 0 interface: 5G NR: MHB_TRX & n41 TRX1 ¹⁾ & n77/n78/n79_PRX MIMO; LTE: MHB_TRX & UHB_PRX MIMO ²⁾ WCDMA: MHB_TRX	1400–5000 MHz
ANT1	AIO	Antenna 1 interface: 5G NR: LB_TRX & MHB_DRX MIMO & n41_DRX1 ¹⁾ & n77/n78/n79_DRx MIMO LTE: LB_TRX & MHB_DRX MIMO & UHB_DRX MIMO ²⁾ & LAA PRX WCDMA: LB_TRX	600–6000 MHz
ANT2	AIO	Antenna 2 interface: 5G NR: LB_DRX & MHB_PRX MIMO & n41 TRX0 ¹⁾ & n77/n78/n79_TRX LTE: LB_DRX & MHB_PRX MIMO & UHB_TRX ²⁾ WCDMA: LB_DRX	600–5000 MHz
ANT3_ GNSSL1	AI	Antenna 3 interface: 5G NR: MHB_DRX MIMO & n41 DRX0 ¹⁾ & n77/n78/n79_DRX LTE: MHB_DRX & UHB_DRX ²⁾ & LAA DRX WCDMA: MHB_DRX GNSS: L1	1400–6000 MHz

NOTES

- ¹⁾ NR TRX1 = TX MIMO + PRX MIMO; NR DRX1 = DRX MIMO.
- ²⁾ UHB frequency range: 3400–3800 MHz.

5.1.2. Port Mapping

Table 31: RM500Q-AE & RM502Q-AE Antenna Mapping

Antenna	WCDMA	LTE	5G NR			LB (MHz)	MHB (MHz)	n77/n78 (MHz)	n79 (MHz)
			Refarmed	n41	n77/n78/ n79				
ANT0	MHB_TRX	MHB_TRX, UHB_PRX ¹⁾ MIMO	MHB_TRX, UHB_PRX ¹⁾ MIMO	TRX1 ²⁾	PRX MIMO	-	1452–2690	3300–4200	4400–5000
ANT1	LB_TRX	LB_TRX, MHB_DRX MIMO, UHB_PRX ¹⁾ MIMO, LAA PRX	LB_TRX, MHB_DRX MIMO, UHB_DRX ¹⁾ MIMO,	DRX1 ²⁾	DRX MIMO	617–960	1452–2690	3300–4200	4400–6000
ANT2	LB_DRX	LB_DRX, MHB_PRX MIMO, UHB_TRX ¹⁾	LB_DRX, MHB_PRX MIMO, UHB_TRX ¹⁾	TRX0 ²⁾	TRX	617–960	1452–2690	3300–4200	4400–5000
ANT3_ GNSSL1	MHB_DRX	MHB_DRX, UHB_DRX ¹⁾ , LAA_DRX	MHB_DRX, UHB_DRX ¹⁾ ,	DRX0 ²⁾	DRX	-	1452–2690	3300–4200	4400–6000

NOTES

- ¹⁾ UHB frequency range: 3400–3800 MHz.
- ²⁾ NR TRX1 = TX MIMO + PRX MIMO; NR DRX1 = DRX MIMO.

5.1.3. Operating Frequency

Table 32: RM500Q-AE&RM502Q-AE Operating Frequencies

Band Name	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
IMT (2100)	1920–1980	2110–2170	B1	–	B1	n1

PCS (1900)	1850–1910	1930–1990	B2	–	B2	n2
DCS (1800)	1710–1785	1805–1880	B3	–	B3	n3
AWS	1710–1755	2110–2155	B4	–	B4	–
Cell (850)	824–849	869–894	B5	–	B5	n5
JCELL (800)	830–840	875–885	–	–	B6	–
IMT-E (2600)	2500–2570	2620–2690	B7	–	–	n7
EGSM (950)	880–915	925–960	B8	–	B8	n8
700 lower A–C	699–716	729–746	B12(B17)	–	–	n12
700 upper C	777–787	746–756	B13	–	–	–
700 D	788–798	758–768	B14	–	–	–
B18	815–830	860–875	B18	–	–	–
B19	830–845	875–890	B19	–	B19	–
EU800	832–862	791–821	B20	–	–	n20
PCS + G	1850–1915	1930–1995	B25	–	–	n25
B26	814–849	859–894	B26	–	–	–
700 APAC	703–748	758–803	B28	–	–	n28
FLO	–	717–728	B29	–	–	–
WCS	2305–2315	2350–2360	B30	–	–	–
L-band	–	1452–1496	B32	–	–	–
B34	2010–2025	2010–2025	–	B34	–	–
B38	2570–2620	2570–2620	–	B38	–	n38
B39	1880–1920	1880–1920	–	B39	–	–
B40	2300–2400	2300–2400	–	B40	–	n40
B41/B41-XGP	2496–2690	2496–2690	–	B41	–	n41
B42	3400–3600	3400–3600	–	B42	–	–
B43	3600–3800	3600–3800	–	B43	–	–
B46	5150–5925	5150–5925	–	B46	–	–
B48	3550–3700	3550–3700	–	B48	–	n48*

B66	1710–1780	2110–2200	B66	–	–	n66
B71	663–698	617–652	B71	–	–	n71
n77	3300–4200	3300–4200	–	–	–	n77
n78	3300–3800	3300–3800	–	–	–	n78
n79	4400–5000	4400–5000	–	–	–	n79

5.1.4. Receiving Sensitivity

The following tables show conducted receiving sensitivity of RM500Q-AE and RM502Q-AE.

Table 33: RM500Q-AE&RM502Q-AE Conducted Receiving Sensitivity (Unit: dBm)

Mode	Frequency	Primary	Diversity	SIMO ¹⁾	3GPP (SIMO)
WCDMA	WCDMA B1	-109.5	-110.3	-110.5	-106.7 dBm
	WCDMA B2	-109.5	-110.6	-110.5	-104.7 dBm
	WCDMA B3	-109.5	-110.4	-110.5	-103.7 dBm
	WCDMA B4	-109	-110.1	-110	-106.7 dBm
	WCDMA B5	-110.5	-112	-112	-104.7 dBm
	WCDMA B8	-109.5	-112	-111.5	-103.7 dBm
	WCDMA B19	-111	-112	-112	-104.7 dBm
LTE	LTE-FDD B1 (10 MHz)	-98.0	-99.2	-101.0	-96.3 dBm
	LTE-FDD B2 (10 MHz)	-97.0	-99.2	-101.5	-94.3 dBm
	LTE-FDD B3 (10 MHz)	-97.0	-98.7	-101.2	-93.3 dBm
	LTE-FDD B4 (10 MHz)	-97.5	-98.7	-101.0	-96.3 dBm
	LTE-FDD B5 (10 MHz)	-99.0	-101.0	-102.5	-94.3 dBm
	LTE-FDD B7 (10 MHz)	-97.0	-98.5	-100.5	-94.3 dBm
	LTE-FDD B8 (10 MHz)	-98.5	-100.5	-102.2	-93.3 dBm
LTE-FDD B12(B17) (10 MHz)	-99.5	-101.5	-102.5	-93.3 dBm	

	LTE-FDD B13 (10 MHz)	-100.0	-101.5	-102.5	-93.3 dBm
	LTE-FDD B14 (10 MHz)	-100.0	-101.2	-102.5	-93.3 dBm
	LTE-FDD B18 (10 MHz)	-98.7	-101.0	-102.0	-96.3 dBm
	LTE-FDD B19 (10 MHz)	-99.0	-101.2	-102.1	-96.3 dBm
	LTE-FDD B20 (10 MHz)	-100.0	-101.5	-102.5	-93.3 dBm
	LTE-FDD B25 (10 MHz)	-97.0	-99.3	-101.0	-92.8 dBm
	LTE-FDD B26 (10 MHz)	-99.0	-101.3	-102.2	-93.8 dBm
	LTE-FDD B28 (10 MHz)	-100.0	-101.5	-102.5	-94.8 dBm
	LTE-FDD B30 (10 MHz)	-96.0	-98.0	-100.0	-95.3 dBm
	LTE-FDD B32 (10 MHz)	TBD	TBD	TBD	-95.3 dBm
	LTE-TDD B34 (10 MHz)	-97.0	-98.5	-100.5	-96.3 dBm
	LTE-TDD B38 (10 MHz)	-97.0	-98.3	-100.5	-96.3 dBm
	LTE-TDD B39 (10 MHz)	-97.0	-97.0	-100.0	-96.3 dBm
	LTE-TDD B40 (10 MHz)	-96.0	-97.0	-100.0	-96.3 dBm
	LTE-TDD B41 (10 MHz)	-96.8	-98.3	-100.5	-94.3 dBm
	LTE-TDD B42 (10 MHz)	-96.8	-99.0	-100.5	-95 dBm
	LTE-TDD B43 (10 MHz)	-96.8	-99.0	-100.5	-95 dBm
	LTE-TDD B48 (10 MHz)	-96.8	-96.8	-99.0	-95 dBm
	LTE-FDD B66 (10 MHz)	-96.8	-98.3	-100.2	-96.5 dBm
	LTE-FDD B71 (10 MHz)	-100.0	-101.0	-102.5	-94.2 dBm
5G NR	5G NR-FDD n1 (20 MHz) (SCS: 15 kHz)	-94.5	-95.5	-97.5	-94.0 dBm
	5G NR-FDD n2 (20 MHz) (SCS: 15 kHz)	-94.5	-95.5	-97.5	-92.0 dBm
	5G NR-FDD n3 (20 MHz) (SCS: 15 kHz)	-93.5	-95.5	-97.0	-91.0 dBm
	5G NR-FDD n5 (20 MHz) (SCS: 15 kHz)	-95.5	-97.0	-99.5	-91 dBm

5G NR-FDD n7 (20 MHz) (SCS: 15 kHz)	-93.5	-94	-96.5	-92.0 dBm
5G NR-FDD n8 (20 MHz) (SCS: 15 kHz)	-95.0	-97.0	-98.5	-90.0dBm
5G NR-FDD n12 (15 MHz) (SCS: 15 kHz)	-95.0	-98.0	-99.5	-84.0 dBm
5G NR-FDD n20 (20 MHz) (SCS: 15 kHz)	-95.0	-97.0	-99.0	-90.0 dBm
5G NR-FDD n25 (20 MHz) (SCS: 15 kHz)	-94.5	-95.0	-97.5	-90.5 dBm
5G NR-FDD n28 (20 MHz) (SCS: 15 kHz)	-95.0	-97.0	-99.0	-91.0 dBm
5G NR-TDD n38 (20 MHz) (SCS: 30 kHz)	-94.0	-95.0	-97.0	-94.0 dBm
5G NR-TDD n40 (20 MHz) (SCS: 30 kHz)	-93.5	-93.5	-95.5	-94.0 dBm
5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-85.0	-87.0	-88.5	-84.7 dBm
5G NR-FDD n48 (20 MHz) (SCS: 30 kHz)	-94.0	-95.5	-97	-93.0 dBm
5G NR-FDD n66 (40 MHz) (SCS: 15 kHz)	-91.5	-92.0	-94.5	-90.1 dBm
5G NR-FDD n71 (20 MHz) (SCS: 15 kHz)	-95.0	-97.5	-99.5	-86.0 dBm
5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	-86.0	-87.0	-89.0	-85.1 dBm
5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-86.0	-87.5	-89.0	-85.6 dBm
5G NR-TDD n79 (100 MHz) (SCS: 30 kHz)	-86.0	-86.5	-89.5	-85.6 dBm

NOTE

¹⁾ SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which improves Rx performance.

5.1.5. Output Power

The following table shows the RF output power of the module.

Table 34: Cellular Output Power

Mode	Frequency	Max.	Min.
WCDMA	WCDMA bands	24 dBm +1/-3 dB (Class 3)	< -50 dBm
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	LTE HPUE bands (B38/B40/B41/B42/B43)	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm (BW: 5–20 MHz) ¹⁾
	5G NR HUPE bands (n41/n77/n78/n79)	26 dBm +2/-3 dB (Class 2)	< -40 dBm (BW: 5–20 MHz) ¹⁾

NOTE

¹⁾ For 5G NR TDD bands, the normative reference for this requirement is *TS 38.101-1 clause 6.3.1*.

5.2. GNSS Antenna Interface

5.2.1. General Description

The module includes a fully integrated global navigation satellite system solution (GPS, GLONASS, BeiDou/COMPASS, and Galileo).

The module supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the module GNSS engine is switched off. It must be switched on via AT command. For more details about GNSS engine technology and configurations, see **document [5]**.

5.2.2. GNSS Frequency

Table 35: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42 ±1.023 (L1)	MHz
Galileo	1575.42 ±2.046 (E1)	MHz
QZSS	1575.42 (L1)	MHz
GLONASS	1597.5–1605.8	MHz
BeiDou/COMPASS	1561.098 ±2.046	MHz

NOTES

1. Keep the characteristic impedance for the trace of GNSS antenna (ANT3_GNSSL1) to 50 Ω.
2. Place the π-type matching components as close to the antenna as possible.
3. Keep the digital circuits, such as that of (U)SIM card, USB interface, camera module, display connector and SD card, away from the antenna traces.
4. Keep 75 dB isolation between each antenna traces.
5. Keep 15 dB isolation between each antenna to improve the receiving sensitivity. and 20 dB isolation between 5G NR UL MIMO TRX0 and TRX1 antennas.

5.2.3. GNSS Performance

The following table shows GNSS performance of the module.

Table 36: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-148	dBm
	Reacquisition	Autonomous	-159	dBm
	Tracking	Autonomous	-159	dBm
TTFF (GNSS)	Cold start	Autonomous	33.99	s
	@ open sky	XTRA enabled	13.56	s

	Warm start @ open sky	Autonomous	22.55	s
		XTRA enabled	2.02	s
	Hot start @ open sky	Autonomous	1.33	s
		XTRA enabled	1.47	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	1.8	m

NOTES

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after the loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.3. Antenna Connectors

5.3.1. Antenna Connector Location

RM500Q-AE and RM502Q-AE have four antenna connectors each: ANT0, ANT1, ANT2 and ANT3_GNSS1, which are shown as below.



Figure 28: RM500Q-AE Antenna Connectors



Figure 29: RM502Q-AE Antenna Connectors

5.3.2. Antenna Connector Size

RM500Q-AE and RM502Q-AE are mounted with standard 2 mm × 2 mm receptacle antenna connectors for convenient antenna connection. The antenna connector's PN is IPEX 20579-001E, and the connector dimensions are illustrated as below:

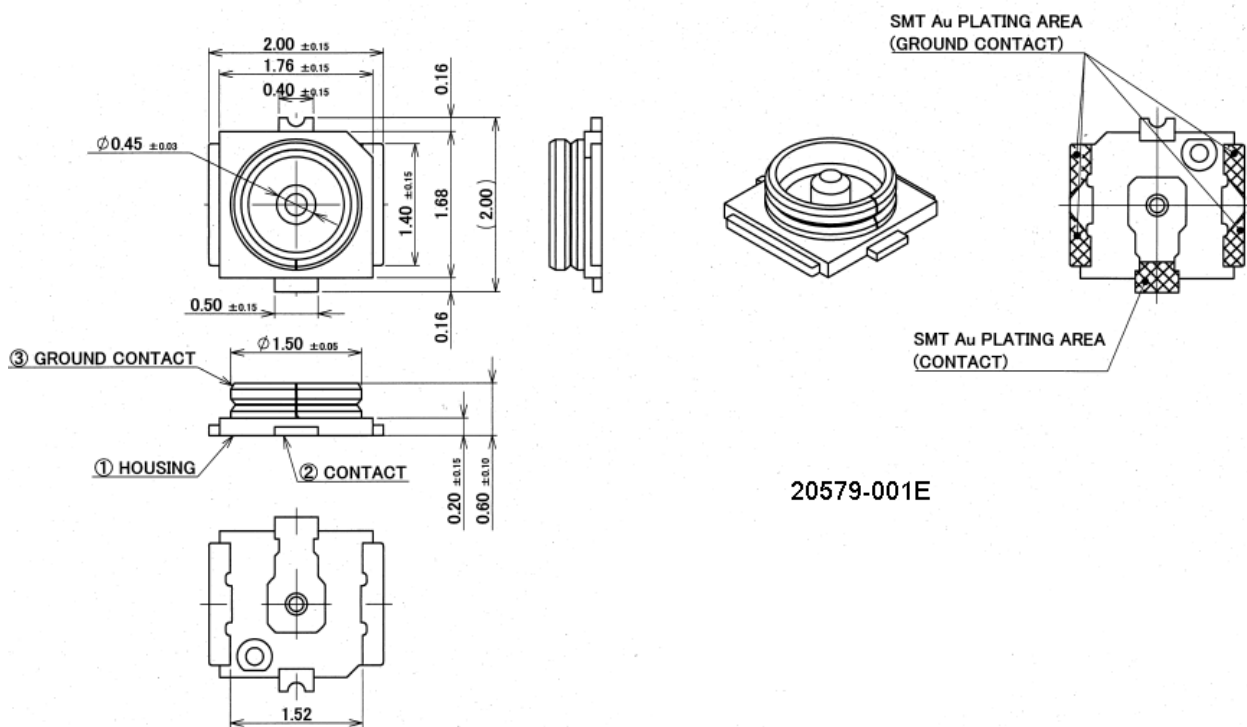


Figure 30: RF Connector Dimensions (Unit: mm)

Table 37: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max 1.3 (DC–3 GHz) Max 1.4 (3–6 GHz)

5.3.3. Antenna Connector Installation

The receptacle RF connector used in conjunction with the module will accept two types of mating plugs that will meet a maximum height of 1.2 mm using a Ø 0.81 mm coaxial cable or a maximum height of 1.45 mm utilizing a Ø 1.13 mm coaxial cable.

The following figure shows the specifications of mating plugs using Ø 0.81 mm coaxial cables.

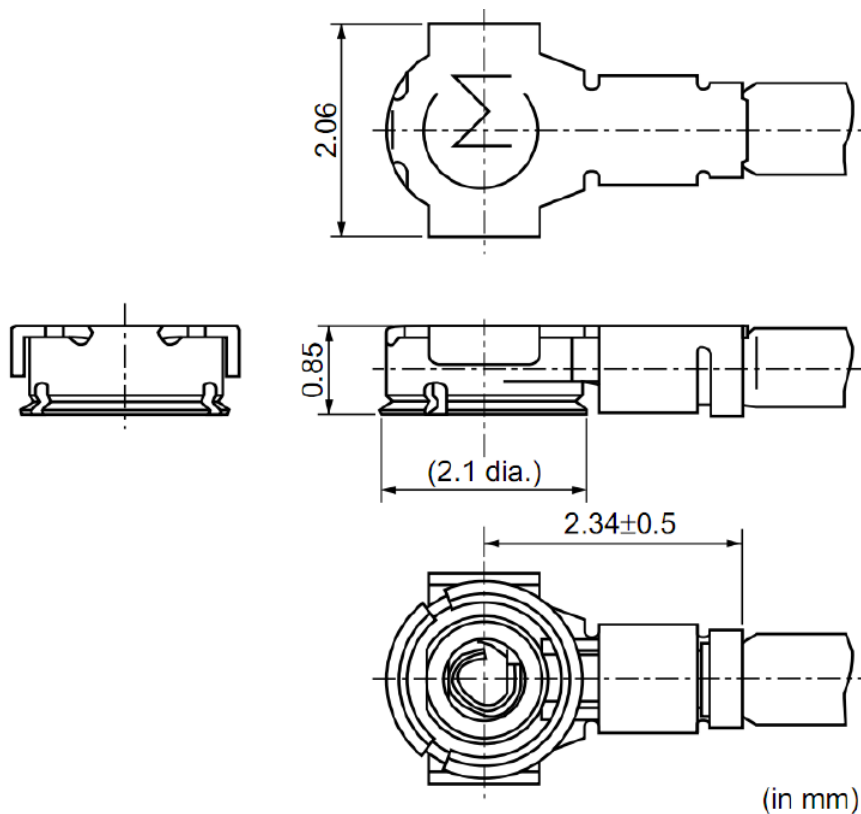


Figure 31: Specifications of Mating Plugs Using Ø 0.81 mm Coaxial Cables

The following figure illustrates the connection between the receptacle RF connector on the module and the mating plug using a \varnothing 0.81 mm coaxial cable.

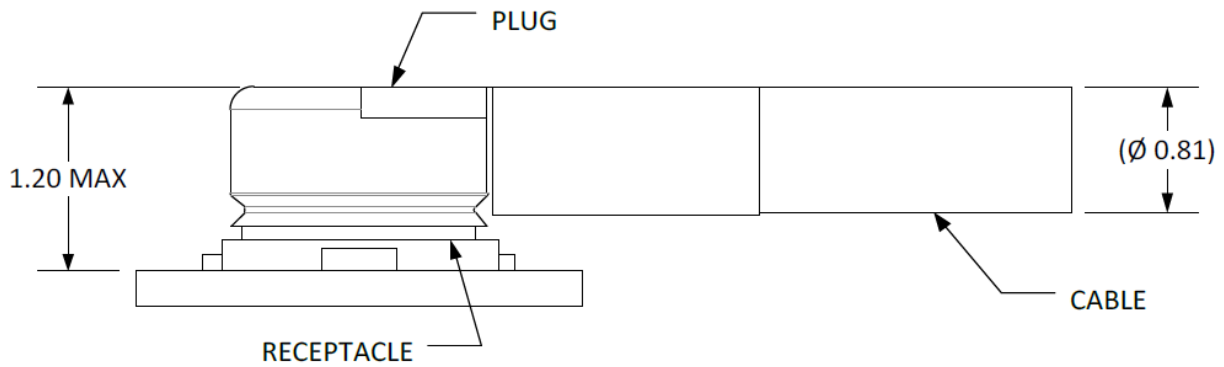


Figure 32: Connection Between RF Connector and Mating Plug Using \varnothing 0.81 mm Coaxial Cable

The following figure illustrates the connection between the receptacle RF connector on the module and the mating plug using a \varnothing 1.13 mm coaxial cable.

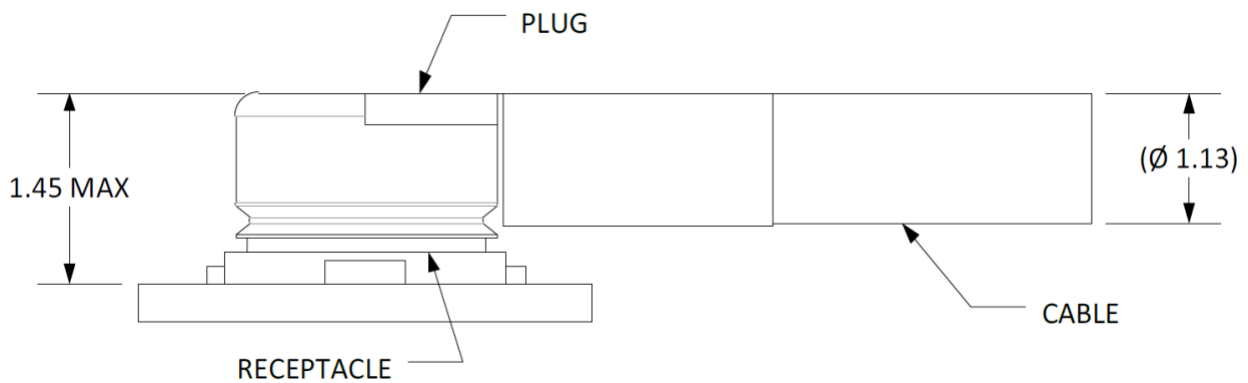


Figure 33: Connection Between RF Connector and Mating Plug Using \varnothing 1.13 mm Coaxial Cable

5.3.4. Recommended RF Connector Installation

5.3.4.1. Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

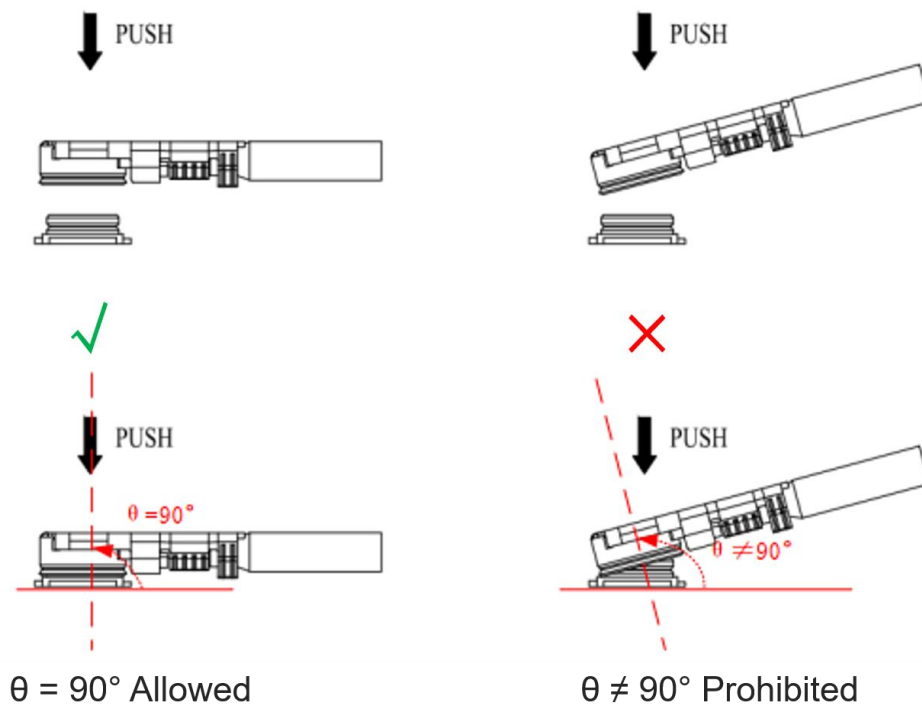


Figure 34: Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

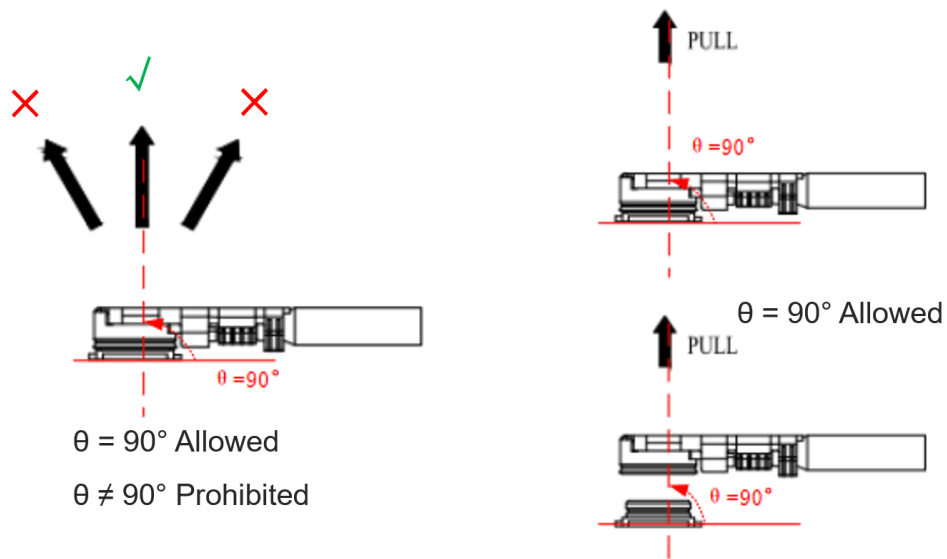


Figure 35: Pull out a Coaxial Cable Plug

5.3.4.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

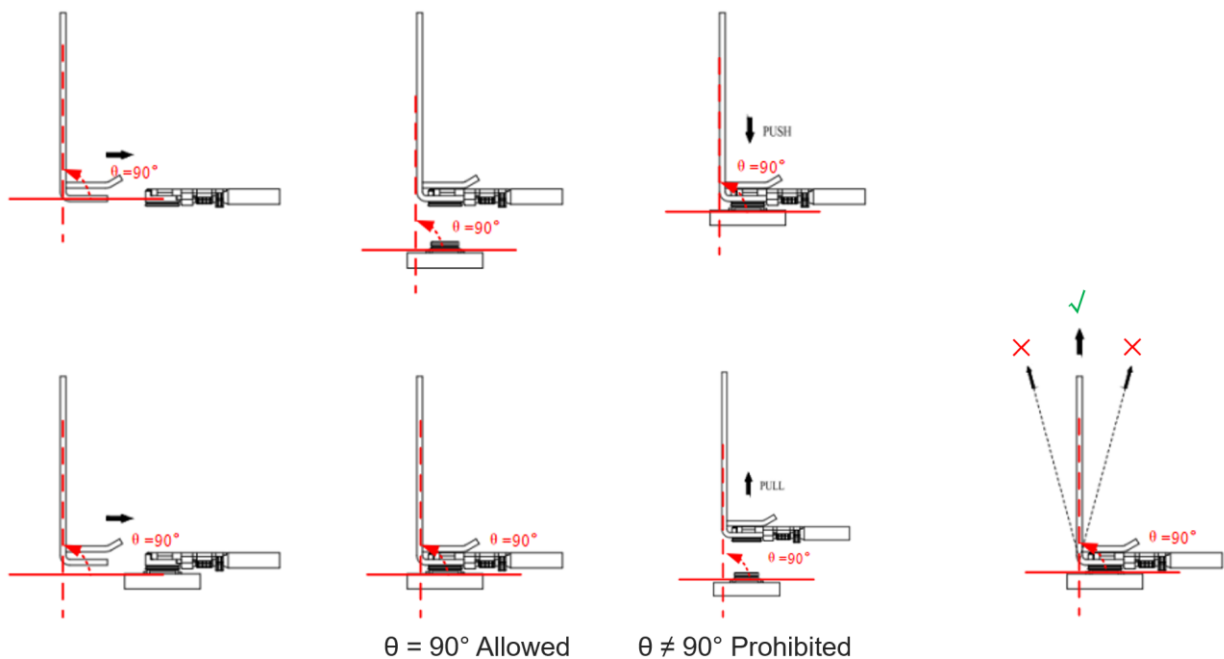


Figure 36: Install the Coaxial Cable Plug with A Jig

5.3.5. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit <https://www.i-pex.com>.

5.4. Antenna Requirements

The following table shows the requirements on WCDMA, LTE, 5G NR antenna and GNSS antennas.

Table 38: Antenna Requirements

Type	Requirements
WCDMA/LTE/5G NR	<ul style="list-style-type: none"> ● VSWR: ≤ 3 ● Efficiency: $> 30\%$ ● Input Impedance: $50\ \Omega$ ● Cable insertion loss: <ul style="list-style-type: none"> $< 1\ \text{dB}$ WCDMA B5/B6/B8/B19 LTE B5/B8/B12(B17)/B13/B14/B18/B19/B20/B26/B28/B29/B71 5G NR n5/n8/n12/n20/n28/n71 $< 1.5\ \text{dB}$ WCDMA B1/B2/B3/B4 LTE B1/B2/B3/B4/B25/B32/B34/B39/B66 5G NR n1/n2/n3/n25/n66 $< 2\ \text{dB}$ LTE B7/B30/B38/B40/B41/B42/B43/B46/B48 5G NR n7/n38/n40/n41/n48/n77/n78/n79
GNSS	<ul style="list-style-type: none"> ● Frequency range: 1559–1606 MHz ● Polarization: RHCP or linear ● VSWR: < 2 (Typ.) ● Passive antenna gain: $> 0\ \text{dBi}$

6 Electrical Characteristics and Reliability

6.1. Power Supply Requirements

The typical input voltage of the module is 3.7 V, the following table shows the power supply requirements of the module.

Table 39: Power Supply Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	3.135	3.7	4.4	V
Voltage Ripple		–	30	100	mV
Voltage Drop		–	–	165	mV

6.2. Current Consumption

Table 40: RM500Q-AE&RM502Q-AE Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	82	μA
	AT+CFUN=0 (USB Suspend)	5.11	mA
Sleep state	WCDMA @ DRX = 0.64s, USB Suspend	5.389	mA
	LTE-FDD @ DRX = 0.64s, USB Suspend	5.689	mA

	LTE-TDD @ DRX = 0.64s, USB Suspend	5.803	mA
Idle state	WCDMA @ Paging Frame = 64	31.06	mA
	WCDMA @ Paging Frame = 64, USB Active	52.42	mA
	LTE-FDD @ DRX = 0.64 s	32.93	mA
	LTE-FDD @ DRX = 0.64 s, USB Active	54.77	mA
	LTE-TDD @ DRX = 0.64 s	32.85	mA
	LTE-TDD @ DRX = 0.64 s, USB Active	54.56	mA
	WCDMA (GNSS OFF)	WCDMA B1 HSDPA CH10700 @ 23 dBm	595
WCDMA B1 HSUPA CH10700 @ 23 dBm		540	mA
WCDMA B2 HSDPA CH9800 @ 23 dBm		650	mA
WCDMA B2 HSUPA CH9800 @ 23 dBm		615	mA
WCDMA B3 HSDPA CH1338 @ 23 dBm		570	mA
WCDMA B3 HSUPA CH1338 @ 23 dBm		545	mA
WCDMA B4 HSDPA CH1638 @ 23 dBm		520	mA
WCDMA B4 HSUPA CH1638 @ 23 dBm		505	mA
WCDMA B5 HSDPA CH4407 @ 23 dBm		430	mA
WCDMA B5 HSUPA CH4407 @ 23 dBm		405	mA
WCDMA B6 HSDPA CH4400 @ 23 dBm		420	mA
WCDMA B6 HSUPA CH4400 @ 23 dBm		415	mA
WCDMA B8 HSDPA CH3012 @ 23 dBm		430	mA
WCDMA B8 HSUPA CH3012 @ 23 dBm		420	mA
WCDMA B19 HSDPA CH738 @ 23 dBm		420	mA
WCDMA B19 HSUPA CH738 @ 23 dBm		420	mA
LTE (GNSS OFF)	LTE-FDD B1 CH300 @ 23 dBm	795	mA
	LTE-FDD B2 CH900 @ 23 dBm	715	mA

LTE-FDD B3 CH1575 @ 23 dBm	770	mA
LTE-FDD B4 CH2175 @ 23 dBm	680	mA
LTE-FDD B5 CH2525 @ 23 dBm	485	mA
LTE-FDD B7 CH3100 @ 23 dBm	745	mA
LTE-FDD B8 CH3625 @ 23 dBm	495	mA
LTE-FDD B12(B17) CH5095 @ 23 dBm	485	mA
LTE-FDD B13 CH5230 @ 23 dBm	560	mA
LTE-FDD B14 CH5330 @ 23 dBm	480	mA
LTE-FDD B18 CH5925 @ 23 dBm	515	mA
LTE-FDD B19 CH6075 @ 23 dBm	490	mA
LTE-FDD B20 CH6300 @ 23 dBm	480	mA
LTE-FDD B25 CH8365 @ 23 dBm	695	mA
LTE-FDD B26 CH8865 @ 23 dBm	470	mA
LTE-FDD B28 CH9435 @ 23 dBm	490	mA
LTE-FDD B30 CH9820 @ 23 dBm	860	mA
LTE-TDD B34 CH36275 @ 23 dBm	440	mA
LTE-TDD B38 CH38000 @ 23 dBm	420	mA
LTE-TDD B39 CH38450 @ 23 dBm	380	mA
LTE-TDD B40 CH39150 @ 23 dBm	345	mA
LTE-TDD B41 CH40620 @ 23 dBm	440	mA
LTE-TDD B42 CH42590 @ 23 dBm	460	mA
LTE-TDD B43 CH44590 @ 23 dBm	500	mA
LTE-TDD B48 CH55990 @ 23 dBm	480	mA
LTE-FDD B66 CH66886 @ 23 dBm	765	mA
LTE-FDD B71 CH68761 @ 23 dBm	460	mA

5G NR (GNSS OFF)	5G NR-TDD n41 CH501204 @ 26 dBm	500	mA
	5G NR-TDD n41 CH518598 @ 26 dBm	500	mA
	5G NR-TDD n41 CH535998 @ 26 dBm	515	mA
	5G NR-TDD n77 CH620668 @ 26 dBm	500	mA
	5G NR-TDD n77 CH650000 @ 26 dBm	500	mA
	5G NR-TDD n77 CH679332 @ 26 dBm	520	mA
	5G NR-TDD n78 CH620668 @ 26 dBm	500	mA
	5G NR-TDD n78 CH636666 @ 26 dBm	530	mA
	5G NR-TDD n78 CH652666 @ 26 dBm	500	mA
	5G NR-TDD n79 CH695090 @ 26 dBm	550	mA
	5G NR-TDD n79 CH713522 @ 26 dBm	550	mA
	5G NR-TDD n79 CH731976 @ 26 dBm	530	mA
	5G NR-FDD n1 CH423000 @ 23 dBm	950	mA
	5G NR-FDD n1 CH428000 @ 23 dBm	880	mA
	5G NR-FDD n1 CH433000 @ 23 dBm	930	mA
	5G NR-FDD n2 CH387000 @ 23 dBm	610	mA
	5G NR-FDD n2 CH392000 @ 23 dBm	740	mA
	5G NR-FDD n2 CH397000 @ 23 dBm	610	mA
	5G NR-FDD n3 CH362000 @ 23 dBm	780	mA
	5G NR-FDD n3 CH368500 @ 23 dBm	780	mA
	5G NR-FDD n3 CH375000 @ 23 dBm	870	mA
	5G NR-FDD n5 CH174800 @ 23 dBm	515	mA
	5G NR-FDD n5 CH176300 @ 23 dBm	510	mA
	5G NR-FDD n5 CH177800 @ 23 dBm	510	mA
	5G NR-FDD n7 CH525000 @ 23 dBm	690	mA

5G NR-FDD n7 CH531000 @ 23 dBm	690	mA
5G NR-FDD n7 CH537000 @ 23 dBm	670	mA
5G NR-FDD n8 CH186000 @ 23 dBm	550	mA
5G NR-FDD n8 CH188500 @ 23 dBm	520	mA
5G NR-FDD n8 CH191000 @ 23 dBm	520	mA
5G NR-FDD n12 CH146800 @ 23 dBm	480	mA
5G NR-FDD n12 CH147500 @ 23 dBm	480	mA
5G NR-FDD n12 CH148200 @ 23 dBm	480	mA
5G NR-FDD n20 CH159200 @ 23 dBm	480	mA
5G NR-FDD n20 CH161200 @ 23 dBm	480	mA
5G NR-FDD n20 CH163200 @ 23 dBm	490	mA
5G NR-FDD n25 CH387000 @ 23 dBm	640	mA
5G NR-FDD n25 CH392500 @ 23 dBm	750	mA
5G NR-FDD n25 CH398000 @ 23 dBm	680	mA
5G NR-FDD n28 CH152600 @ 23 dBm	550	mA
5G NR-FDD n28 CH156100 @ 23 dBm	560	mA
5G NR-FDD n28 CH159600 @ 23 dBm	530	mA
5G NR-TDD n38 CH515000 @ 23 dBm	310	mA
5G NR-TDD n38 CH519000 @ 23 dBm	310	mA
5G NR-TDD n38 CH523000 @ 23 dBm	310	mA
5G NR-TDD n40 CH461000 @ 23 dBm	580	mA
5G NR-TDD n40 CH470000 @ 23 dBm	580	mA
5G NR-TDD n40 CH479000 @ 23 dBm	580	mA
5G NR-TDD n48 CH637000 @ 23 dBm	420	mA
5G NR-TDD n48 CH641667 @ 23 dBm	420	mA

	5G NR-TDD n48 CH646333 @ 23 dBm	410	mA
	5G NR-FDD n66 CH423000 @ 23 dBm	790	mA
	5G NR-FDD n66 CH429000 @ 23 dBm	880	mA
	5G NR-FDD n66 CH435000 @ 23 dBm	850	mA
	5G NR-FDD n71 CH124400 @ 23 dBm	500	mA
	5G NR-FDD n71 CH126900 @ 23 dBm	480	mA
	5G NR-FDD n71 CH129400 @ 23 dBm	490	mA
WCDMA data	WCDMA B1 CH10700 @ 23 dBm	670	mA
	WCDMA B2 CH9800 @ 23 dBm	730	mA
	WCDMA B3 CH1338 @ 23 dBm	650	mA
	WCDMA B4 CH1638 @ 23 dBm	600	mA
	WCDMA B5 CH4408 @ 23 dBm	460	mA
	WCDMA B6 CH4175 @ 23 dBm	460	mA
	WCDMA B8 CH3012 @ 23 dBm	475	mA
	WCDMA B19 CH338 @ 23 dBm	460	mA

6.3. Digital I/O Characteristic

Table 41: Logic Levels of Digital I/O (1.8 V)

Parameter	Description	Min.	Max.	Unit
V _{IH}	Input high voltage	1.65	2.1	V
V _{IL}	Input low voltage	-0.3	0.54	V
V _{OH}	Output high voltage	1.3	1.8	V
V _{OL}	Output low voltage	0	0.4	V

Table 42: (U)SIM 1.8V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.65	1.95	V
V _{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V _{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V _{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V _{OL}	Output low voltage	0	0.4	V

Table 43: (U)SIM 3.0V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V _{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V _{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V _{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V _{OL}	Output low voltage	0	0.4	V

6.4. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

Table 44: Electrostatic Discharge Characteristics (Temperature: 25 °C, Humidity: 40 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VCC, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV

Other Interfaces

±0.5

±1

kV

6.5. Thermal Dissipation

RM500Q-AE and RM502Q-AE are designed to work in an extended temperature range. To achieve a maximum performance while working under extended temperatures or extreme conditions (such as with maximum power or data rate) for a long time, it is strongly recommended to add a thermal pad or other thermally conductive compounds between the module and the main PCB for thermal dissipation.

The thermal dissipation area on the bottom (i.e. the area for adding thermal pad) is shown as below, and thermal paste are also added on the BB, MCP, PMU, WTR, PA-1, PA-2 chips inside the module. The dimensions are measured in mm.

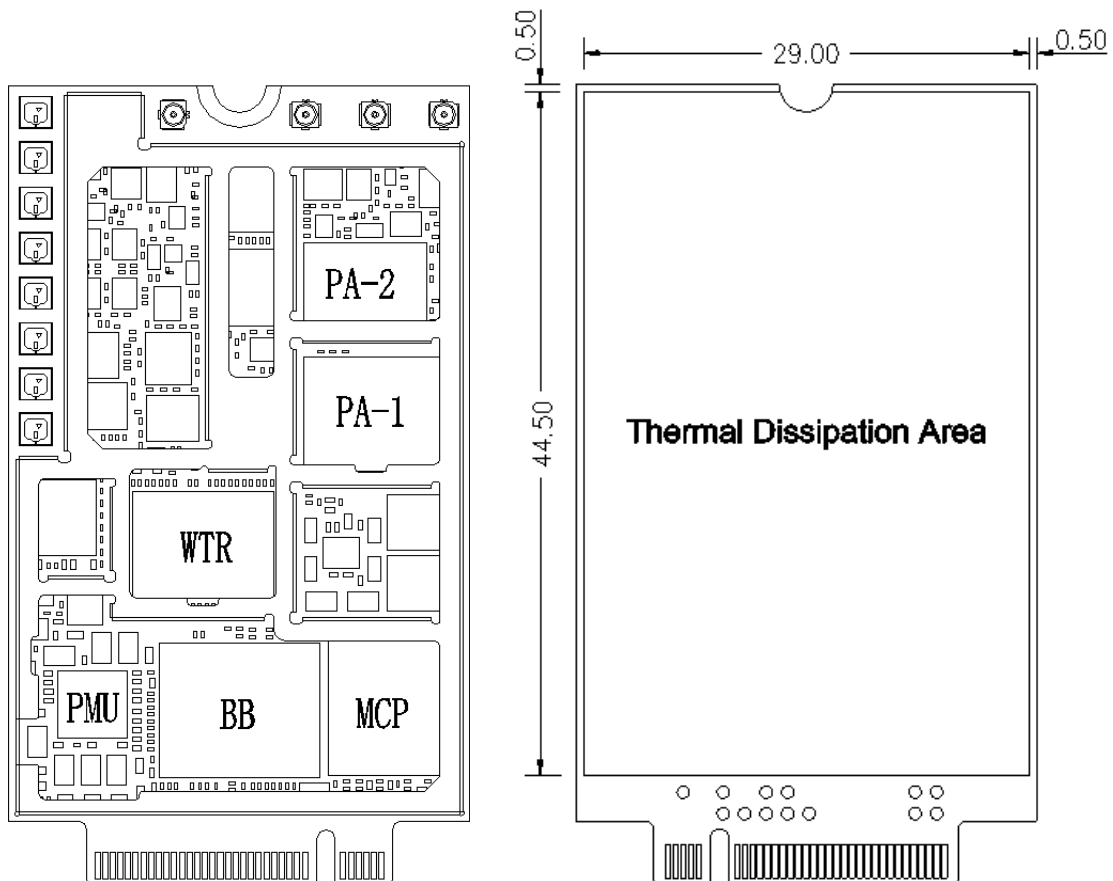


Figure 37: Thermal Dissipation Area Inside and on Bottom Side of the Module

Other measures to enhance heat dissipation performance are listed as follows:

- Add as many ground vias as possible on the PCB.
- Maximize airflow over/around the module.
- Place the module away from other heating sources.
- Module mounting holes must be used to attach (ground) the device to the main PCB ground.
- It is NOT recommended to apply solder mask on the main PCB where the module's thermal dissipation area is located.
- Select appropriate material, thickness and surface for the outer housing of the application device that integrates the module (i.e. the mechanical enclosure) to enhance thermal dissipation ability. Customers may also need active cooling to dissipate heat of the module.
- If possible, add a heatsink on the top of the module. A thermal pad should be used between the heatsink and the module, and the heatsink should be designed with as many fins as possible to increase heat dissipation area.

NOTE

If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

6.6. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 45: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
VCC	-0.3		4.7	V
Voltage at Digital Pins	-0.3		2.3	V

6.7. Operating and Storage Temperatures

Table 46: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range ¹⁾	-30	+25	+70	°C
Extended Temperature Range ²⁾	-40	-	+85	°C
Storage temperature Range	-40	-	+90	°C

NOTES

- ¹⁾ To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module meets 3GPP specifications.
- ²⁾ To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice*, SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out} , may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

7 Mechanical Dimensions and Packaging

This chapter mainly describes mechanical dimensions and packaging specifications of RM500Q-AE and RM502Q-AE. All dimensions are measured in mm, and the tolerances are ± 0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions of the Module

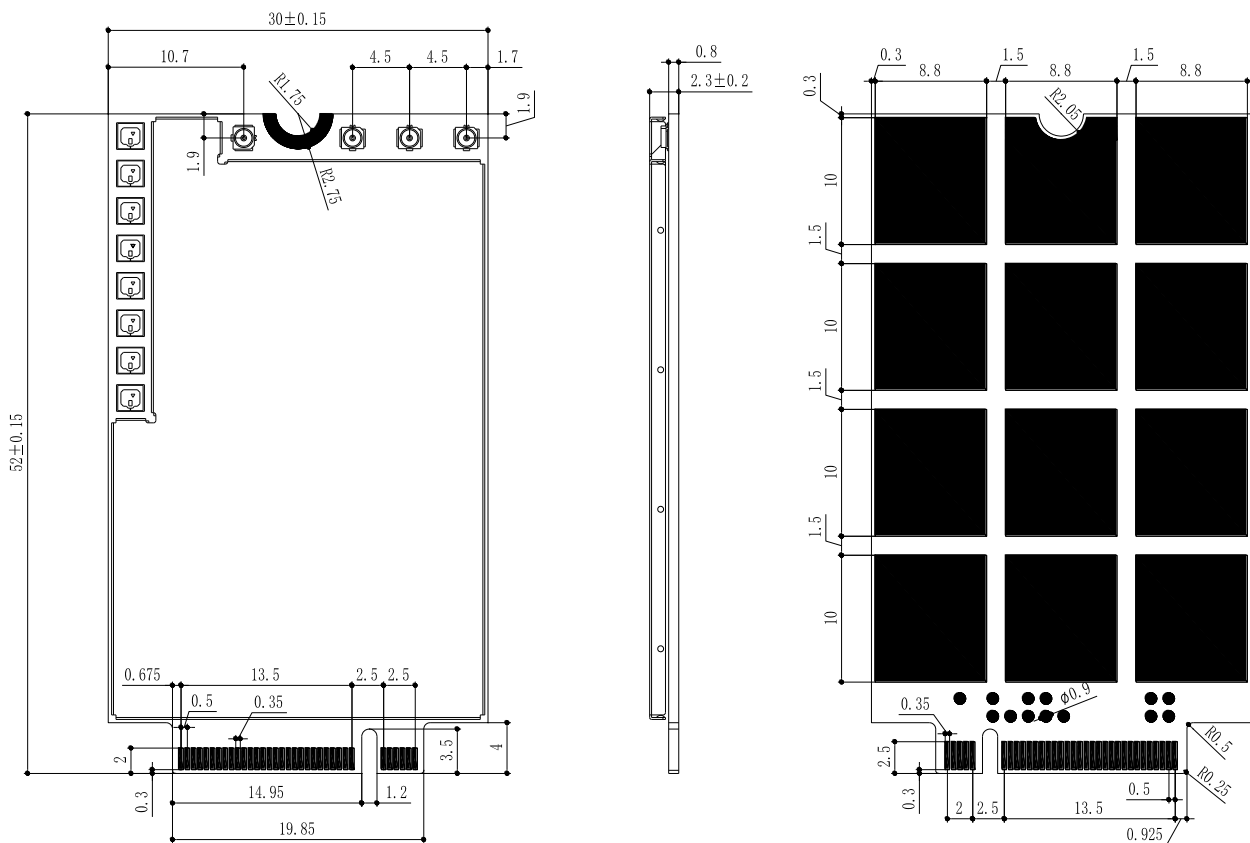


Figure 38: Mechanical Dimensions of the Module (Unit: mm)

7.2. Top and Bottom Views of the Module

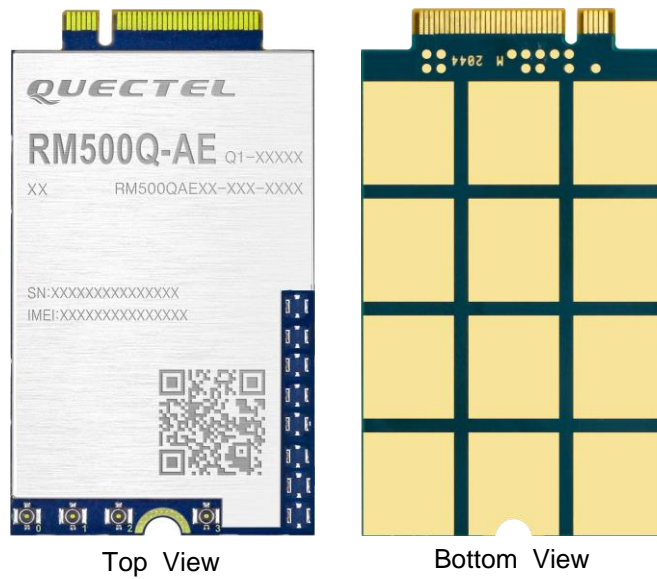


Figure 39: RM500Q-AE Top View and Bottom View

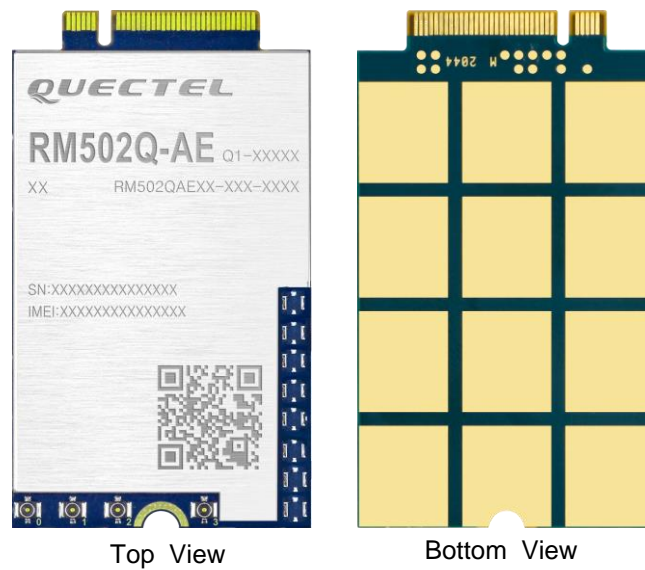


Figure 40: RM502Q-AE Top View and Bottom View

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7.3. M.2 Connector

The module adopts a standard PCI Express M.2 connector which complies with the directives and standards listed in the PCI Express M.2 Specification.

7.4. Packaging

The modules are packaged in trays. The following figure shows the tray size.

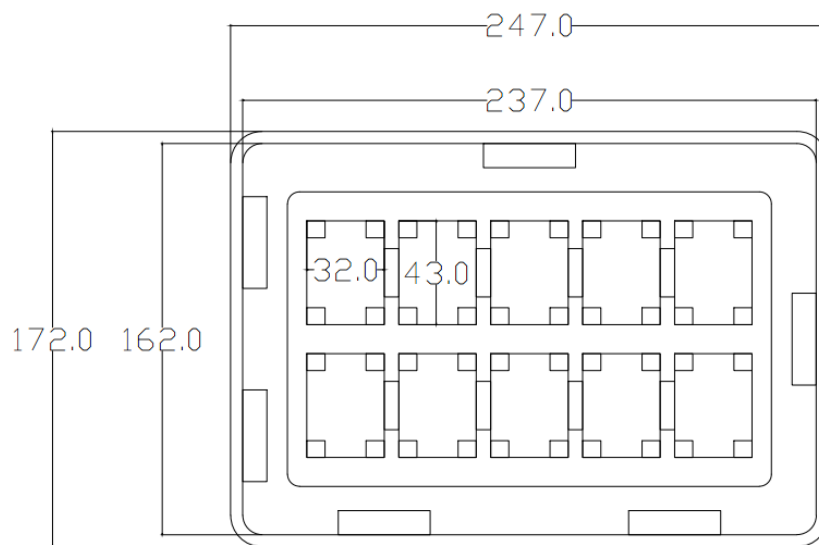


Figure 41: Tray Size (Unit: mm)

Each tray contains 10 modules. The smallest package contains 100 modules. Tray packaging procedures are as below.

1. Use 10 trays to package 100 modules at a time (tray size: 247 mm × 172 mm).
2. Place an empty tray on the top of the 10-tray stack.
3. Fix the stack with masking tape in “#” shape as shown in the following figure.
4. Pack the stack with conductive bag, and then fix the bag with masking tape.
5. Place the list of IMEI No. into a small carton.
6. Seal the carton and then label the seal with sealing sticker (small carton size: 250 mm × 175 mm × 128 mm).



Figure 42: Tray Packaging Procedure

8 Appendix References

Table 47: Related Documents

SN.	Document Name	Description
[1]	Quectel_RM50xQ-AE_CA&EN-DC_Features	CA and EN-DC features of RM500Q-AE and RM502Q-AE modules.
[2]	Quectel_PCIe_Card_EVB_User_Guide	PCIe card EVB user guide.
[3]	Quectel_RG50xQ&RM5xxQ_Series_AT_Commands_Manual	The AT command manual for RG50xQ series and RM5xxQ series.
[4]	Quectel_RM500Q_Series+IPQ8074A_Reference Design	RM500Q+IPQ8074A reference design
[5]	Quectel_RG50xQ&RM5xxQ_Series_GNSS_Application_Note	The GNSS application note for RG50xQ series and RM5xxQ series.

Table 48: Terms and Abbreviations

Abbreviation	Description
BIOS	Basic Input Output System
bps	Bit Per Second
BW	Bandwidth
CHAP	Challenge-Handshake Authentication Protocol
COEX	Coexistence
CPE	Customer Premise Equipment
CSQ	Cellular Signal Quality
DC-DC	Direct Current to Direct Current
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink

DPR	Dynamic Power Reduction
DRX	Discontinuous Reception (Chapter 3.1.1, Chapter 6.2) Diversity Reception (Chapter 5)
ESD	Electrostatic Discharge
EP	EndPoint
ET	Envelope Tracking
FDD	Frequency Division Duplexing
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
kbps	Kilo Bits Per Second
LAA	License Assisted Access
LED	Light Emitting Diode
LTE	Long Term Evolution
Mbps	Mega Bits Per Second
ME	Mobile Equipment
MIMO	Multiple-Input Multiple-Output
MLCC	Multilayer Ceramic Chip Capacitor
MO	Mobile Originated
MSB	Most Significant Bit
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board

PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
RC	Root Complex
RF	Radio Frequency
RFFE	RF Front-End
Rx	Receive
SAR	Specific Absorption Rate
SCS	Sub-carrier Spacing
SMS	Short Message Service
TCP	Transmission Control Protocol
Tx	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UL	Uplink
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V _{IH}	Input High Voltage Level
V _{IL}	Input Low Voltage Level
V _{OH}	Output High Voltage Level
V _{OL}	Output Low Voltage Level
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
