HIGH-VOLTAGE MIXED-SIGNAL IC

UC8253

All-in-one driver IC w/ Timing Controller for
White/Black/Red Dot-Matrix Micro-Cup ESL

ES Specifications **IC Version: c_A**
Datasheet Revision: 0.61 (for TFT_module_Use_Only) **Nov 25, 2020**

ULTRACHIP

The Coolest EPD Driver, Ever!

Table of Content

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All-in-one driver IC with Timing Controller for White/Black/Red Dot-Matrix Micro-Cup ESL

INTRODUCTION

The UC8253 is an all-in-one driver with timing controller for ESL. Its output is of 1-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for source driver and gate driver.

The DC-DC controller allows it to generate the source output voltage VSH/VSL (±2.4V~±15.0V) and VDHR (+2.4V~+15.0V). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

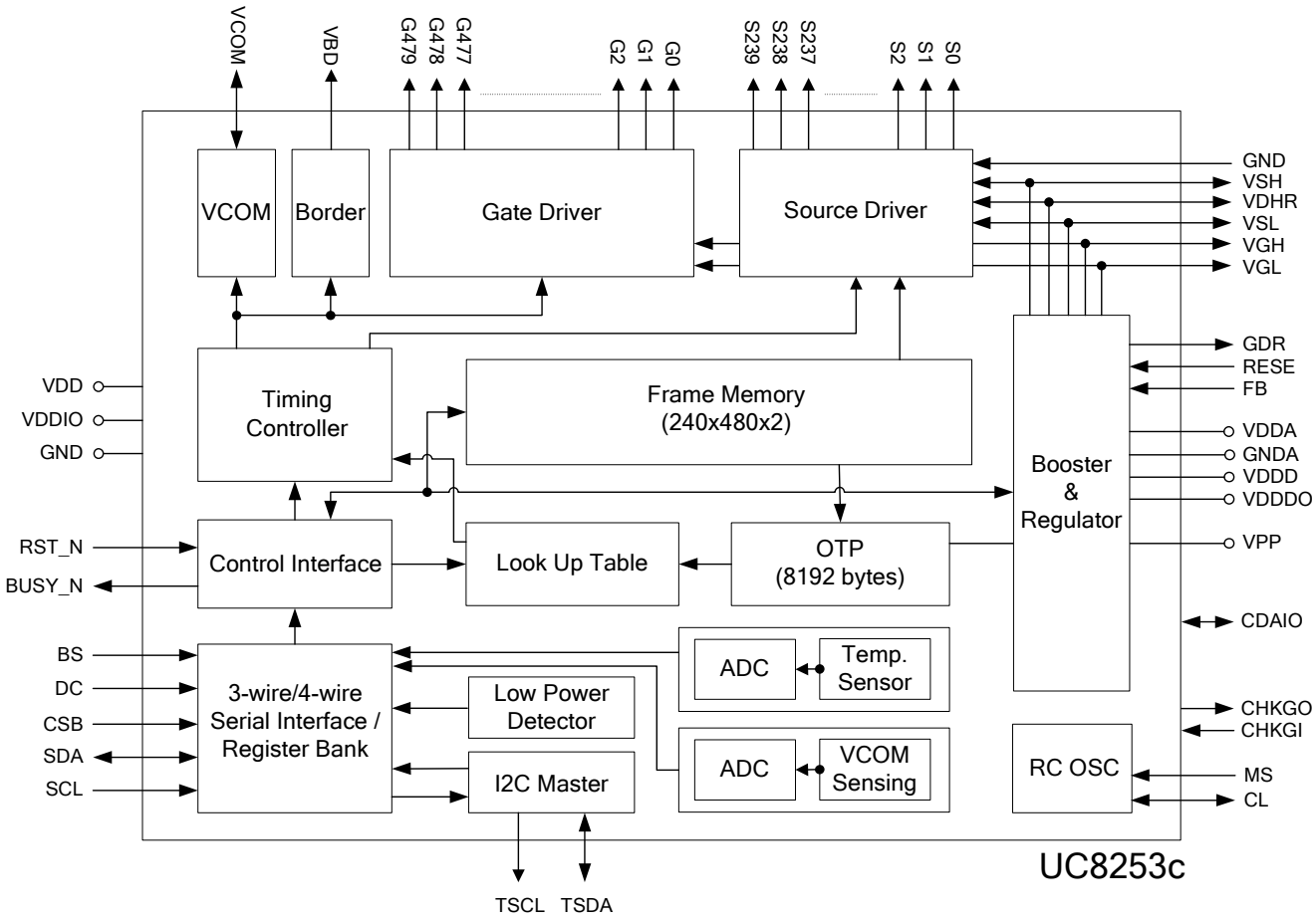
- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several resolutions
  - Up to 240 source x 480 gate resolution + 1 border + 1 VCOM
  - 1 bit for white/black and 1 bit for red per pixel
- Cascade: 2 or more chips cascade mode
- Memory (Max.): 240 x 480 x 2 bits SRAM
- 3-wire/4-wire (SPI) serial interface
  - Clock rate up to 20MHz
- Temperature sensor:
  - On-Chip: -25~50 °C ± 2.0°C / 8-bit status
  - Off-Chip: -55~125°C ± 2.0°C /11-bit status (I^2C/LM75)
- Support LPD, Low Power Detection (V_{DD}<2.5V)
- OSC / PLL: On-chip RC oscillator
- VCOM:
  - AC-VCOM / DC-VCOM (by LUT)
  - Support VCOM sensing (6-bit digital status)
- Charge Pump: On-chip booster and regulator:
  - VGH: +20V
  - VGL: -20V
  - VSH: +2.4 ~ +15.0V (programmable, black/white)
  - VSL: -2.4 ~ -15.0V (programmable, black/white)
  - VDHR: +2.4 ~ +15.0V (programmable, red)
- Supply voltage: 2.3~ 3.6V
- OTP: 8K-byte OTP for LUTs and Settings
- Package: COG
- Source/Gate bump information
  - Bump pitch: 13μM ± 3 μM
  - Bump space: 1μM ± 3 μM
  - Bump surface: 1200μM^2

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
UC8253cGAA-L0P3-3	3-inch tray, wafer thickness 300uM
UC8253cGAA-L0X3-3	3-inch tray, wafer thickness 300uM
UC8253cGAA-L0P3-4	4-inch tray, wafer thickness 300uM
UC8253cGAA-L0X3-4	4-inch tray, wafer thickness 300uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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CONTACT DETAILS

UltraChip Inc. (Headquarter)
4F, No. 618, Recom Road,
Neihu District, Taipei 114,
Taiwan, R. O. C.

Tel: +886 (2) 8797-8947
Fax: +886 (2) 8797-8910
Sales e-mail: sales@ultrachip.com
Web site: http://www.ultrachip.com

PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY PINS			
VDD	7	PWR	Digital power
VDDA	10	PWR	Analog power
VDDIO	10	PWR	IO power
VDDDO	4	PWR	Digital power output (1.32V)
VDDD (VDDDI)	4	PWR	Digital power input (1.32V)
VPP	6	PWR	OTP program power (8.25V)
VDM	4	PWR	Analog Ground.
GND	25	PWR	Digital Ground.
GNDA	10	PWR	Analog Ground.
LDO PINS			
VSH	10	I/O	Positive source driver Voltage (+2.4V ~ +15V)
VDHR	8	I/O	Positive source driver voltage for Red (+2.4V ~ +15V)
VSL	10	I/O	Negative source driver voltage (-2.4V ~ -15V)
CONTROL INTERFACE PINS			
BS	1	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. **H: 3-wire interface. (Default)**
RST_N	1	I (Pull-up)	Global reset pin. L: active. When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. Source/Gate/Border/VCOM will be released to floating. The minimal width of RST_N=low is 50us.
MS	1	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	1	I/O	Clock input/output pin. Master: Clock output. Slave: Clock input.
CDAIO	1	I/O	Cascade data pin. Leave it open if not used.
MM	1	I	Cascade setting pin. Leave it open if not used.
M1M2_SYNC	1	I/O	Cascade sync pin. Leave it open if not used.
BUSY_N		O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.

Pin (Pad) Name	Pin Count	Type	Description
MCU INTERFACE (SPI) PINS			
CSB	1	I	Serial communication chip select.
SDA	1	I/O	Serial communication data input/output
SCL	1	I	Serial communication clock input.
DC	1	I	Command/Data input. L: command H: data Connect to GND if BS=High.
I²C INTERFACE			
TSCL	2	O (open-drain)	I²C clock (External pull-up resistor is necessary.) Leave them open if not used.
TSDA	2	I/O (open-drain)	I²C data (External pull-up resistor is necessary.) Leave them open if not used.
OUTPUT PINS			
S0~S239 (S<0>~S<239>)	240	O	Source driver output signals.
G0~G479 (G<0>~G<479>)	480	O	Gate driver output signals.
VCOM	16	O	VCOM output.
VBD (VBD<1>~VBD<2>)	2	O	Border output pins.
BOOSTER PINS			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	according to application
VGH	12	I/O	Positive Gate voltage.
VGL	16	I/O	Negative Gate voltage.
CHECK PANEL PINS			
CHKGI	1	I (Pull-down)	Check panel break input.
CHKGO	1	O	Check panel break output.
RESERVED PINS			
VSYNC	1	O	Reserved pins. Leave it floating.
TEST1~TEST3	3	I	Reserved pins. Leave it floating or connected to VSS.
TEST6~TEST7	2	O	Reserved pins. Leave it floating.
DUMMY<0> ~ DUMMY<60>	61	-	Reserved pins. Leave it floating.
NC	12	--	Not Connected.
GD<0>~GD<3>	4		Reserved pins. Leave it floating.

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD,SHL, SHD_N,RST_N	0FH
		0	1	--	--	--	#	#	#	#	#	VCMZ ,TS_AUTO,TIEG,NORG,VCM_LUTZ	8DH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	#	--	--	#	#	BD_EN ,VDS_EN, VDG_EN	03H
		0	1	--	--	--	#	#	#	#	#	VCOM_SLEW,VGHL_LV[3:0]	10H
		0	1	--	--	#	#	#	#	#	#	VDH[5:0]	3FH
		0	1	--	--	#	#	#	#	#	#	VDL[5:0]	3FH
		0	1	#	#	#	#	#	#	#	#	OPEN,VDHR[6:0]	0DH
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W or OLD Pixel Data (400x300):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00H
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--	Data_flag	00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (240x480):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	00H
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		1	1	1	0	1	0	0	1	0	1	Check code	A5H
14	VCOM LUT (LUTC) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0		20H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~8 repeated 6 times)	0	0	0	0	1	0	0	0	0	1		21H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H
16	K2W LUT (LUTKW / LUTR) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	1	0		22H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H
17	W2K LUT (LUTWK / LUTW) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	1	1		23H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H
18	K2K LUT (LUTKK / LUTK) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	1	0	0		24H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H
19	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	#	--	--	--	--	--	--	--	EOPT	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[15:8]	00H
		0	1	#	#	#	#	#	#	#	#	GROUP_KWE[7:0]	FFH
		0	1	--	--	--	--	--	--	#	#	ATRED , NORED	00H
20	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	--	--	#	#	#	#	#	#	FRS[4:0]	06H
21	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
22	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00H
23	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42H
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
24	Temperature Sensor Read (TSR)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**		**43H**
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
25	Panel Break Check (PBC)	0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**		**44H**
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
26	VCOM and data interval setting (CDI)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**		**50H**
		0	1	#	#	#	#	#	#	#	#	VBD[1:0], DDX[1:0], CDI[3:0]	D7H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
27	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51H
		1	1	--	--	--	--	--	--	--	#	LPD	01H
28	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
29	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
30	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
31	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H
		0	0	#	#	#	#	#	#	#	#	Reserved	00H
		1	1	#	#	#	#	#	#	#	#	CHIP_REV[7:0]	09H
		1	1	#	#	#	#	#	#	#	#	LUT_REV[23:0]	FFH
		1	1	:	:	:	:	:	:	:	:		FFH
		1	1	#	#	#	#	#	#	#	#		FFH
32	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I²C_ERR, I²C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
33	Cyclic Redundancy Check (CRC)	0	0	0	1	1	0	0	0	1	0		72H
		1	1	#	#	#	#	#	#	#	#	CRC_MSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	CRC_LSB[7:0]	00H
34	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
35	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00H
36	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	00H
37	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	07H
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
38	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H
39	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H
40	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H
41	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H
42	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
43	OTP Programming Address (PGAR)	0	0	1	0	1	0	0	0	1	1		A3 H
		0	1	--	--	--	#	#	#	#	#	ST_ADDR[12:8]	00
		0	1	#	#	#	#	#	#	#	#	ST_ADDR[7:0]	00

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
		0	1	--	--	--	#	#	#	#	#	END_ADDR[12:8]	1F
		0	1	#	#	#	#	#	#	#	#	END_ADDR[7:0]	FF
44	Cascade Setting (CCSET)	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**E0H**
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H
45	Power Saving (PWS)	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**		**E3H**
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
46	LVD Voltage Select (LVSEL)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**		**E4H**
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
47	Force Temperature (TSSET)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**1**		**E5H**
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked ‘W/R’ can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

COMMAND DESCRIPTION

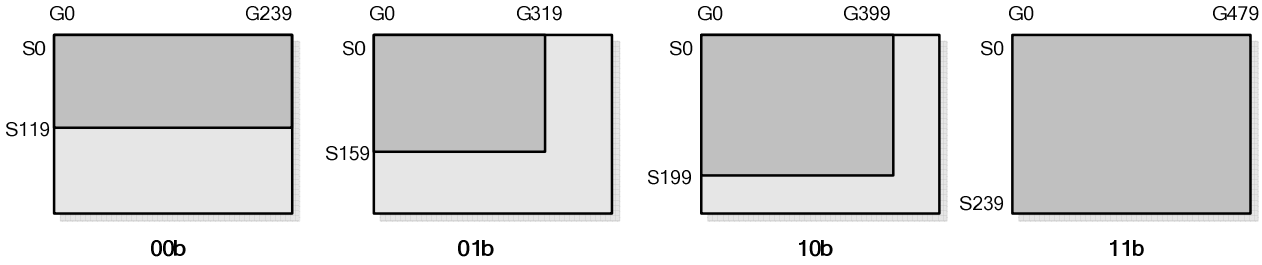
W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH
	0	1	0	0	0	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	0DH

RES[1:0]: Display Resolution setting (source x gate)

00b: 240x120 (Default) Active gate channels: G0 ~ G239. Active source channels: S0 ~ S119.
01b: 320x160 Active gate channels: G0 ~ G319. Active source channels: S0 ~ S159.
10b: 400x200 Active gate channels: G0 ~ G399. Active source channels: S0 ~ S199.
11b: 480x240 Active gate channels: G0 ~ G479. Active source channels: S0 ~ S239.



REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50uS to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.

1: No effect (Default).

VCMZ: VCOM Hi-Z state function

0: No effect (Default)

1 : VCOM is always floating

TS_AUTO: Temperature sensor will be activated automatically one time.

0: No effect

1: Before enabling booster, Temperature Sensor will be activated automatically one time (Default).

TIEG: VGL state function

0: No effect

1 : After power off booster, VGL will be tied to GND (Default).

NORG: VCOM state during refreshing display

0: No effect (Default)

1: Expect refreshing display, VCOM is tied to GND.

VC_LUTZ: VCOM state during refreshing display

0: No effect

1: After refreshing display, the output of VCOM is set to floating automatically (Default).

Note: Priority of Vcom setting: VCMZ > EOPT > NORG > VC_LUTZ

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01H
	0	1	-	-	-	BD_EN	-	-	VDS_EN	VDG_EN	03H
	0	1	-	-	-	VCOM_SLEW	VGHL_LV[3:0]				10H
	0	1	-	-	VSH[5:0]						3FH
	0	1	-	-	VSL[5:0]						3FH
	0	1	OPTEN	VDHR[6:0]							0DH

BD_EN: Border LDO enable
0 : Border LDO disable (Default)
Border level selection: 00b: VCOM 01b: VDH 10b: VDL 11b: VDHR
1 : Border LDO enable
Border level selection: 00b: VCOM 01b: VBH(VCOM-VDL) 10b:VBL(VCOM-VDH) 11b: VDHR

VDS_EN: Source power selection
0 : External source power from VSH/VSL/VDHR pins
1 : Internal DC/DC function for generating VSH/VSL/VDHR. (Default)

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_SLEW: VCOM slew rate selection for voltage transition. The value is fixed at **1**.

VGHL_LV[3:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
0000 (Default)	VGH=20V, VGL= -20V
0001	VGH=19V, VGL= -19V
0010	VGH=18V, VGL= -18V
0011	VGH=17V, VGL= -17V
0100	VGH=16V, VGL= -16V
0101	VGH=15V, VGL= -15V
0110	VGH=14V, VGL= -14V
0111	VGH=13V, VGL= -13V
1000	VGH=12V, VGL= -12V
1001	VGH=11V, VGL= -11V
1010	VGH=10V, VGL= -10V

VSH[5:0]: Internal VSH power selection for B/W pixel.(**Default value: 11 1111b**)

VSH	Voltage	VSH	Voltage	VSH	Voltage	VSH	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	5.0 V	01 1101	8.2V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	**11 1111**	**15.0 V**

VSL[5:0]: Internal VSL power selection for B/W pixel. (**Default value: 11 1111b**)

VSL	Voltage	VSL	Voltage	VSL	Voltage	VSL	Voltage
00 0000	-2.4 V	01 0000	-5.6 V	10 0000	-8.8 V	11 0000	-12.0 V
00 0001	-2.6 V	01 0001	-5.8 V	10 0001	-9.0 V	11 0001	-12.2 V
00 0010	-2.8 V	01 0010	-6.0 V	10 0010	-9.2 V	11 0010	-12.4 V
00 0011	-3.0 V	01 0011	-6.2 V	10 0011	-9.4 V	11 0011	-12.6 V
00 0100	-3.2 V	01 0100	-6.4 V	10 0100	-9.6 V	11 0100	-12.8 V
00 0101	-3.4 V	01 0101	-6.6 V	10 0101	-9.8 V	11 0101	-13.0 V
00 0110	-3.6 V	01 0110	-6.8 V	10 0110	-10.0V	11 0110	-13.2 V
00 0111	-3.8 V	01 0111	-7.0 V	10 0111	-10.2 V	11 0111	-13.4 V
00 1000	-4.0 V	01 1000	-7.2 V	10 1000	-10.4 V	11 1000	-13.6 V
00 1001	-4.2 V	01 1001	-7.4 V	10 1001	-10.6 V	11 1001	-13.8 V
00 1010	-4.4 V	01 1010	-7.6 V	10 1010	-10.8 V	11 1010	-14.0 V
00 1011	-4.6 V	01 1011	-7.8 V	10 1011	-11.0 V	11 1011	-14.2 V
00 1100	-4.8 V	01 1100	-8.0 V	10 1100	-11.2 V	11 1100	-14.4 V
00 1101	-5.0 V	01 1101	-8.2 V	10 1101	-11.4 V	11 1101	-14.6 V
00 1110	-5.2 V	01 1110	-8.4 V	10 1110	-11.6 V	11 1110	-14.8 V
00 1111	-5.4 V	01 1111	-8.6 V	10 1111	-11.8 V	**11 1111**	**-15.0 V**

VDHR[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 001101b**)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0 V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	**5.0 V**	01 1101	8.2 V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	11 1111	15.0 V

OPTEN: 1 enable step-0.1V voltage selection.

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
1000 0000	2.4 V	1010 0000	5.6 V	1100 0000	8.8 V	1110 0000	12 V
1000 0001	2.5 V	1010 0001	5.7 V	1100 0001	8.9 V	1110 0001	12.1 V
1000 0010	2.6 V	1010 0010	5.8 V	1100 0010	9.0 V	1110 0010	12.2 V
1000 0011	2.7 V	1010 0011	5.9 V	1100 0011	9.1 V	1110 0011	12.3 V
1000 0100	2.8 V	1010 0100	6.0 V	1100 0100	9.2 V	1110 0100	12.4 V
1000 0101	2.9 V	1010 0101	6.1 V	1100 0101	9.3 V	1110 0101	12.5 V
1000 0110	3.0 V	1010 0110	6.2 V	1100 0110	9.4 V	1110 0110	12.6 V
1000 0111	3.1 V	1010 0111	6.3 V	1100 0111	9.5 V	1110 0111	12.7 V
1000 1000	3.2 V	1010 1000	6.4 V	1100 1000	9.6 V	1110 1000	12.8 V
1000 1001	3.3 V	10101001	6.5 V	1100 1001	9.7 V	1110 1001	12.9 V
1000 1010	3.4 V	1010 1010	6.6 V	1100 1010	9.8 V	1110 1010	13.0 V
1000 1011	3.5 V	1010 1011	6.7 V	1100 1011	9.9 V	1110 1011	13.1 V
1000 1100	3.6 V	1010 1100	6.8 V	1100 1100	10.0 V	1110 1100	13.2 V
1000 1101	3.7 V	1010 1101	6.9 V	1100 1101	10.1 V	1110 1101	13.3 V
1000 1110	3.8 V	1010 1110	7.0 V	1100 1110	10.2 V	1110 1110	13.4 V
1000 1111	3.9 V	1010 1111	7.1 V	1100 1111	10.3 V	1110 1111	13.5 V
1001 0000	4.0 V	1011 0000	7.2 V	1101 0000	10.4 V	1111 0000	13.6 V
1001 0001	4.1 V	1011 0001	7.3 V	1101 0001	10.5 V	1111 0001	13.7 V
1001 0010	4.2 V	1011 0010	7.4 V	1101 0010	10.6 V	1111 0010	13.8 V
1001 0011	4.3 V	1011 0011	7.5 V	1101 0011	10.7 V	1111 0011	13.9 V
1001 0100	4.4 V	1011 0100	7.6 V	1101 0100	10.8 V	1111 0100	14.0 V
1001 0101	4.5 V	1011 0101	7.7 V	1101 0101	10.9 V	1111 0101	14.1 V
1001 0110	4.6 V	1011 0110	7.8 V	1101 0110	11.0 V	1111 0110	14.2 V
1001 0111	4.7 V	1011 0111	7.9 V	1101 0111	11.1 V	1111 0111	14.3 V
1001 1000	4.8 V	1011 1000	8.0 V	1101 1000	11.2 V	1111 1000	14.4 V
1001 1001	4.9 V	1011 1001	8.1 V	1101 1001	11.3 V	1111 1001	14.5 V
1001 1010	5.0 V	1011 1010	8.2 V	1101 1010	11.4 V	1111 1010	14.6 V
1001 1011	5.1 V	1011 1011	8.3 V	1101 1011	11.5 V	1111 1011	14.7 V
1001 1100	5.2 V	1011 1100	8.4 V	11011100	11.6 V	1111 1100	14.8 V
1001 1101	5.3 V	1011 1101	8.5 V	1101 1101	11.7 V	1111 1101	14.9 V
1001 1110	5.4 V	1011 1110	8.6 V	1101 1110	11.8 V	1111 1110	15.0 V
1001 1111	5.5 V	1011 1111	8.7 V	1101 1111	11.9 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	03H
	0	1	**-**	**-**	T_VDS_OFF[1:0]		**-**	**-**	**-**	**-**	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17H
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17H
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17H

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be larger than 200uS.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “NEW” data to SRAM.

In KWR mode, this command writes “RED” data to SRAM.

(13) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	17H
	0	1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host’s control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for VCOM (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0	20H
	0	1	Group Repeat Time [7:0]								00H
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						0
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						0
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						0
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						0
	0	1	State 1 repeat times [7:0]								0
	0	1	State 2 repeat times [7:0]								0

This command stores VCOM Look-Up Table with 8 groups of data. This LUT includes 8 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34……:

[D7:D6] Level selection

00b: VCOM_DC

01b: VSH+VCOM_DC (VCOMH)

10b: VSL-VCOM_DC (VCOML)

11b: Floating

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), all 8 groups are used.

If KW/R=1 (KW mode), only 6 groups are used.

(15) W2W LUT (LUTWW) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build White Look-up Table for W2W (43-byte command, structure of bytes 2~8 repeated 6 times)	0	0	0	0	1	0	0	0	0	1	21H
	0	1	Group Repeat Time [7:0]								
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						00H
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						
	0	1	State 1 repeat times [7:0]								
	0	1	State 2 repeat times [7:0]								

This command stores LUTW2W Look-Up Table with 6 groups of data. This LUT includes 6 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34……:

[D7:D6] Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), LUTWW is not used.

If KW/R=1 (KW mode), LUTWW is used.

(16) K2W LUT (LUTKW / LUTR) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for K2W or Red (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0	20H
	0	1	Group Repeat Time [7:0]								00H
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						00H
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						00H
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						00H
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						00H
	0	1	State 1 repeat times [7:0]								00H
	0	1	State 2 repeat times [7:0]								00H

This command stores LUTKW / LUTR Look-Up Table with 8 groups of data. This LUT includes 8 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34……:

[D7:D6] Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), all 8 groups are used.

If KW/R=1 (KW mode), only 6 groups are used.

(17) W2K LUT (LUTWK / LUTW) (R23H)

This command builds Look-up Table for White-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used.

(18) K2K LUT (LUTKK / LUTK) (R24H)

This command builds Look-up Table for Black-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.

Note: All LUTs are independent of each other and could be deal with separately.If waveform time is different for each LUT , IC would elect longest LUT as refresh time and fill 0 (GND) to remaining refresh time for other LUT.

(19) LUT OPTION (LUTOPT) (R2AH)

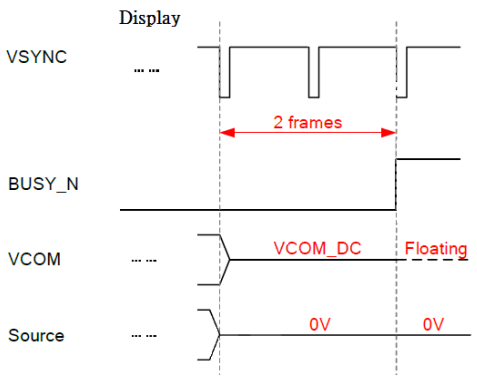
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	2AH
	0	1	EOPT	ESO	-	-	-	-	-	-	00H
	0	1	STATE_XON[7:0]								00H
	0	1	STATE_XON[15:8]								00H
	0	1	GROUP_KWE[7:0]								FFH
	0	1	-	-	-	-	-	ATRED	NORED		00H

This command sets XON and the several options of KWR mode's LUT. .

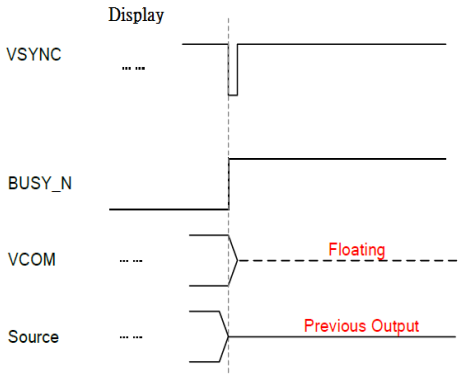
EOPT: LUT sequence option

0: Disable 1: Enable

EOPT=0



EOPT=1



ESO: LUT sequence option 2

STATE_XON[15:0]:

All Gate ON control (Each bit controls one state, STATE_XON [0] for Group-1/State-1, STATE_XON [1] for Group-1/State-2 …..)

0000 0000 0000 0000b: no All-Gate-ON

0000 0000 0000 0001b: Group-1/State-1 All-Gate-ON

0000 0000 0000 0011b: Group-1/State-1 and Group-1/State-2 All-Gate-ON

0000 0000 0000 0111b: Group-1/State-1, Group-1/State-2 and Group-2/State-1 All-Gate-ON

: :

GROUP_KWE[7:0]:

The control bits are only available when KW/R=0 (KWR mode) and (ATRED | NORED)=1

There are only 8 groups in the K/W LUT. Each bit controls one group.

1111 1111b: all groups are executed sequentially.

1111 1110b: only Group-1 is bypassed.

1111 1100b: Group-1 and Group-2 are bypassed.

: :

ATRED: Automatic mode. The option is only available when KW/R=0

NORED: No Red data. The option is only available when KW/R=0

(20) PLL CONTROL (PLL) (R30H)

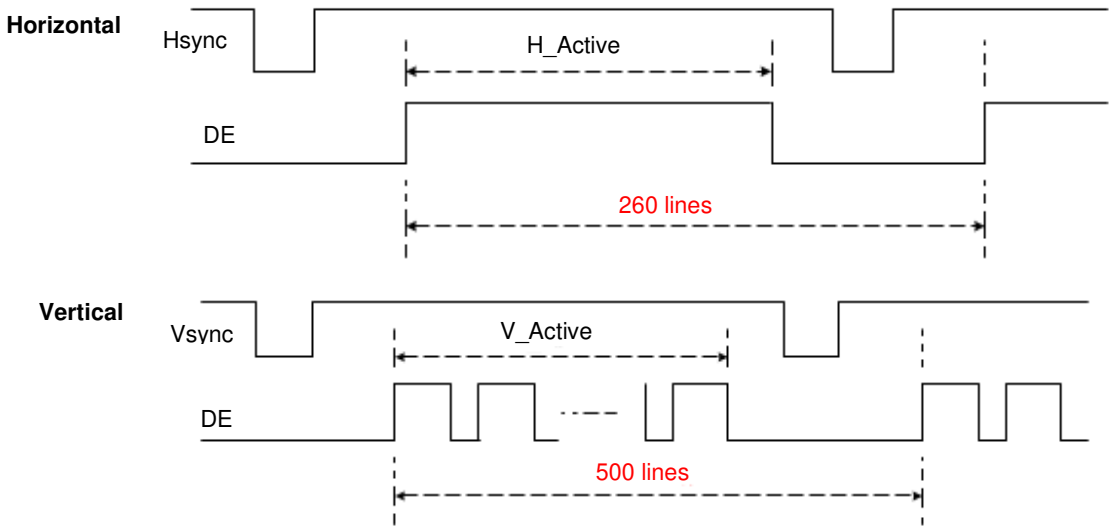
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30H
	0	1	-	-	-	FRS[4:0]					09H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[4:0]: Frame rate setting

FRS	Frame rate
00000	5Hz
00001	10Hz
00010	15Hz
00011	20Hz
00100	25Hz
00101	30Hz
00110	35Hz
00111	40Hz
01000	45Hz
01001	**50Hz**
01010	55Hz
01011	60Hz
01100	65Hz
01101	70Hz
01110	75Hz
01111	80Hz

FRS	Frame rate
10000	85Hz
10001	90Hz
10010	95Hz
10011	100Hz
10100	105Hz
10101	110Hz
10110	115Hz
10111	120Hz
11000	130Hz
11001	140Hz
11010	150Hz
11011	160Hz
11100	170Hz
11101	180Hz
11110	190Hz
11111	200Hz



(21) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature(°C)
0000_0000	**0**
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temperature(°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(22) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(23) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I²C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(24) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(25) PANEL GLASS CHECK (PBC) (R44H)

Action	R/W	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	44H
	R	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(26) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50h
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7h

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for B/W data,

DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

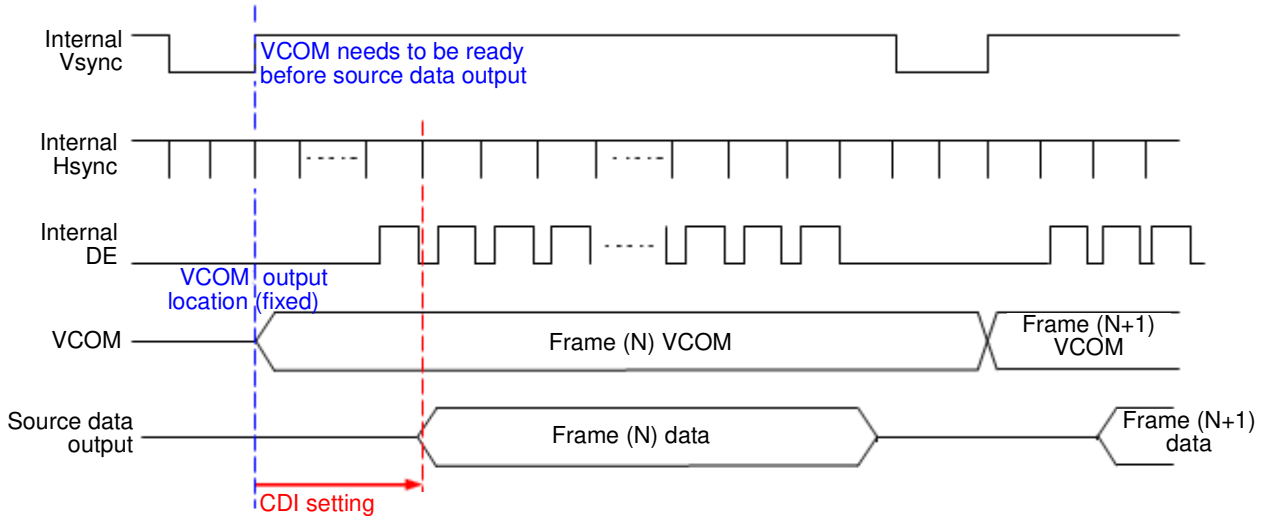
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



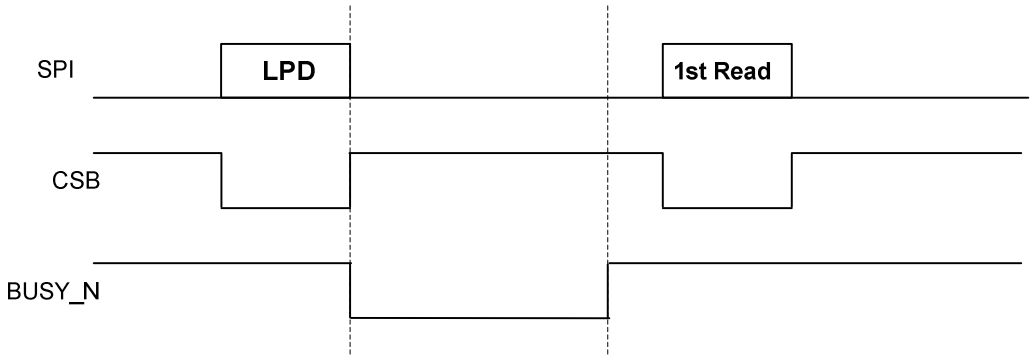
(27) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(28) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

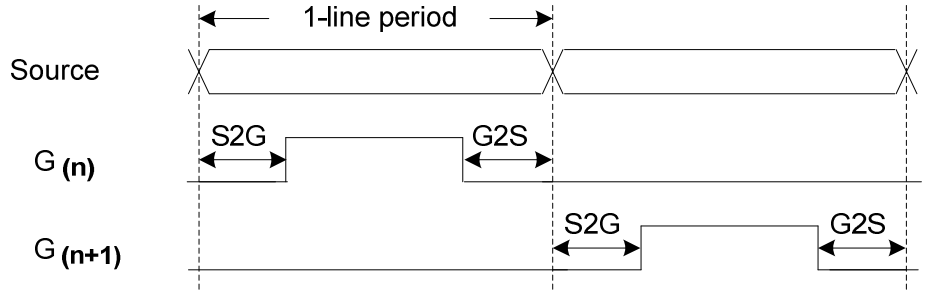
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 650 nS.



(29) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	HRES[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation, assuming HRES[7:3]=0, VRES[8:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[8:0] – 1

Source: First active source = S0;
Last active source = HRES[7:3]*8 - 1

Example: 128 (source) x 272 (gate), assuming HRES[7:3]=0, VRES[8:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[8:0] = 272, 272 - 1= 271)

Source: First active source = S0,
Last active source = S127; (HRES[7:3]=16, 16*8 – 1 = 127)

(30) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)

VST[8:0]: Vertical Display Start Position (Gate)

Example : For 128(Source) x 240(Gate)
HST[7:3] = 4 (HST[8:0] = 4*8 = 32),
VST[8:0] = 32

Gate: First active gate = G32 (VST[8:0] = 32),
Last active gate = G271 (VST[8:0] = 32, VRES[8:0] = 240, 32+240-1=271)

Source: First active source = S32 (HST[7:3] = 32),
Last active source = S159 (HST[7:3] = 32, HRES[8:0] = 128, 32+128-1=159)

(31) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	70h
	1	1	RESERVED								FFh
	1	1	CHIP_REV[7:0]								09h
	1	1	LUT_REV[7:0]								FFh
	1	1	LUT_REV[15:8]								FFh
	1	1	LUT_REV[23:16]								FFh

The LUT_REV is read from OTP address = 0x0017~0x0019 / 0x1017~0x1019.

CHIP_REV[7:0]: Chip Revision, fixed at 0x09h.

(32) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	71h
	1	1	-	PTL_ flag	I²C_ERR	I²C_ BUSYN	data_ flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_FLAG Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSYN: I²C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(33) CYCLIC REDUNDANCY CHECK (CRC) (R72H)

Action	R/W	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Cyclic redundancy check	R	0	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	72H
	R	1	CRC_MSB[7:0]								FFH
	R	1	CRC_LSB[7:0]								FFH

This command reads Cyclic redundancy check(CRC) result.

The calculation only includes 0x0000~0x1FEF OTP data..

Polynomial = $x^{16} + x^{12} + x^5 + 1$, initial vaulte: 16'hFFFF

The result will be reset after this command.

CRC_MSB[7:0]: Most significant bits of CRC result

CRC_LSB[7:0]: Most significant bits of CRC result

(34) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s
01b: 5s (default)
10b: 8s
11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(35) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	-	VV[6:0]						00h

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(36) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	-	VDCS[6:0]						00h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(37) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~1Dh)

HRED[7:3]: Horizontal end channel bank. (value 00h~1Dh). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~1DFh)

VRED[8:0]: Vertical end line. (value 000h~1DFh). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(38) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(39) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(40) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(41) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

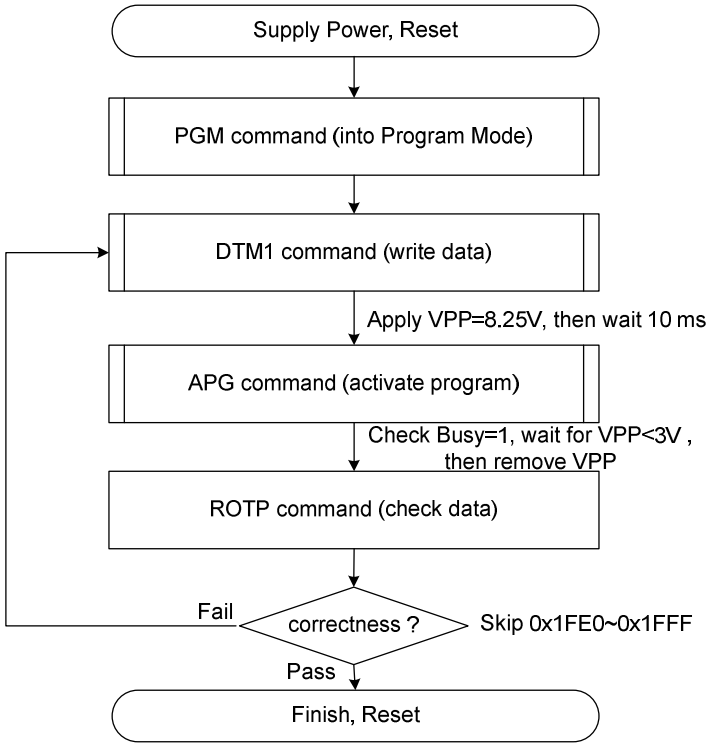
The BUSY_N flag would fall to 0 until the programming is completed.

(42) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.



The sequence of programming OTP.

(43) OTP PROGRAMMING ADDRESS (PGAR) (RA3H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
OTP Programming Address	0	0	1	0	1	0	0	0	1	1	A3H
	0	1	-	-	-	ST_ADDR[12:8]					00
	0	1	ST_ADDR[7:0]								00
	0	1	-	-	-	END_ADDR[12:8]					1F
	0	1	END_ADDR[7:0]								FF

The command is set OTP programming memory start address and end address.

ST_ADDR [12:0]: OTP programming start address.

END_ADDR [12:0]: OTP programming end address.

Example:

For Bank0 0x0000 (start address) ~ 0x0FFF (end address), 4K bytes.

ST_ADDR [12:8] = 0x00

ST_ADDR [7:0] = 0x00

END_ADDR [12:8] = 0x0F

END_ADDR [7:0] = 0xFF

For Bank1 0x1000 (start address) ~ 0x1FFF (end address), 4K bytes.

ST_ADDR [12:8] = 0x10

ST_ADDR [7:0] = 0x00

END_ADDR [12:8] = 0x1F

END_ADDR [7:0] = 0xFF

(44) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

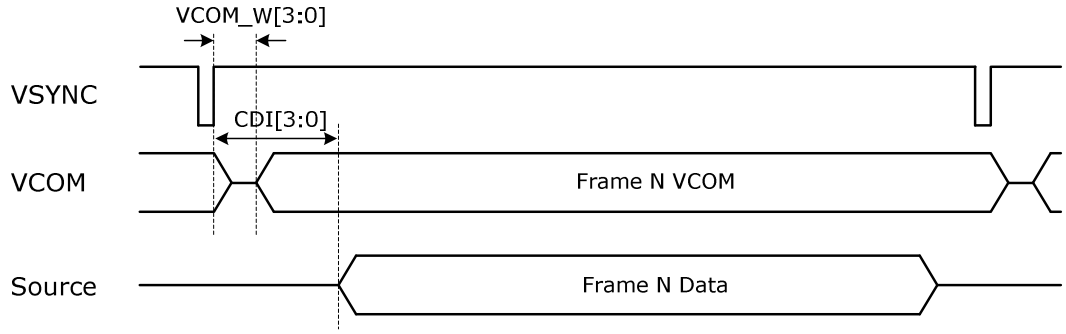
1: Temperature value is defined by TS_SET[7:0] registers.

(45) POWER SAVING (PWS) (RE3H)

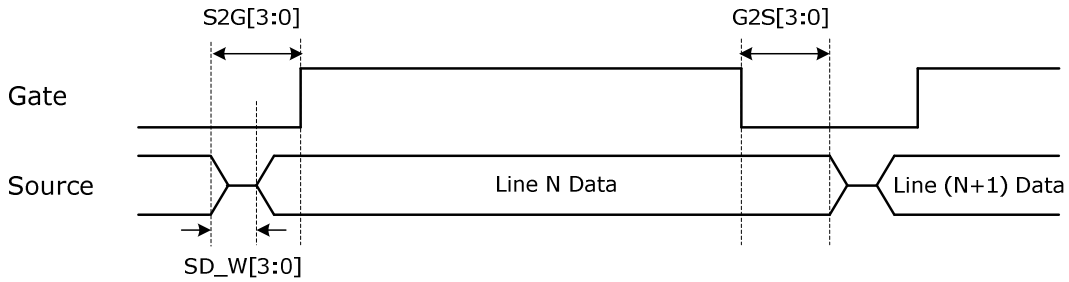
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 650nS)



(46) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(47) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

HOST INTERFACES

UC8253 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

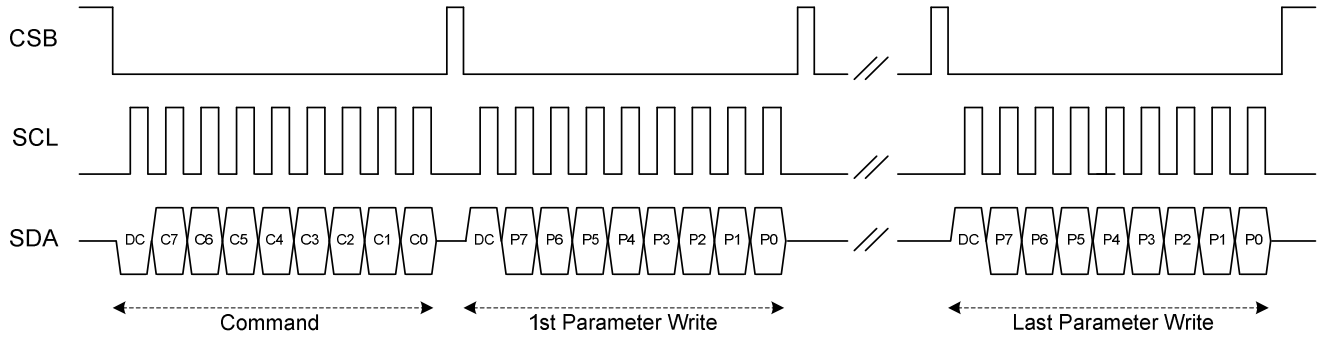


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

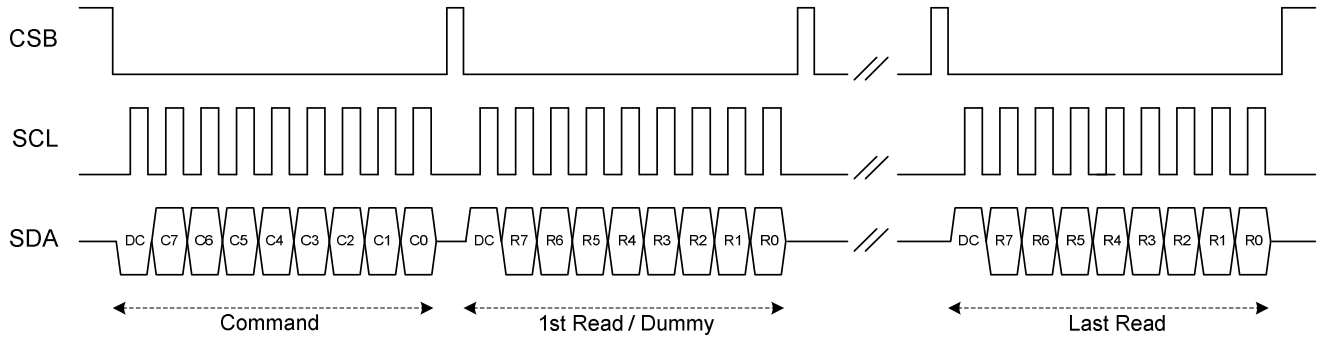


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

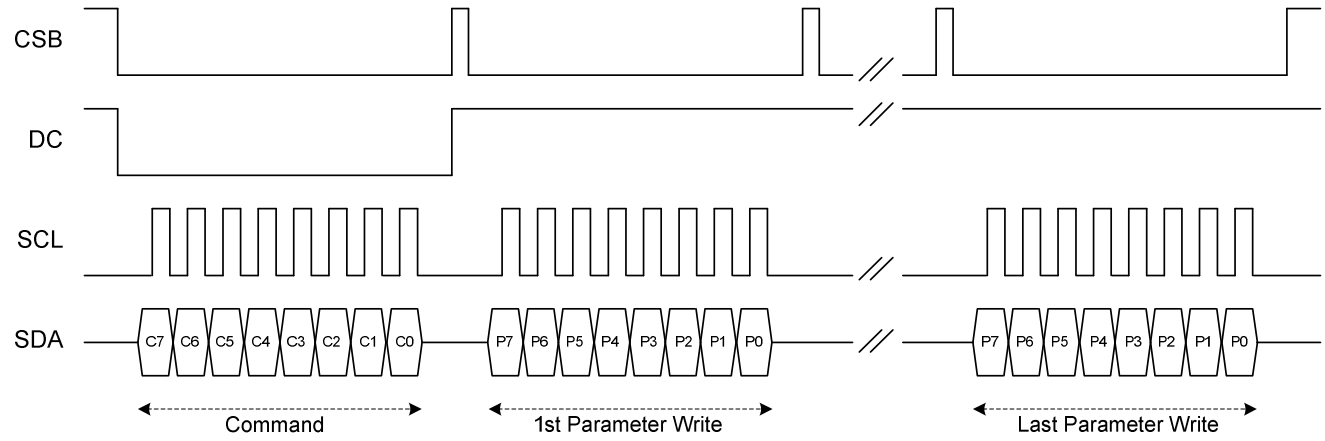


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High. Only in the case of OTP data read, the 1st packet of output data are dummy data.

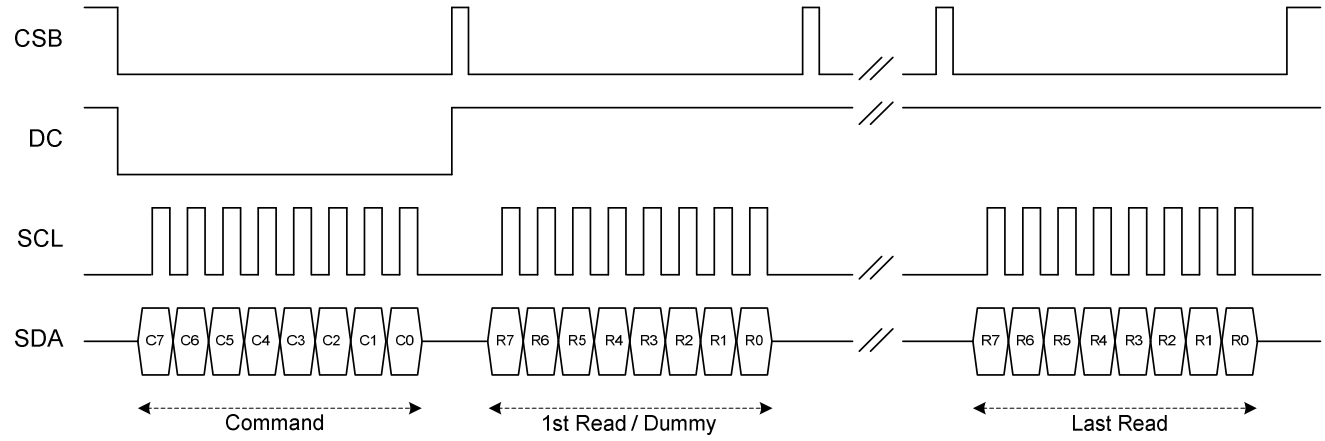
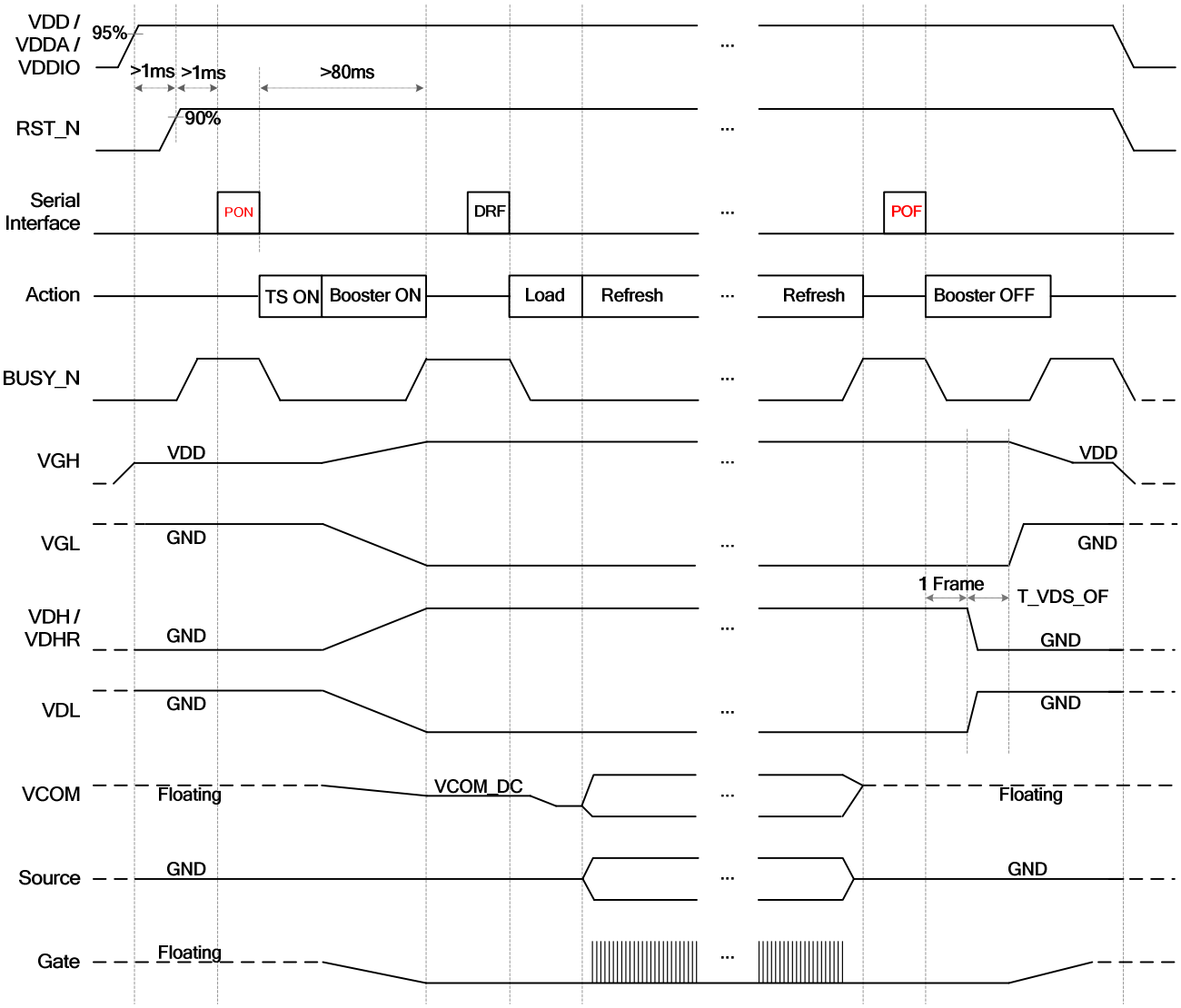


Figure: 4-wire SPI read operation

POWER MANAGEMENT

Power ON/OFF Sequence

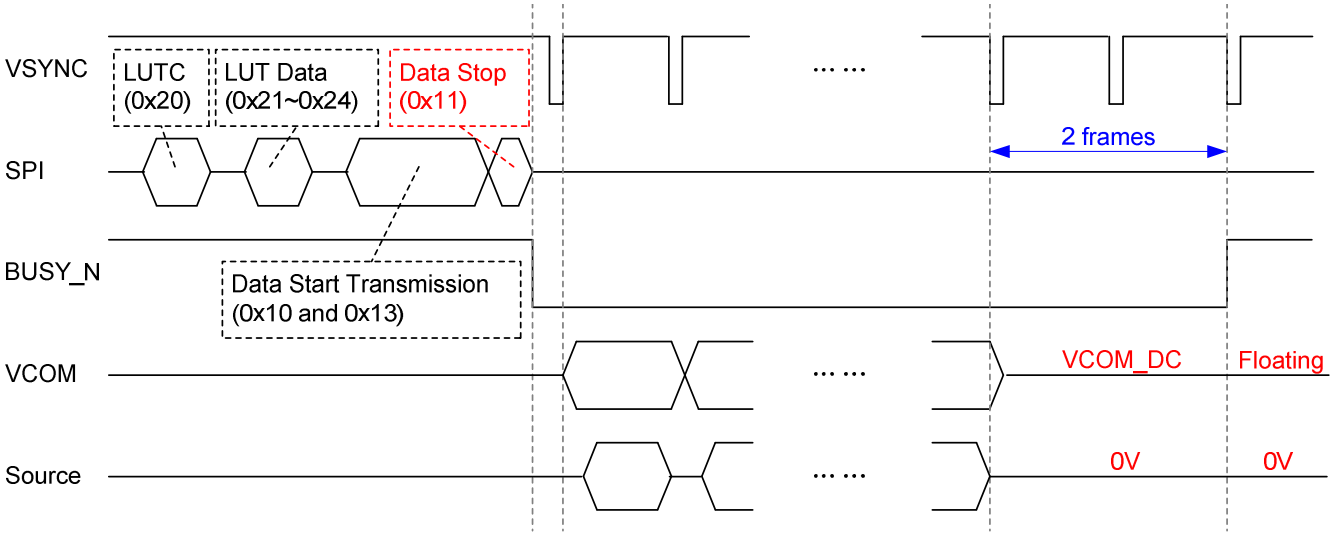
1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. In OTP mode (REG=0), the LUT in OTP will be copied to register automatically after the DSP/DRF command.
4. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



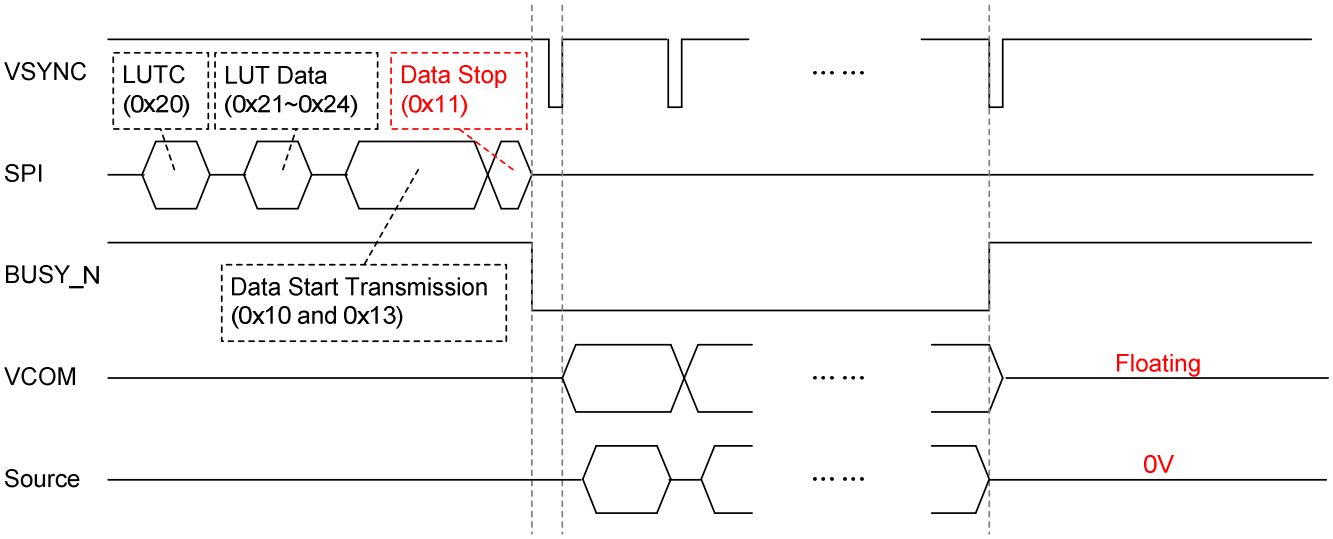
Data Transmission Waveform

Example 1: After 3 cases, the driver will send 2 frame VCOM and data to 0 V.

1. All 6 LUT groups (KW mode) or 8 LUT groups (KWR mode) complete.
2. meet the state whose Times to Repeat =0
3. meet the state whose all Number of Frames =0



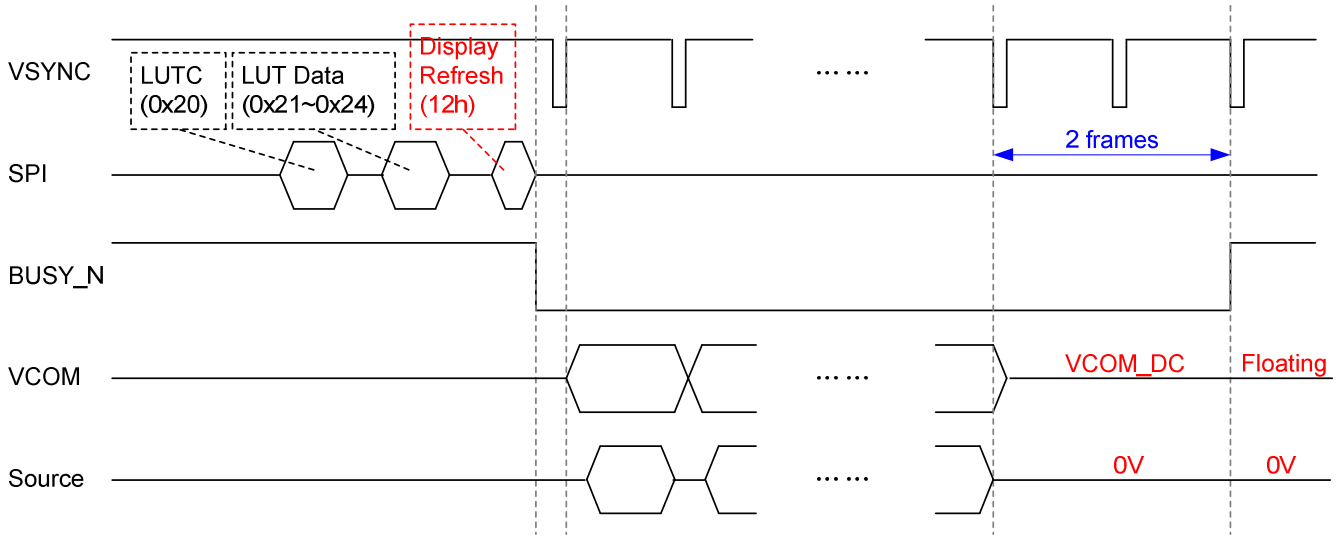
Example2: While level selection in LUT (LUTC only) is “1111_1111b”, the driver will float VCOM.



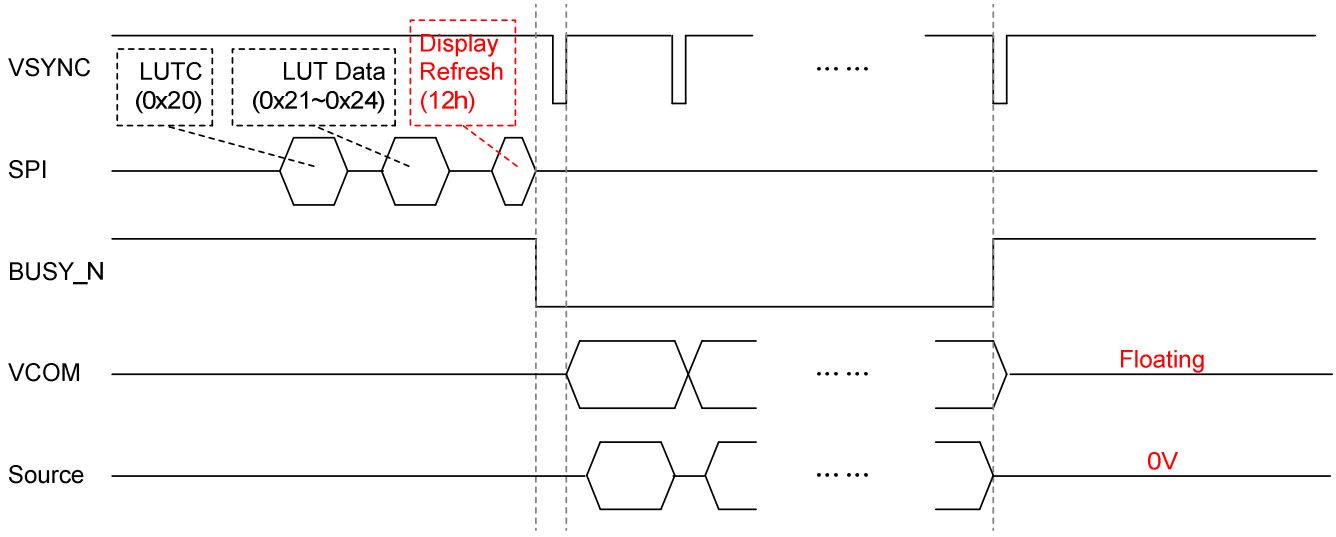
Display Refresh Waveform

Example 1: After three cases, the driver will send 2 frames VCOM and data to 0 V.

1. All 6 LUT groups (KW mode) or 8 LUT groups (KWR mode) complete
2. meet the state whose Times to Repeat = 0
3. meet the state whose all Number of Frames = 0



Example2: While level selection in LUT (LUTC only) is “1111_1111b”, the driver will float VCOM.



BUSY_N Signal

Commands, except reading command, are restricted by refreshing display (DRF / DSP) as listed in the following table.

BUSY_N is used to represent the status of internal action. Commands activating internal operation or calculation will cause BUSY_N falling to LOW. After actions completed, BUSY_N will return to HIGH.

Command	Refresh Restriction	BUSY_N flag
PSR	X	No action
PWR	X	No action
POF	X	Flag
PFS	X	No action
PON	X	Flag
PMES	X	Flag
BTST	X	No action
DSLP	X	Flag
AUTO	X	Flag
DTM1	X	No action
DSP	X	Flag
DRF	X	Flag
DTM2	X	No action
LUTC	X	No action
LUTWW	X	No action
LUTWK/LUTW	X	No action
LUTKW/LUTR	X	No action
LUTKK/LUTK	X	No action
LUTOPT	X	No action
PLL	X	No action
TSC	X	Flag
TSE	X	No action
TSW	X	No action
TSR	X	No action
PBC	X	No action
CDI	X	No action
LPD	X	Flag
TCON	X	No action
TRES	X	No action
GSST	X	No action
REV	V	No action
FLG	V	No action
AMV	X	Flag
VV	V	No action
VDCS	X	No action
PTL	X	No action
PTIN	X	No action
PTOUT	X	No action
PGM	X	No action
APG	X	Flag
ROTP	X	No action
CCSET	X	No action
PWS	X	No action
LVSEL	X	No action
TSSET	X	No action

V: Accepted, X: Ignored

OTP ADDRESS MAPPING

The size of the internal One Time Programmable (OTP) memory is 8K bytes, and the address is from 0x000 to 0x1FFF. The unprogrammed bit is logic 1. Only the bit at logic 1 can be programmed to logic 0, but the bit at logic 0 can not be converted to logic 1.

There is an area (0x1FE0~0x1FFF) are reserved for UltraChip only, and write all 0xFF of data to skip the area. The recommended voltage of VPP during programming is 8.25V. In the other condition except for programming, let VPP floating or be connected to GND. The maximum current of VPP during programming is 5mA.

There are 2 banks in the internal OTP, and each bank has 4K bytes storage memory. The formats of each bank are the same, and the selection of bank is controlled by Check Code (0x0000 and 0x1000). The 2 banks are used for two times programming.

Table 1: OTP Address Map

Bank0		Bank1	
Address	Content	Address	Content
0x0000	Check Code (0xA5)	0x1000	Check Code (0xA5)
0x0001~0x0013	Command Default Setting *(1)	0x1001~0x1013	Command Default Setting *(1)
0x0014~0x0016	Chip ID [23:0]	0x1014~0x1016	Chip ID [23:0]
0x0017~0x0019	LUT Version [23:0]	0x1017~0x1019	LUT Version [23:0]
0x001A~0x0029	Temperature Boundary 0~11 (TB0~TB15)	0x101A~0x1029	Temperature Boundary 0~11 (TB0~TB15)
0x002A~0x0112	Temperature Range 0 *(2)	0x102A~0x1112	Temperature Range 0 *(2)
0x0113~0x01FB	Temperature Range 1 *(2)	0x1113~0x11FB	Temperature Range 1 *(2)
0x01FC~0x02E4	Temperature Range 2 *(2)	0x11FC~0x12E4	Temperature Range 2 *(2)
0x02E5~0x03CD	Temperature Range 3 *(2)	0x12E5~0x13CD	Temperature Range 3 *(2)
0x03CE~0x04B6	Temperature Range 4 *(2)	0x13CE~0x14B6	Temperature Range 4 *(2)
0x04B7~0x059F	Temperature Range 5 *(2)	0x14B7~0x159F	Temperature Range 5 *(2)
0x05A0~0x0688	Temperature Range 6 *(2)	0x15A0~0x1688	Temperature Range 6 *(2)
0x0689~0x0771	Temperature Range 7 *(2)	0x1689~0x1771	Temperature Range 7 *(2)
0x0772~0x085A	Temperature Range 8 *(2)	0x1772~0x185A	Temperature Range 8 *(2)
0x085B~0x0943	Temperature Range 9 *(2)	0x185B~0x1943	Temperature Range 9 *(2)
0x0944~0x0A2C	Temperature Range 10 *(2)	0x1944~0x1A2C	Temperature Range 10 *(2)
0x0A2D~0x0B15	Temperature Range 11 *(2)	0x1A2D~0x1B15	Temperature Range 11 *(2)
0x0B16~0x0BFE	Temperature Range 12 *(2)	0x1B16~0x1BFE	Temperature Range 12 *(2)
0x0BFF~0x0CE7	Temperature Range 13 *(2)	0x1BFF~0x1CE7	Temperature Range 13 *(2)
0x0CE8~0x0DD0	Temperature Range 14 *(2)	0x1CE8~0x1DD0	Temperature Range 14 *(2)
0x0DD1~0x0EB9	Temperature Range 15 *(2)	0x1DD1~0x1EB9	Temperature Range 15 *(2)
0x0EBA~0x0FA2	Temperature Range 16 *(2)	0x1EBA~0x1FA2	Temperature Range 16 *(2)
0x0FA3~0x0FFF	Reserved for user-defined	0x1FA3~0x1FDF	Reserved for user-defined
		0x1FE0~0x1FFF	Reserved for UltraChip

Note:

(1) See section “COMMAND DEFAULT SETTING” for more detail.

(2) See section “LUT FORMAT IN OTP” for more detail.

TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 15 temperature boundary settings (TBx) to determine 16 temperature ranges. The sequence of mechanism is from TB0 to TB15, as shown below. If less than 16 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Procedure Order	Comparison Condition	Action & Segment Selection
1-0. Read 0x000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank0), No: Jump to Procedure 1-1
1-1, Read 0xC00	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank1), No: Stop Refresh
2. Read 0x001A / 0x101A	Real Temperature ≦ TB0	Use TR0's table & setting, exit
3. Read 0x001B / 0x101B	Real Temperature ≦ TB1	Use TR1's table & setting, exit
4. Read 0x001C / 0x101C	Real Temperature ≦ TB2	Use TR2's table & setting, exit
5. Read 0x001D / 0x101D	Real Temperature ≦ TB3	Use TR3's table & setting, exit
6. Read 0x001E / 0x101E	Real Temperature ≦ TB4	Use TR4's table & setting, exit
7. Read 0x001F / 0x101F	Real Temperature ≦ TB5	Use TR5's table & setting, exit
8. Read 0x0020 / 0x1020	Real Temperature ≦ TB6	Use TR6's table & setting, exit
9. Read 0x0021 / 0x1021	Real Temperature ≦ TB7	Use TR7's table & setting, exit
10. Read 0x0022 / 0x1022	Real Temperature ≦ TB8	Use TR8's table & setting, exit
11. Read 0x0023 / 0x1023	Real Temperature ≦ TB9	Use TR9's table & setting, exit
12. Read 0x0024 / 0x1024	Real Temperature ≦ TB10	Use TR10's table & setting, exit
13. Read 0x0025 / 0x1025	Real Temperature ≦ TB11	Use TR11's table & setting, exit
14. Read 0x0026 / 0x1026	Real Temperature ≦ TB12	Use TR12's table & setting, exit
15. Read 0x0027 / 0x1027	Real Temperature ≦ TB13	Use TR13's table & setting, exit
16. Read 0x0028 / 0x1028	Real Temperature ≦ TB14	Use TR14's table & setting, exit
17. Read 0x0029 / 0x1029	Real Temperature ≦ TB15	Use TR15's table & setting, exit
18. Other	Real Temperature > TB15	Use TR16's table & setting, finish

***Note:**

(1) TRx's content is defined in “LUT FORMAT IN OTP” section.

Example:

If temperature = -20 ºC, TR0 is selected.

If temperature = -10 ºC, TR1 is selected.

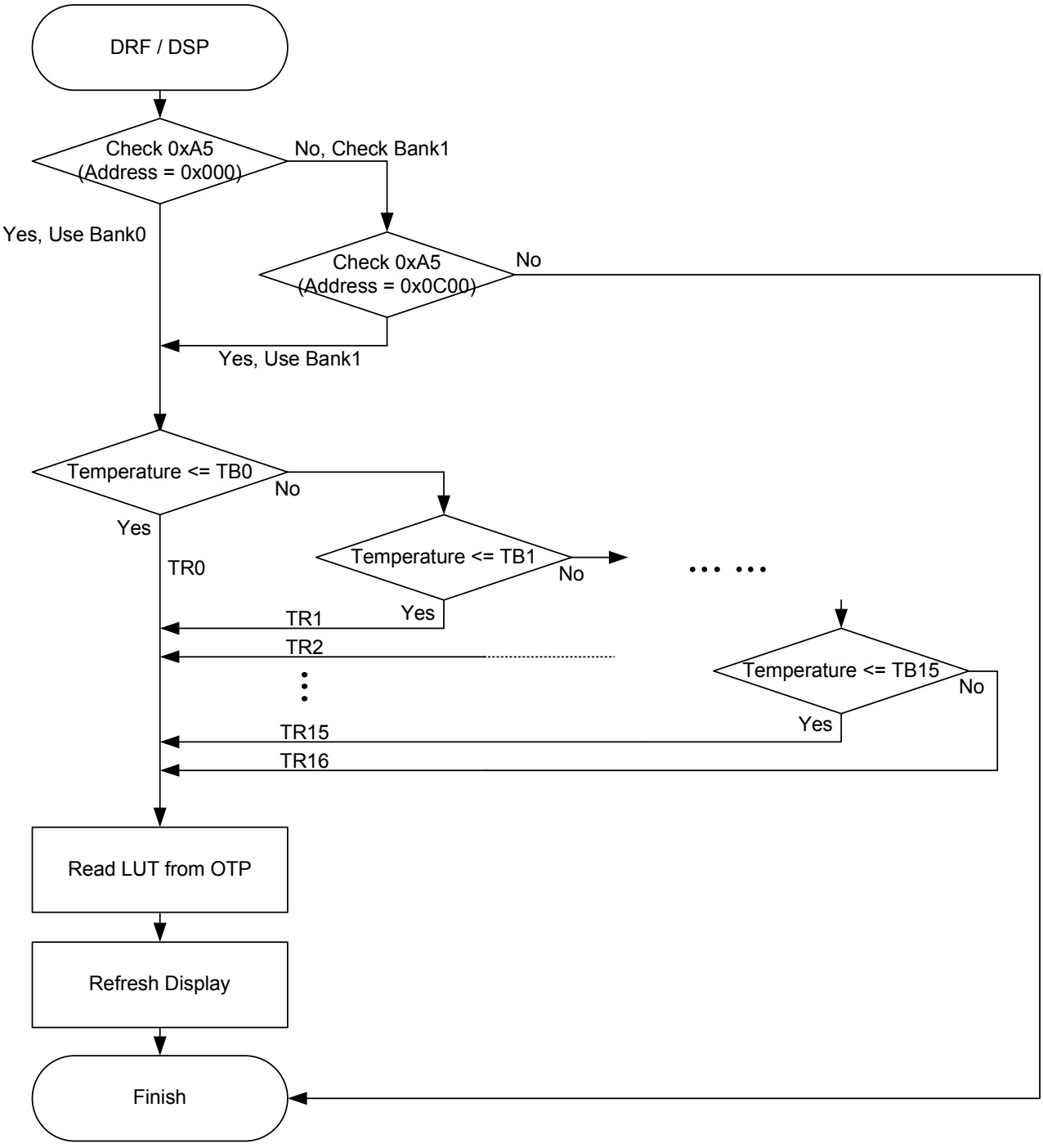
If temperature = 0 ºC, TR2 is selected.

If temperature = 20 ºC, TR4 is selected.

If temperature = 40 ºC, TR5 is selected.

If temperature > 40 ºC, TR5 is selected.

OTP Address	Content	
002h	0xF1	(-15 ºC)
003h	0xFB	(-5 ºC)
004h	0x00	(0 ºC)
005h	0x0A	(10 ºC)
006h	0x1E	(30 ºC)
007h	0x7F	-



Temperature Selection Mechanism

COMMAND DEFAULT SETTING

This function can modify the default value of command registers by the OTP content between address 0x0001~0x0013 (or 0x0101~0x1013). The data of address 0x0001 (or 0x0C01) is the enable key of the function. Changing default value function is used to reduce the initial code length executed by the microcontroller.

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Command	Registers	Original
0x0001	#	#	#	#	#	#	#	#	Check Code	0xA5 (Enable Key)	--
0x0002	#	#	#	#	#	#	--	--	PSR	RES[1:0], REG, KW/R, UD, SHL	0x0F
0x0003	--	--	#	#	--	--	--	--	PFS	T_VDS_OF[1:0]	0x00
0x0004	#	#	#	#	#	#	#	#	BTST	BT_PHA[7:0]	0x17
0x0005	#	#	#	#	#	#	#	#		BT_PHB[7:0]	0x17
0x0006	--	--	#	#	#	#	#	#		BT_PHC[5:0]	0x17
0x0007	#	--	--	--	#	#	#	#	TSE	TSE, TO[3:0]	0x00
0x0008	#	#	#	#	#	#	#	#	CDI	VBD[1:0], DDX[1:0], CDI[3:0]	0xD7
0x0009	#	#	#	#	#	#	#	#	TCON	S2G[3:0], G2S[3:0]	0x22
0x000A	#	#	#	#	#	0	0	0	TRES	HRES[7:3]	0x00
0x000B	--	--	--	--	--	--	--	#		VRES[8:0]	0x00
0x000C	#	#	#	#	#	#	#	#			0x00
0x000D	#	#	#	#	#	0	0	0	GSST	HST[7:3]	0x00
0x000E	--	--	--	--	--	--	--	#		VST[8:0]	0x00
0x000F	#	#	#	#	#	#	#	#			0x00
0x0010	--	--	--	--	--	--	#	#	CCSET	TSFIX,CCEN	0x00
0x0011	#	#	#	#	#	#	#	#	PWS	VCOM_W[3:0], SD_W[3:0]	0x00
0x0012	--	--	--	--	--	--	#	#	LVSEL	LVD_SEL[1:0]	0x03
0x0013	#	#	#	#	#	#	#	#	TSSET	TS_SET[7:0]	0x00

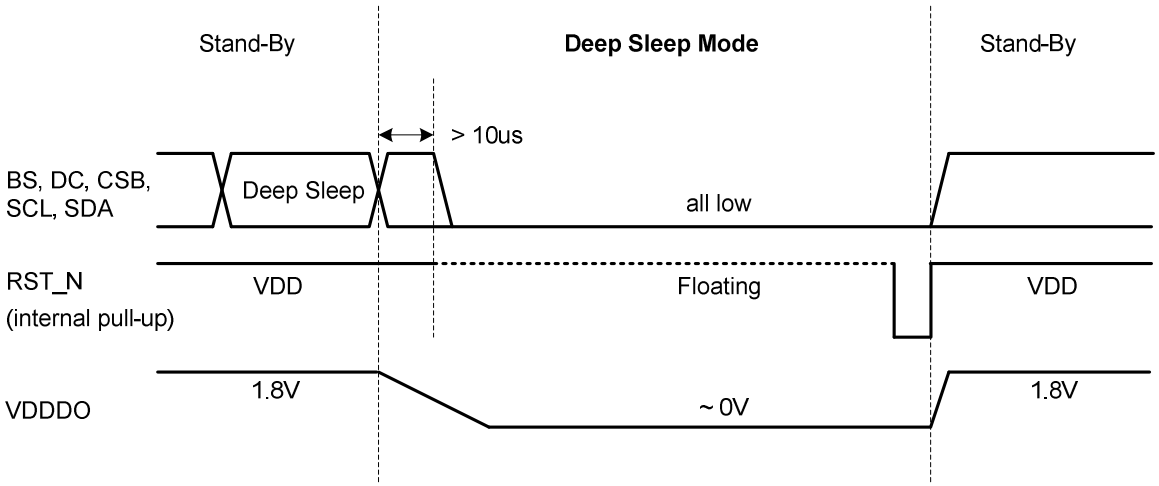
LUT FORMAT IN OTP

There are 16 TRs (temperature range) in a bank. Each TR has independant frame rate, voltage, XON settings and LUTs. The fomat of LUT is different in different mode. In KWR mode, there are only 4 LUTs including LUTC, LUTR, LUTW and LUTK in TRs. In KW mode, there are 5 LUTs including LUT, LUTWW, LUTKW, LUTWK and LUTKK in TRs. All LUTs have same number of state.

<table>
<tr><td rowspan="20">TR0</td><td colspan="10">KWR Mode (KW/R=0)</td><td colspan="10">KWR Mode (KW/R=1)</td></tr>
<tr><td>Address</td><td>D7</td><td>D6</td><td>D5</td><td colspan="2">D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Address</td><td>D7</td><td>D6</td><td>D5</td><td colspan="2">D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>0x002A</td><td>0</td><td>0</td><td>0</td><td colspan="5">Frame Rate[4:0]</td><td>0x002A</td><td>0</td><td>0</td><td>0</td><td colspan="5">Frame Rate[4:0]</td></tr>
<tr><td>0x002B</td><td>0</td><td>0</td><td>0</td><td colspan="2">VCOM_SLEW</td><td colspan="4">VG Voltage[3:0]</td><td>0x002B</td><td>0</td><td>0</td><td>0</td><td colspan="2">VCOM_SLEW</td><td colspan="4">VG Voltage[3:0]</td></tr>
<tr><td>0x002C</td><td>0</td><td>0</td><td colspan="7">VSH Voltage[5:0]</td><td>0x002C</td><td>0</td><td>0</td><td colspan="7">VSH Voltage[5:0]</td></tr>
<tr><td>0x002D</td><td>0</td><td>0</td><td colspan="7">VSL Voltage[5:0]</td><td>0x002D</td><td>0</td><td>0</td><td colspan="7">VSL Voltage[5:0]</td></tr>
<tr><td>0x002E</td><td>0</td><td>0</td><td colspan="7">VDHR Voltage[5:0]</td><td>0x002E</td><td>0</td><td>0</td><td colspan="7">VDHR Voltage[5:0]</td></tr>
<tr><td>0x002F</td><td>0</td><td colspan="9">VCOM_DC Voltage[6:0]</td><td>0x002F</td><td>0</td><td colspan="9">VCOM_DC Voltage[6:0]</td></tr>
<tr><td>0x0030</td><td>EOPT</td><td>ESO</td><td>0</td><td colspan="2">0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0x0030</td><td>EOPT</td><td>ESO</td><td>0</td><td colspan="2">0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0x0031</td><td colspan="9">STATE XON[7:0]</td><td>0x0031</td><td colspan="9">STATE XON[7:0]</td></tr>
<tr><td>0x0032</td><td colspan="9">STATE XON[15:8]</td><td>0x0032</td><td colspan="9">STATE XON[15:8]</td></tr>
<tr><td rowspan="2">0x0033~0x006A</td><td colspan="9" rowspan="2">LUTC
(8 stages)</td><td>0x0033~0x005C</td><td colspan="9">LUTC
(6 stages)</td></tr>
<tr><td>0x005D~0x0086</td><td colspan="9">LUTWW
(6 stages)</td></tr>
<tr><td rowspan="2">0x006B~0x00A2</td><td colspan="9" rowspan="2">LUTR
(8 stages)</td><td>0x0087~0x00B0</td><td colspan="9">LUTKW
(6 stages)</td></tr>
<tr><td>0x00B1~0x00DA</td><td colspan="9">LUTWK
(6 stages)</td></tr>
<tr><td>0x00A3~0x00DA</td><td colspan="9">LUTW
(8 stages)</td><td>0x00DB~0x0104</td><td colspan="9">LUTKK
(6 stages)</td></tr>
<tr><td>0x00DB~0x0112</td><td colspan="9">LUTK
(8 stages)</td><td>0x0105~0x0112</td><td colspan="9">Reserved</td></tr>
</table>

DEEP SLEEP MODE

After deep sleep command (R07H) is transmitted, UC8253 enter “Deep Sleep Mode”, and leaves by RST_N falling. In “Deep Sleep Mode”, the control signals are recommended tied to 0v to avoid IO leakage current. And the die must be keep away from light which causes photoelectric effect to make internal nodes unstable.



PANEL BREAK CHECK

The panel break check (PBC) function is accomplished by testing the connection of the ITO along panel edge. If the panel is broken, the loop ITO may be cut off. The connection check is judged by signal transmission from CHKGO to CHKGI.

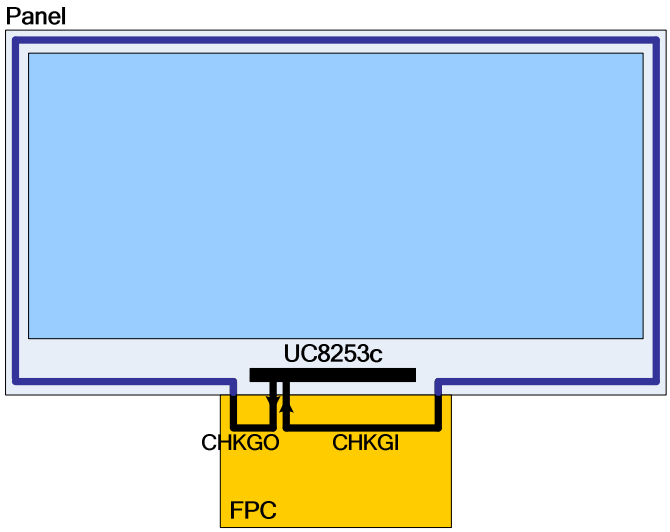


Figure: Panel break check layout example

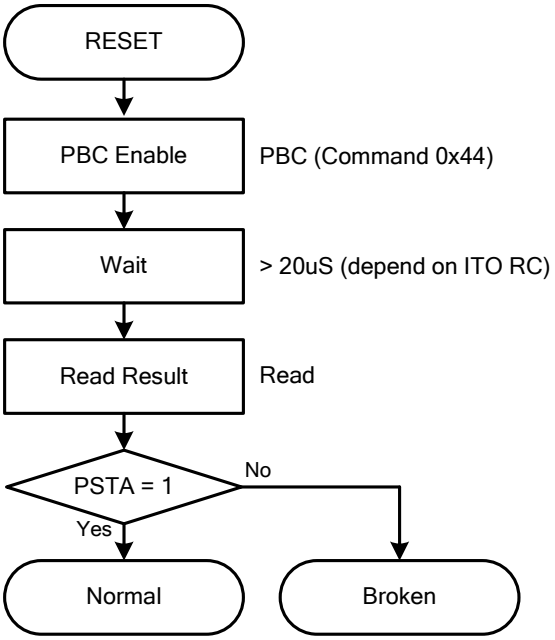
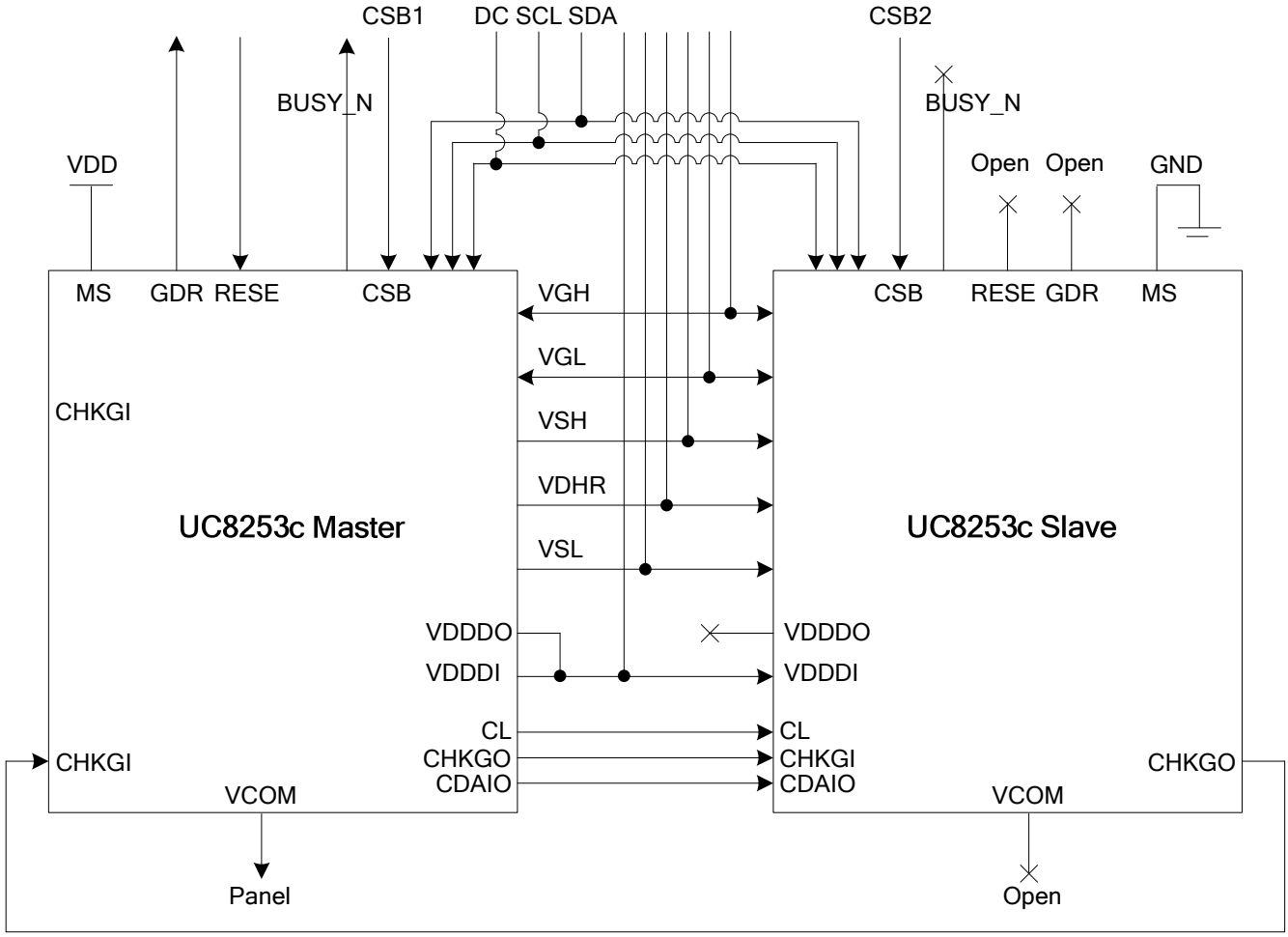


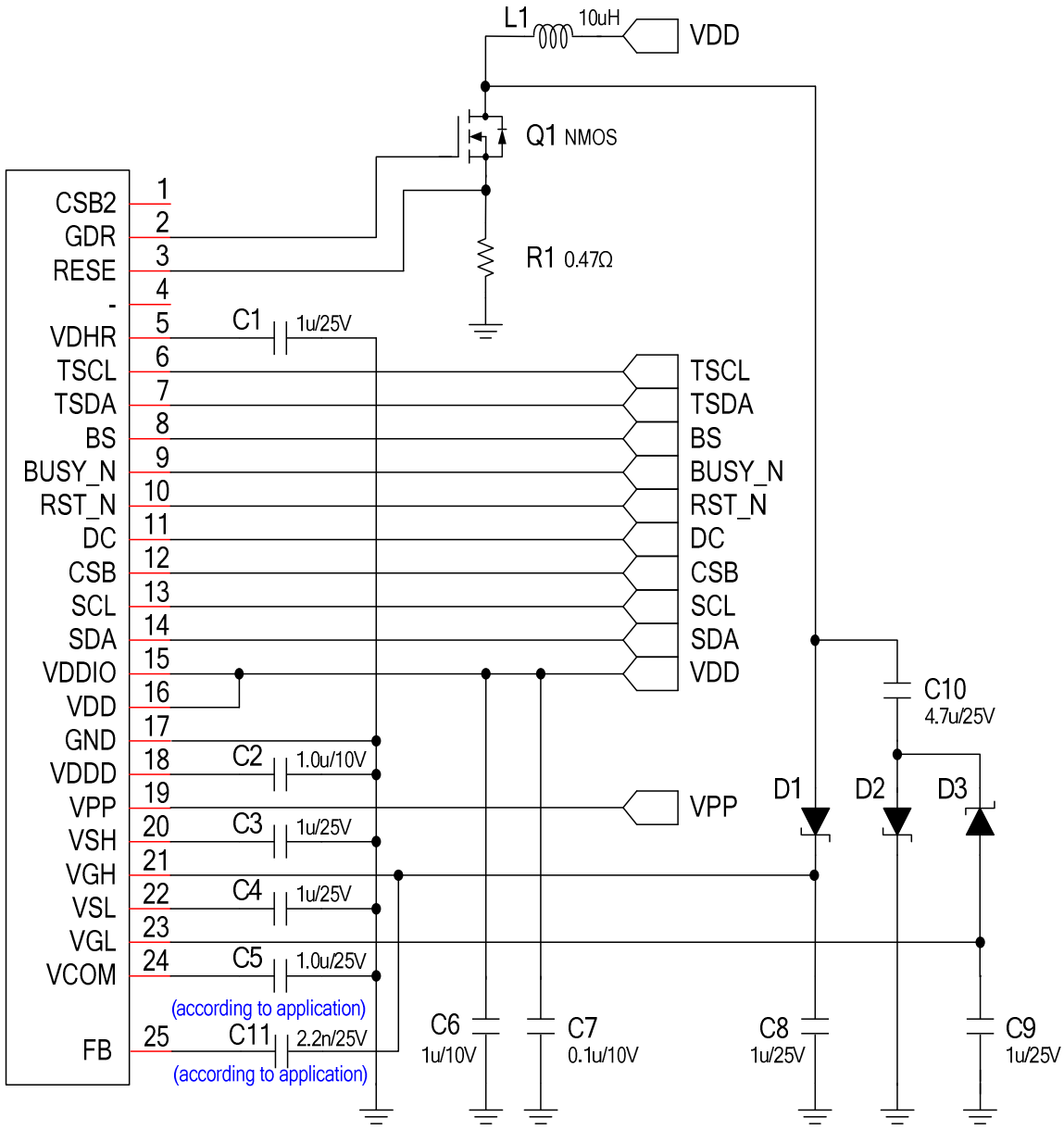
Figure: Panel Break Check (PBC) Sequence

CASCADE APPLICATION CIRCUIT



All commands sent to **Master** must be also sent to **Slave** except for data writing (DTM1 and DTM2). The display data must be separated to two parts, one is for **Master** and another is for **Slave**. They are transmitted to **Master** and **Slave** individually by using CSB1 and CSB2.

BOOSTER APPLICATION CIRCUIT



Note:

The capacitor value of VGH/VGL must be equal or more than the one of VDH/VDL/VDHR.

Recommended Device

Device name	Value	Reference
C1, C3, C4, C5, C8, C9,C10	1uF	X5R/X7R; Voltage Rating : 25V
C2, C6	1uF	X5R/X7R; Voltage Rating : 10V
C7	0.1uF	X5R/X7R; Voltage Rating : 10V
C11	2.2nF	X5R/X7R; Voltage Rating : 25V
R1	0.47 ohm	1% variation, ≥ 0.05W
L1	10uH	Taiyo Yuden NR4018T100M DCR< 0.5 ohm, Isat ≥ 1.2A @ 25° C
D1, D2, D3	Schottky Diode	OnSemi MBR0530 VR> 25V, IF> 500mA, IR< 1mA @ VR= 15V, TA= 100° C
Q1	Switch MOS NMOS	Vishay Si1308EDL VDS> 25V, ID> 500mA, VGS(th)< 1.5VCISS< 200pF, RDS(on)< 400m omh

Recommended Resister

Item	Pins	Resistance
Powers	VDD, VDDA, VDDIO, GND, GNDA, VDM	< 10 Ω
Boosters	VGL, VGH, GDR, RESE	< 10 Ω
Regulators	VSH, VSL, VDHR, VCOM, VDDD, VDDDO	< 10 Ω
Logics	MS, BS, CSB, SCL, SDA, GDR, etc.	< 50 Ω
OTP	VPP	< 20 Ω

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
V_{DD}, V_{DDIO}, V_{DDA}	Logic Supply voltage	-0.3	+6.0	V
V_{PP}	OTP programming voltage	-0.3	+8.5	V
V_I	Digital input range	-0.3	V_{DDIO}+0.3	V
VGH-VGL	Supply range	-	+42.0	V
Source				
VSH	Analog supply voltage – positive	+16		V
VSL	Analog supply voltage -- negative	-16		V
VDHR	Analog supply voltage – positive	+16		V
Gate				
VGH	Analog supply voltage – positive	-0.3	+22	V
VGL	Analog supply voltage -- negative	-22	0.3	V
T_{STG}	Storage temperature range	-55	+125	°C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDDIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDDA	DCDC driver supply voltage		2.3	3.3	3.6	V
VPP	OTP program voltage		8.0	8.25	8.5	V
VIL	LOW Level input voltage	Digital input pins	0	--	0.2xVDDIO	V
VIH	HIGH Level input voltage	Digital input pins	0.8xVDDIO	--	VDDIO	V
VOH	HIGH Level output voltage	Digital input pins, IOH=400uA	0.8xVDDIO	--	--	V
VOL	LOW Level Output voltage	Digital input pins, IOL=-400uA	0	--	0.2xVDDIO	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
RIN	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85	°C
dVGH	VGH Supply voltage dev		-400	0	+400	mV
VGH-VGL	Voltage Range of VGH - VGL		--		40	V
dVSH	Supply voltage dev		-200	0	+200	mV
dVSL	Supply voltage dev		-200	0	+200	mV
dVDHR	Supply voltage dev		-200	0	+200	mV
dVCOM	Supply voltage dev		-200	0	+200	mV
RON	Driver Output Resistance	For source driver, TOP=25°C, VOUT = ±15V		16	38.4	KΩ
		For gate driver, TOP=25°C, VOUT = ±20V		4	8	

VDD=VDDA=VDDIO=3.0V, TOP=25.0 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
IVDD	Digital deep sleep current	VDDD OFF	--	0.3	0.5	uA
	Digital stand-by current	All stopped	--	8.2	40.0	uA
	Digital operating current		--	--	0.1	mA
IVDDIO	IO deep sleep current	VDDD OFF	--	0.1	0.3	uA
	IO stand-by current	Booster OFF	--	2.5	4.0	uA
	IO operating current	No load	--	--	0.1	mA
IVDDA	DCDC deep sleep current	VDDD OFF	--	0.1	0.3	uA
	DCDC stand-by current	Booster OFF	--	15.5	20.0	uA
	DCDC operating current	Source output VDH/VDL, Duty=0.5, Period =125uS VCOM DC No load	--	--	4.0	mA
		Source output VDH/VDL, Duty=0.5, Period =125uS, VCOM DC External cap: 415pF, NMOS=340pF	--	--	20.0	

AC CHARACTERISTICS

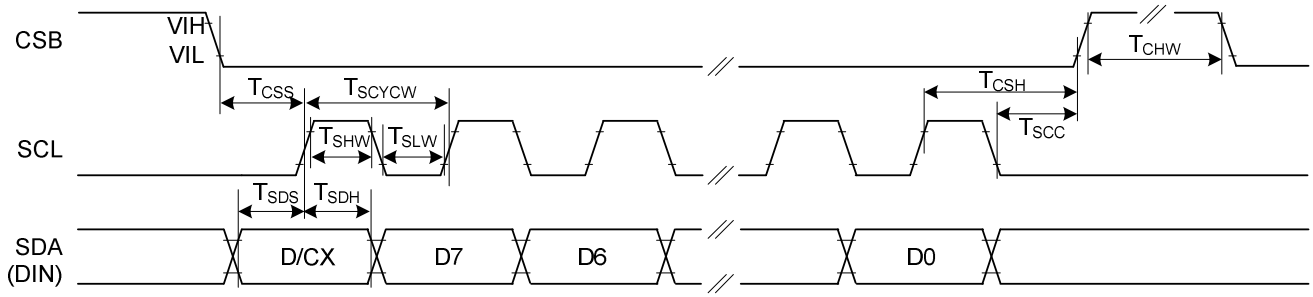


Figure: 3-wire Serial Interface Characteristics (Write mode)

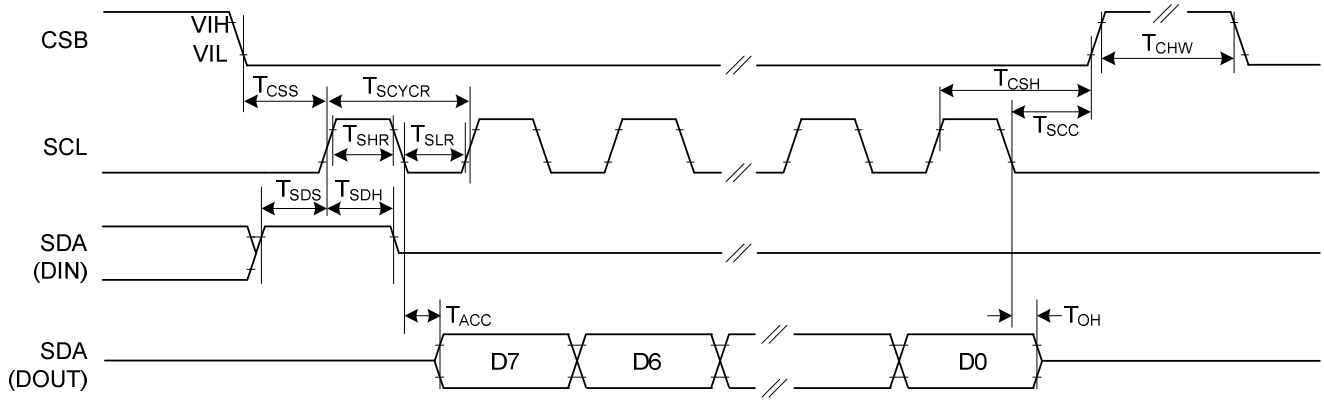


Figure: 3-wire Serial Interface Characteristics (Read mode)

VDD=2.3V

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	170			ns
T_{SHW}		SCL “H” pulse width (Write)	85			ns
T_{SLW}		SCL “L” pulse width (Write)	85			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL “H” pulse width (Read)	175			ns
T_{SLR}		SCL “L” pulse width (Read)	175			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			250	ns
T_{OH}		Output disable time	15			ns

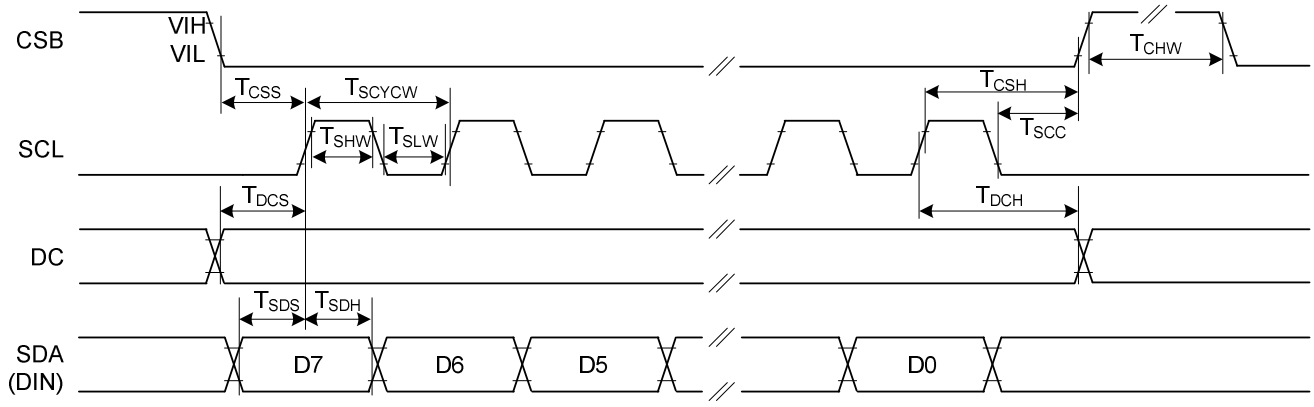


Figure: 4-wire Serial Interface Characteristics (Write mode)

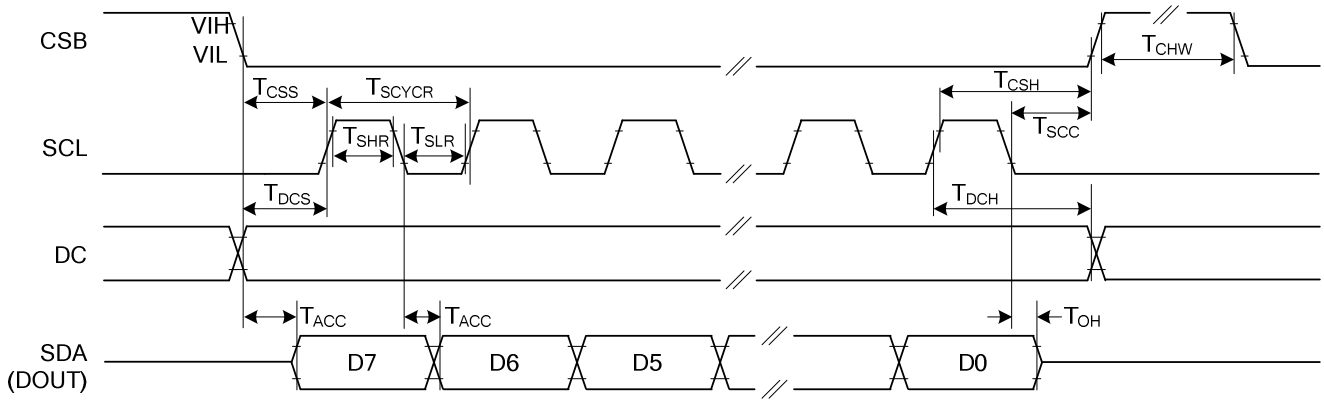


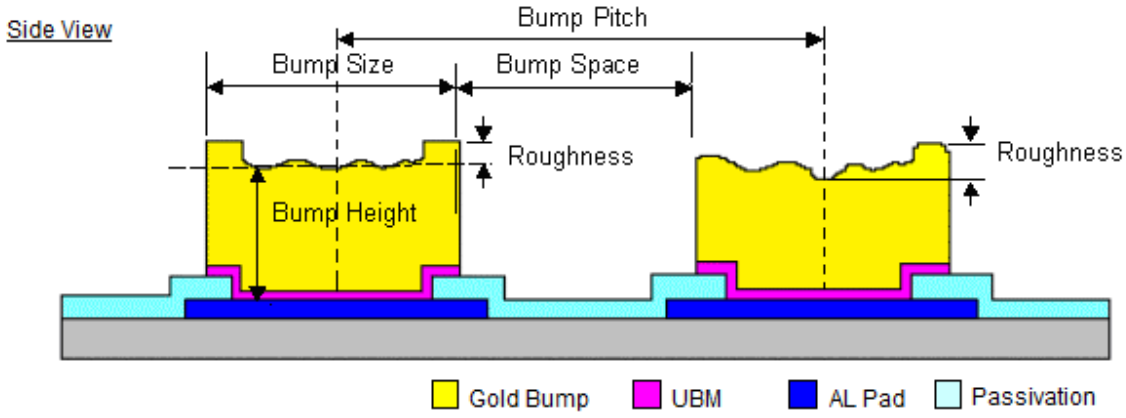
Figure: 4-wire Serial Interface Characteristics (Read mode)

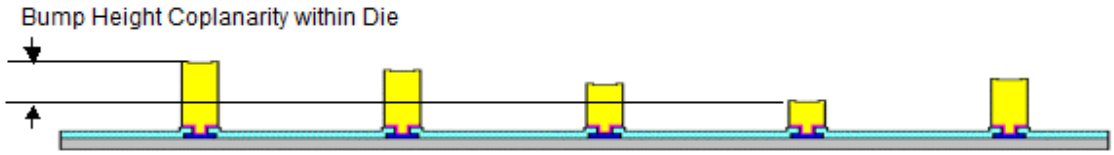
VDD=2.3V

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	170			ns
T_{SHW}		SCL “H” pulse width (Write)	85			ns
T_{SLW}		SCL “L” pulse width (Write)	85			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL “H” pulse width (Read)	175			ns
T_{SLR}		SCL “L” pulse width (Read)	175			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			250	ns
T_{OH}		Output disable time	15			ns

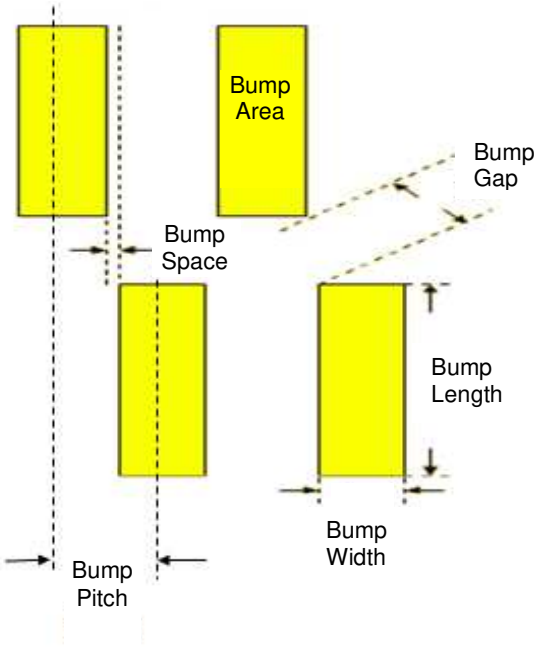
PHYSICAL DIMENSIONS

Die Size:	(11770 μM ± 40μM) x (750 μM ± 40μM)
Die Thickness:	300 μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2μM
Bump Height:	12 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ≤ 2μM
Bump Size:	12 μM x 100 μM ± 3μM
Bump Area:	1200 μM^2
Total bump Area:	1375160μM^2
Bump Pitch:	13μM± 3μM
Bump space:	1 μM ± 3μM
Bump Gap:	19 μM ± 3μM
Hardness:	65 Hv ± 15Hv
Shear:	≥ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center



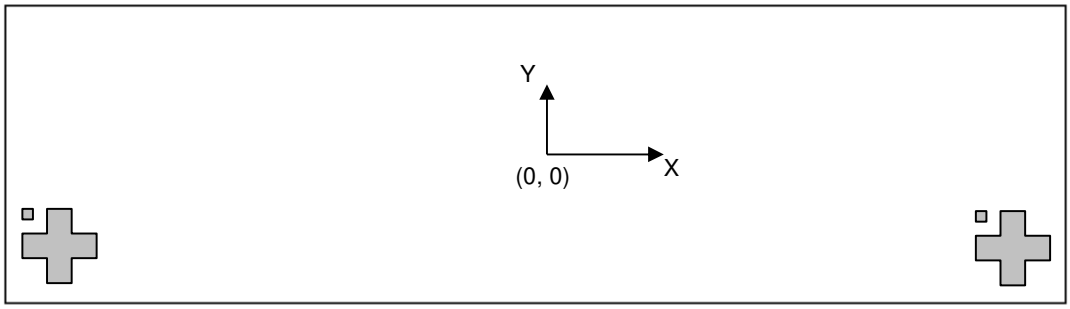


For Stagger Layout



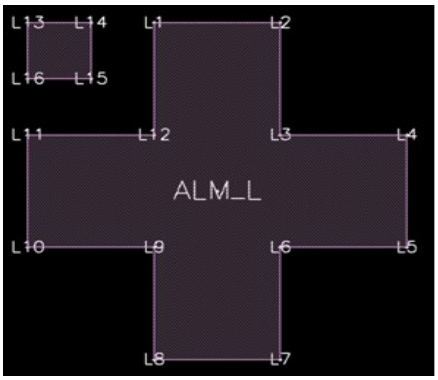
ALIGNMENT MARK INFORMATION

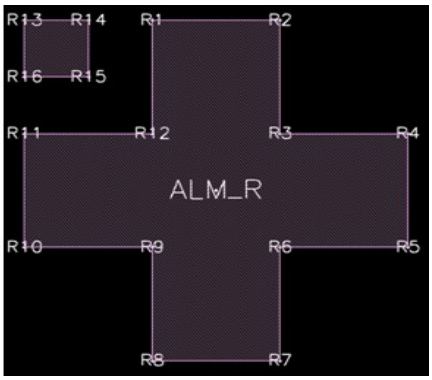
Location:



D-Left Mark D-Right Mark

Shapes and Points:





Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-5765	-185	5765	-185
1	-5775	-155	5755	-155
2	-5755	-155	5775	-155
3	-5755	-175	5775	-175
4	-5735	-175	5795	-175
5	-5735	-195	5795	-195
6	-5755	-195	5775	-195
7	-5755	-215	5775	-215
8	-5775	-215	5755	-215
9	-5775	-195	5755	-195
10	-5795	-195	5735	-195
11	-5795	-175	5735	-175
12	-5775	-175	5755	-175
13	-5795	-155	5735	-155
14	-5785	-155	5745	-155
15	-5785	-165	5745	-165
16	-5795	-165	5735	-165

PAD COORDINATES

#	Pad	X	Y	W	H
1	NC<0>	-5750	-308	28	70
2	VCOM	-5704	-308	28	70
3	VCOM	-5658	-308	28	70
4	VCOM	-5612	-308	28	70
5	VCOM	-5566	-308	28	70
6	VCOM	-5520	-308	28	70
7	VCOM	-5474	-308	28	70
8	VCOM	-5428	-308	28	70
9	VCOM	-5382	-308	28	70
10	VDM	-5336	-308	28	70
11	DUMMY<0>	-5290	-308	28	70
12	DUMMY<1>	-5244	-308	28	70
13	DUMMY<2>	-5198	-308	28	70
14	DUMMY<3>	-5152	-308	28	70
15	DUMMY<4>	-5106	-308	28	70
16	DUMMY<5>	-5060	-308	28	70
17	DUMMY<6>	-5014	-308	28	70
18	DUMMY<7>	-4968	-308	28	70
19	DUMMY<8>	-4922	-308	28	70
20	DUMMY<9>	-4876	-308	28	70
21	DUMMY<10>	-4830	-308	28	70
22	DUMMY<11>	-4784	-308	28	70
23	DUMMY<12>	-4738	-308	28	70
24	DUMMY<13>	-4692	-308	28	70
25	DUMMY<14>	-4646	-308	28	70
26	DUMMY<15>	-4600	-308	28	70
27	DUMMY<16>	-4554	-308	28	70
28	VGL	-4508	-308	28	70
29	VGL	-4462	-308	28	70
30	VGL	-4416	-308	28	70
31	VGL	-4370	-308	28	70
32	VGL	-4324	-308	28	70
33	VGL	-4278	-308	28	70
34	VGL	-4232	-308	28	70
35	VGL	-4186	-308	28	70
36	VGL	-4140	-308	28	70
37	VGL	-4094	-308	28	70
38	VGL	-4048	-308	28	70
39	VGL	-4002	-308	28	70
40	VGL	-3956	-308	28	70
41	VGL	-3910	-308	28	70
42	VGL	-3864	-308	28	70
43	VGL	-3818	-308	28	70
44	GND	-3772	-308	28	70
45	VSL	-3726	-308	28	70
46	VSL	-3680	-308	28	70
47	VSL	-3634	-308	28	70
48	VSL	-3588	-308	28	70
49	VSL	-3542	-308	28	70
50	VSL	-3496	-308	28	70
51	VSL	-3450	-308	28	70
52	VSL	-3404	-308	28	70
53	VSL	-3358	-308	28	70
54	VSL	-3312	-308	28	70
55	GND	-3266	-308	28	70
56	VGH	-3220	-308	28	70

#	Pad	X	Y	W	H
57	VGH	-3174	-308	28	70
58	VGH	-3128	-308	28	70
59	VGH	-3082	-308	28	70
60	VGH	-3036	-308	28	70
61	VGH	-2990	-308	28	70
62	VGH	-2944	-308	28	70
63	VGH	-2898	-308	28	70
64	VGH	-2852	-308	28	70
65	VGH	-2806	-308	28	70
66	VGH	-2760	-308	28	70
67	VGH	-2714	-308	28	70
68	GND	-2668	-308	28	70
69	VSH	-2622	-308	28	70
70	VSH	-2576	-308	28	70
71	VSH	-2530	-308	28	70
72	VSH	-2484	-308	28	70
73	VSH	-2438	-308	28	70
74	VSH	-2392	-308	28	70
75	VSH	-2346	-308	28	70
76	VSH	-2300	-308	28	70
77	VSH	-2254	-308	28	70
78	VSH	-2208	-308	28	70
79	GND	-2162	-308	28	70
80	VPP	-2116	-308	28	70
81	VPP	-2070	-308	28	70
82	VPP	-2024	-308	28	70
83	VPP	-1978	-308	28	70
84	VPP	-1932	-308	28	70
85	VPP	-1886	-308	28	70
86	VDDD	-1840	-308	28	70
87	VDDD	-1794	-308	28	70
88	VDDD	-1748	-308	28	70
89	VDDD	-1702	-308	28	70
90	VDDDO	-1656	-308	28	70
91	VDDDO	-1610	-308	28	70
92	VDDDO	-1564	-308	28	70
93	VDDDO	-1518	-308	28	70
94	VDM	-1472	-308	28	70
95	VDM	-1426	-308	28	70
96	GND	-1380	-308	28	70
97	GND	-1334	-308	28	70
98	GND	-1288	-308	28	70
99	GND	-1242	-308	28	70
100	GND	-1196	-308	28	70
101	GND	-1150	-308	28	70
102	GND	-1104	-308	28	70
103	GND	-1058	-308	28	70
104	GND	-1012	-308	28	70
105	GND	-966	-308	28	70
106	GND	-920	-308	28	70
107	GND	-874	-308	28	70
108	GNDA	-828	-308	28	70
109	GNDA	-782	-308	28	70
110	GNDA	-736	-308	28	70
111	GNDA	-690	-308	28	70
112	GNDA	-644	-308	28	70

#	Pad	X	Y	W	H
113	GNDA	-598	-308	28	70
114	GNDA	-552	-308	28	70
115	GNDA	-506	-308	28	70
116	GNDA	-460	-308	28	70
117	GNDA	-414	-308	28	70
118	VDDA	-368	-308	28	70
119	VDDA	-322	-308	28	70
120	VDDA	-276	-308	28	70
121	VDDA	-230	-308	28	70
122	VDDA	-184	-308	28	70
123	VDDA	-138	-308	28	70
124	VDDA	-92	-308	28	70
125	VDDA	-46	-308	28	70
126	VDDA	0	-308	28	70
127	VDDA	46	-308	28	70
128	VDD	92	-308	28	70
129	VDD	138	-308	28	70
130	VDD	184	-308	28	70
131	VDD	230	-308	28	70
132	VDD	276	-308	28	70
133	VDD	322	-308	28	70
134	VDD	368	-308	28	70
135	DUMMY<17>	414	-308	28	70
136	DUMMY<18>	460	-308	28	70
137	DUMMY<19>	506	-308	28	70
138	DUMMY<20>	552	-308	28	70
139	DUMMY<21>	598	-308	28	70
140	DUMMY<22>	644	-308	28	70
141	DUMMY<23>	690	-308	28	70
142	DUMMY<24>	736	-308	28	70
143	TEST1	782	-308	28	70
144	DUMMY<25>	828	-308	28	70
145	TEST2	874	-308	28	70
146	DUMMY<26>	920	-308	28	70
147	DUMMY<27>	966	-308	28	70
148	DUMMY<28>	1012	-308	28	70
149	M1M2_SYNC	1058	-308	28	70
150	DUMMY<29>	1104	-308	28	70
151	DUMMY<30>	1150	-308	28	70
152	MM	1196	-308	28	70
153	DUMMY<31>	1242	-308	28	70
154	DUMMY<32>	1288	-308	28	70
155	VDDIO	1334	-308	28	70
156	VDDIO	1380	-308	28	70
157	VDDIO	1426	-308	28	70
158	VDDIO	1472	-308	28	70
159	TEST3	1518	-308	28	70
160	DUMMY<33>	1564	-308	28	70
161	SDA	1610	-308	28	70
162	DUMMY<34>	1656	-308	28	70
163	DUMMY<35>	1702	-308	28	70
164	SCL	1748	-308	28	70
165	GND	1794	-308	28	70
166	CSB	1840	-308	28	70
167	VDDIO	1886	-308	28	70
168	DUMMY<36>	1932	-308	28	70
169	GND	1978	-308	28	70
170	DC	2024	-308	28	70
171	VDDIO	2070	-308	28	70

#	Pad	X	Y	W	H
172	DUMMY<37>	2116	-308	28	70
173	GND	2162	-308	28	70
174	RST_N	2208	-308	28	70
175	DUMMY<38>	2254	-308	28	70
176	BUSY_N	2300	-308	28	70
177	DUMMY<39>	2346	-308	28	70
178	CL	2392	-308	28	70
179	VDDIO	2438	-308	28	70
180	VSYNC	2484	-308	28	70
181	GND	2530	-308	28	70
182	DUMMY<40>	2576	-308	28	70
183	VDDIO	2622	-308	28	70
184	BS	2668	-308	28	70
185	GND	2714	-308	28	70
186	DUMMY<41>	2760	-308	28	70
187	VDDIO	2806	-308	28	70
188	CHKGI	2852	-308	28	70
189	GND	2898	-308	28	70
190	MS	2944	-308	28	70
191	VDDIO	2990	-308	28	70
192	DUMMY<42>	3036	-308	28	70
193	TSDA	3082	-308	28	70
194	TSDA	3128	-308	28	70
195	TSCL	3174	-308	28	70
196	TSCL	3220	-308	28	70
197	DUMMY<43>	3266	-308	28	70
198	DUMMY<44>	3312	-308	28	70
199	CHKGO	3358	-308	28	70
200	DUMMY<45>	3404	-308	28	70
201	CDAIO	3450	-308	28	70
202	DUMMY<46>	3496	-308	28	70
203	TEST6	3542	-308	28	70
204	DUMMY<47>	3588	-308	28	70
205	TEST7	3634	-308	28	70
206	DUMMY<48>	3680	-308	28	70
207	DUMMY<49>	3726	-308	28	70
208	DUMMY<50>	3772	-308	28	70
209	DUMMY<51>	3818	-308	28	70
210	DUMMY<52>	3864	-308	28	70
211	DUMMY<53>	3910	-308	28	70
212	DUMMY<54>	3956	-308	28	70
213	VDHR	4002	-308	28	70
214	VDHR	4048	-308	28	70
215	VDHR	4094	-308	28	70
216	VDHR	4140	-308	28	70
217	VDHR	4186	-308	28	70
218	VDHR	4232	-308	28	70
219	VDHR	4278	-308	28	70
220	VDHR	4324	-308	28	70
221	DUMMY<55>	4370	-308	28	70
222	DUMMY<56>	4416	-308	28	70
223	DUMMY<57>	4462	-308	28	70
224	DUMMY<58>	4508	-308	28	70
225	GND	4554	-308	28	70
226	FB	4600	-308	28	70
227	FB	4646	-308	28	70
228	GND	4692	-308	28	70
229	RESE	4738	-308	28	70
230	RESE	4784	-308	28	70

#	Pad	X	Y	W	H
231	GND	4830	-308	28	70
232	DUMMY<59>	4876	-308	28	70
233	DUMMY<60>	4922	-308	28	70
234	GDR	4968	-308	28	70
235	GDR	5014	-308	28	70
236	GDR	5060	-308	28	70
237	GDR	5106	-308	28	70
238	GDR	5152	-308	28	70
239	GDR	5198	-308	28	70
240	GDR	5244	-308	28	70
241	GDR	5290	-308	28	70
242	VDM	5336	-308	28	70
243	VCOM	5382	-308	28	70
244	VCOM	5428	-308	28	70
245	VCOM	5474	-308	28	70
246	VCOM	5520	-308	28	70
247	VCOM	5566	-308	28	70
248	VCOM	5612	-308	28	70
249	VCOM	5658	-308	28	70
250	VCOM	5704	-308	28	70
251	NC<1>	5750	-308	28	70
252	NC<2>	5833	308	12	100
253	NC<3>	5816	189	12	100
254	GD<0>	5799	308	12	100
255	G<0>	5782	189	12	100
256	G<2>	5765	308	12	100
257	G<4>	5748	189	12	100
258	G<6>	5731	308	12	100
259	G<8>	5714	189	12	100
260	G<10>	5697	308	12	100
261	G<12>	5680	189	12	100
262	G<14>	5663	308	12	100
263	G<16>	5646	189	12	100
264	G<18>	5629	308	12	100
265	G<20>	5612	189	12	100
266	G<22>	5595	308	12	100
267	G<24>	5578	189	12	100
268	G<26>	5561	308	12	100
269	G<28>	5544	189	12	100
270	G<30>	5527	308	12	100
271	G<32>	5510	189	12	100
272	G<34>	5493	308	12	100
273	G<36>	5476	189	12	100
274	G<38>	5459	308	12	100
275	G<40>	5442	189	12	100
276	G<42>	5425	308	12	100
277	G<44>	5408	189	12	100
278	G<46>	5391	308	12	100
279	G<48>	5374	189	12	100
280	G<50>	5357	308	12	100
281	G<52>	5340	189	12	100
282	G<54>	5323	308	12	100
283	G<56>	5306	189	12	100
284	G<58>	5289	308	12	100
285	G<60>	5272	189	12	100
286	G<62>	5255	308	12	100
287	G<64>	5238	189	12	100
288	G<66>	5221	308	12	100
289	G<68>	5204	189	12	100

#	Pad	X	Y	W	H
290	G<70>	5187	308	12	100
292	G<74>	5153	308	12	100
293	G<76>	5136	189	12	100
294	G<78>	5119	308	12	100
295	G<80>	5102	189	12	100
296	G<82>	5085	308	12	100
297	G<84>	5068	189	12	100
298	G<86>	5051	308	12	100
299	G<88>	5034	189	12	100
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443	G<376>	2586	189	12	100
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473	G<436>	2076	189	12	100
474	G<438>	2059	308	12	100
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476	G<442>	2025	308	12	100
477	G<444>	2008	189	12	100
478	G<446>	1991	308	12	100
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487	G<464>	1838	189	12	100
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491	G<472>	1770	189	12	100
492	G<474>	1753	308	12	100
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546	S<46>	955.5	308	12	100
547	S<47>	942.5	189	12	100
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563	S<63>	734.5	189	12	100
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566	S<66>	695.5	308	12	100
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602	S<102>	227.5	308	12	100
603	S<103>	214.5	189	12	100
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605	S<105>	188.5	189	12	100
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607	S<107>	162.5	189	12	100
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624	S<124>	-58.5	308	12	100
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640	S<140>	-266.5	308	12	100
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650	S<150>	-396.5	308	12	100
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653	S<153>	-435.5	189	12	100
654	S<154>	-448.5	308	12	100
655	S<155>	-461.5	189	12	100
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657	S<157>	-487.5	189	12	100
658	S<158>	-500.5	308	12	100
659	S<159>	-513.5	189	12	100
660	S<160>	-526.5	308	12	100
661	S<161>	-539.5	189	12	100
662	S<162>	-552.5	308	12	100
663	S<163>	-565.5	189	12	100
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665	S<165>	-591.5	189	12	100
666	S<166>	-604.5	308	12	100
667	S<167>	-617.5	189	12	100
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670	S<170>	-656.5	308	12	100
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693	S<193>	-955.5	189	12	100
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698	S<198>	-1020.5	308	12	100
699	S<199>	-1033.5	189	12	100
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702	S<202>	-1072.5	308	12	100
703	S<203>	-1085.5	189	12	100

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710	S<210>	-1176.5	308	12	100
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712	S<212>	-1202.5	308	12	100
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715	S<215>	-1241.5	189	12	100
716	S<216>	-1254.5	308	12	100
717	S<217>	-1267.5	189	12	100
718	S<218>	-1280.5	308	12	100
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720	S<220>	-1306.5	308	12	100
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724	S<224>	-1358.5	308	12	100
725	S<225>	-1371.5	189	12	100
726	S<226>	-1384.5	308	12	100
727	S<227>	-1397.5	189	12	100
728	S<228>	-1410.5	308	12	100
729	S<229>	-1423.5	189	12	100
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840	G<289>	-3334	308	12	100
841	G<287>	-3351	189	12	100
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847	G<275>	-3453	189	12	100
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#	Pad	X	Y	W	H
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892	G<185>	-4218	308	12	100
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#	Pad	X	Y	W	H
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969	G<31>	-5527	189	12	100
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980	G<9>	-5714	308	12	100
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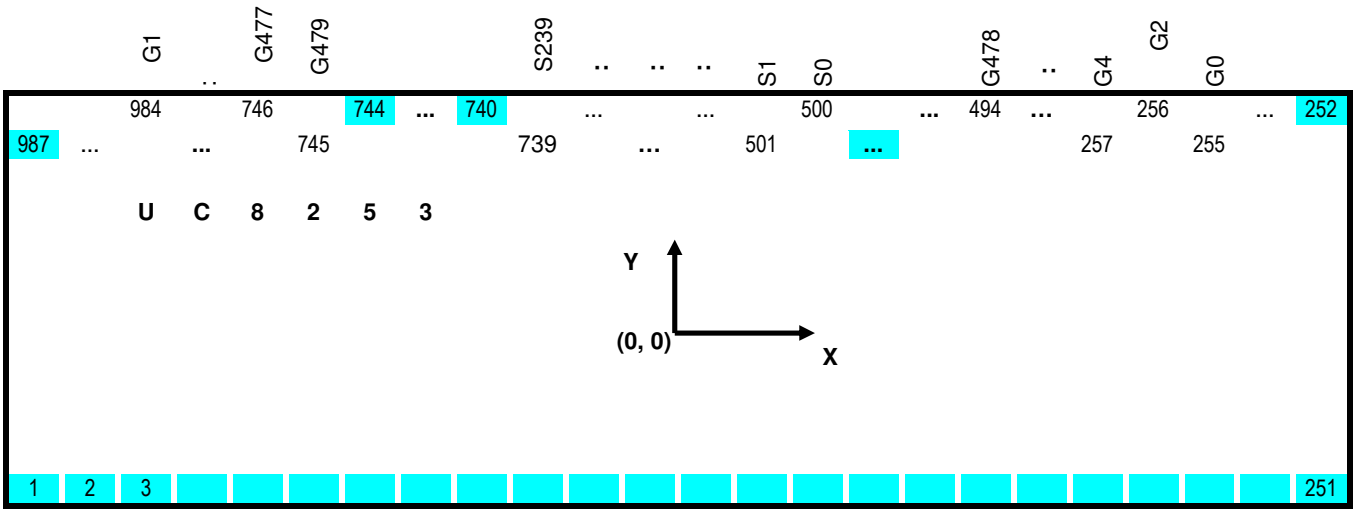
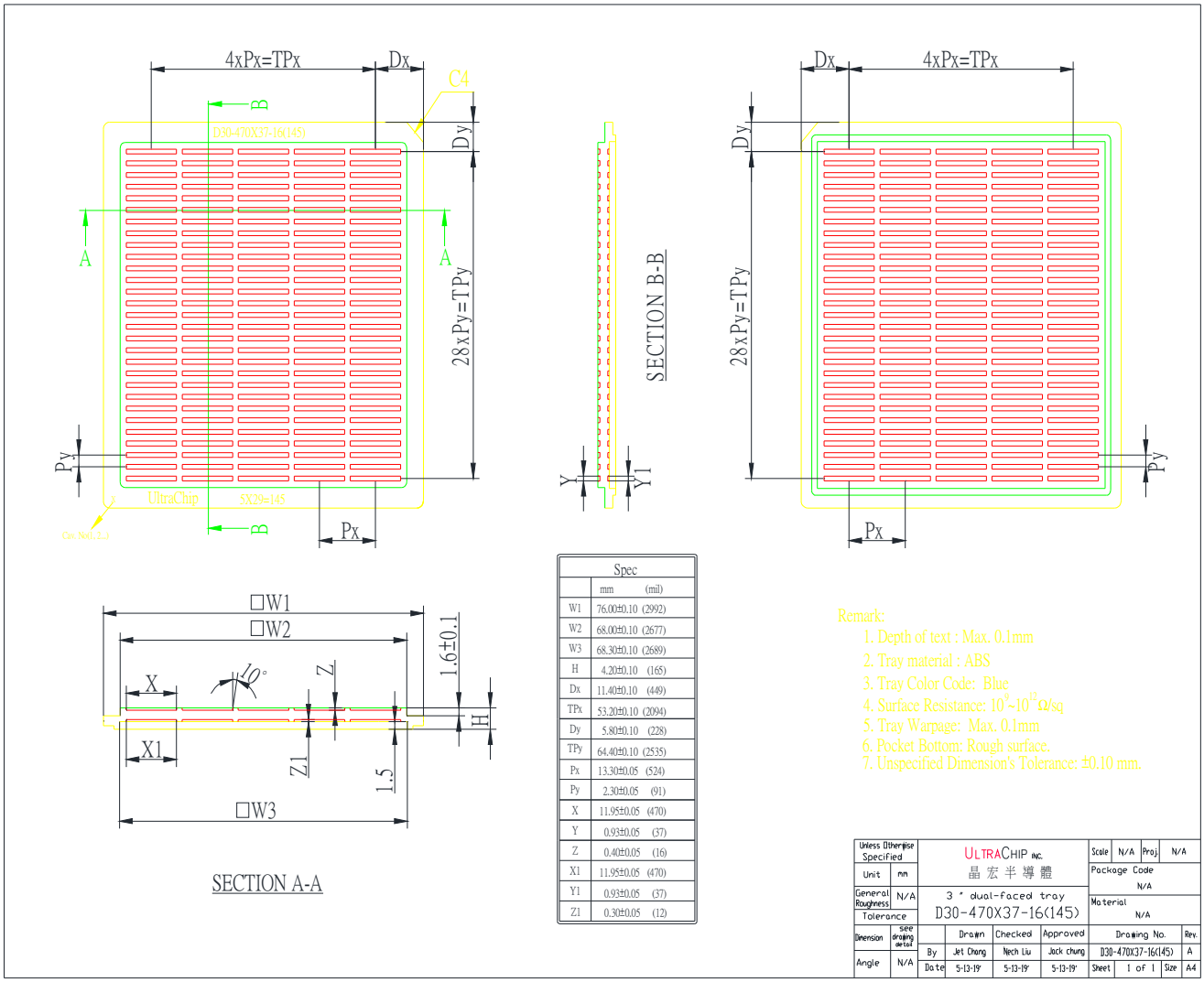
Output Pad Location



TRAY INFORMATION

3 Inch Tray



Spec		
	mm	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
H	4.20±0.10	(165)
Dx	11.40±0.10	(449)
TPx	53.20±0.10	(2094)
Dy	5.80±0.10	(228)
TPy	64.40±0.10	(2535)
Px	13.30±0.05	(524)
Py	2.30±0.05	(91)
X	11.95±0.05	(470)
Y	0.93±0.05	(37)
Z	0.40±0.05	(16)
X1	11.95±0.05	(470)
Y1	0.93±0.05	(37)
Z1	0.30±0.05	(12)

Unless Otherwise Specified		ULTRACHIP INC. 晶宏半導體			Scale N/A	Proj. N/A
Unit	mm				Package Code N/A	
General Roughness	N/A	3 " dual-faced tray D30-470X37-16(145)			Material N/A	
Tolerance						
Dimension	see drawing detail		Drawn	Checked	Approved	Drawing No. D30-470X37-16(145) Rev. A
Angle	N/A	By	Jet Chang	Nech Liu	Jack chung	
		Date	5-13-19'	5-13-19'	5-13-19'	Sheet 1 of 1 Size A4

REVISION HISTORY

Revision	Contents	Date
0.1	NA	May 7,2019
0.2	Revise Feature Highlights、Physical Dimensions、Alignment Mark Information、Tray Information	Fed 13 2020
0.3	Revise R22H、LUT Format	Apr 29 2020
0.4	1.revise “FB” Pin description 2.revise Booster Application Circuit_ ‘’C1、C3、C4、C6、C8” 3.revise DC Characteristics 4.revise 3/4-wire Serial Interface Characteristics	Jun 29 2020
0.6	Page 14. Revise PSR description Page 52. Revise LUT Format in OTP Page 56. Revise Booster Application Circuit Page 60&61. Revise 3/4-wire Serial Interface Characteristics	Oct 13 2020
0.61	P11 Add Command Table RA3H P14 Revise command PSR(R00H) description P39 Add Command PGAR(RA3H) description	Nov 25,2020