APPLICATION NOTE – REFERENCE DESIGN

MODEL NAME：7.3inch e-Paper (F)

1 About This Application Note

This document describes a reference design system that integrates the N-color (black, white, red, yellow, orange, green and blue) 7.3” display. It includes an application circuit, timing information, pin assignments and software programming guide for the ePaper display module.

2 Overview

This 7.3” panel is a 800x480 ePaper display with integrated timing control and power management circuitry. Each pixel on the display has the capability of showing 7 states –black, white, red, yellow, orange, green and blue. The7.3” panel is ideal for applications such as signage for retail pricing with the ability to highlight promotions.

3 Device Interface

This section describes the interface and pin assignments of the 7.3” panel.

Table 1 Pin descriptions for7.3” panel

Pin Assignment				
Pin#	**Type**	**Signal**	**Description**	**Remark**
1		NC	No connection and do not connect with other NC pins	
2	P	TFT_VCOM	TFT_VCOM driving voltage	
3	P	FPL_VCOM	FPL_VCOM driving voltage	
4		NC	NC	
5	I/O	GDRH	N-Channel MOSFET Gate Drive Control	
6	I/O	RESEH	Current Sense Input for the Control Loop	
7		GDRL	Reserved	
8	P	GND	Ground	
9	I/O	GDRC	P-Channel MOSFET Gate Drive Control	
10	I/O	RESEC	Current Sense Input for the Control Loop	
11	P	VPC	VPC driving voltage	
12	P	GND	Ground	
13	P	VGL	Negative Gate driving voltage	
14	P	VPH	VPH driving voltage	
15	P	VSH	Positive Source driving voltage	
16	P	VSH_LV	Positive Source driving voltage	
17	P	VSH_LV2	Positive Source driving voltage	
18	P	VSL	Negative Source driving voltage	
19	P	VSL_LV	Negative Source driving voltage	
20	P	VSL_LV2	Negative Source driving voltage	
21	P	GNDA	Ground ; Connect to GND	
22		REFN	Reserved	
23		REFP	Reserved	
24	O	TSCL	I2C Interface to digital temperature sensor Clock pin	
25	I/O	TSDA	I2C Interface to digital temperature sensor Data pin	
26	I	BS0	Bus selection pin; L: 4-wire IF. H: 3-wire IF. (Default)	
27	I	BS1	Bus selection pin; L: refer to BS0. (Default) H: Standard 4-wire SPI/dual SPI/quad SPI	
28	I	RES#	Reset	
29	O	BUSY_N	Busy state output pin	

30	I	D/C#	Data /Command control pin (D/C)	
31	I	CS#	Chip Select input pin (CSB)	
32	I	SCL	Serial clock pin (SPI)	
33	I/O	SI0	serial data pin (SPI)	
34	I/O	SI1	serial data pin ; Reserved	
35	I/O	SI2	serial data pin ; Reserved	
36	I/O	SI3	serial data pin ; Reserved	
37	P	VDDDO	Core logic power pin; Connect to VDDD	
38	P	VDD	Supply voltage	
39	P	GND	Ground; Connect to GNDA	
40	P	VDDIO	Supply voltage	
41	P	VCP2	Charge Pump Pin	
42	P	CP2N	Charge Pump Pin	
43	P	CP2P	Charge Pump Pin	
44	P	VCP1	Charge Pump Pin	
45	P	CP1N	Charge Pump Pin	
46	P	CP1P	Charge Pump Pin	
47		CGH1N	Charge Pump Pin; Reserved	
48		CGH1P	Charge Pump Pin; Reserved	
49	P	VGH	Positive Gate driving voltage	
50	P	VCOMBD	VCOMBD driving voltage	

I: Input Pin; O: Output Pin; I/O: Input/Out Pin; P: Power Pin

3.1 SPI Interface Timing

Figure 1 3-wire SPI Timing Diagram

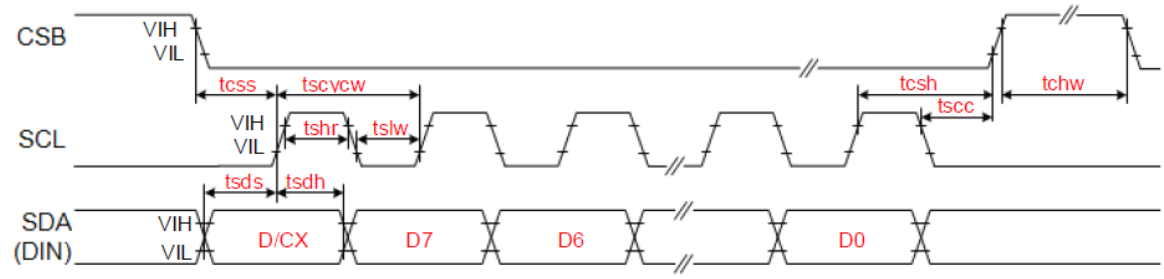


Figure : 3-wire Serial Interface – Write

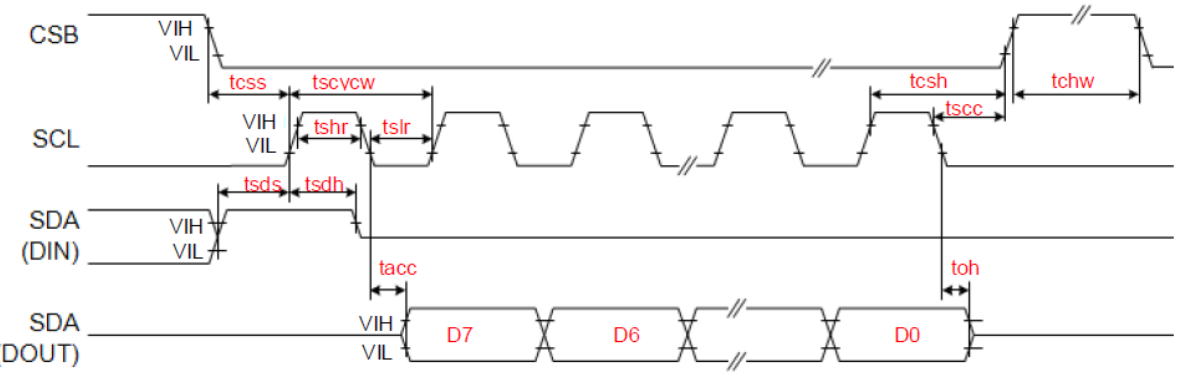


Figure : 3-wire Serial Interface – Read

Figure 2 Host Communications Timing Diagram

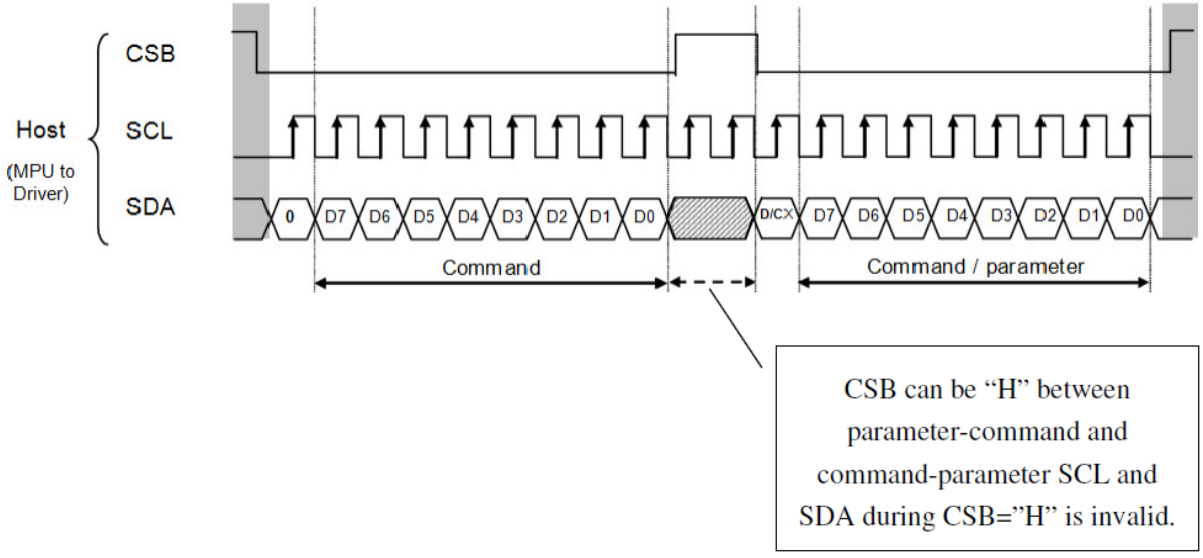


Figure 3 4-wire SPI Timing Diagram

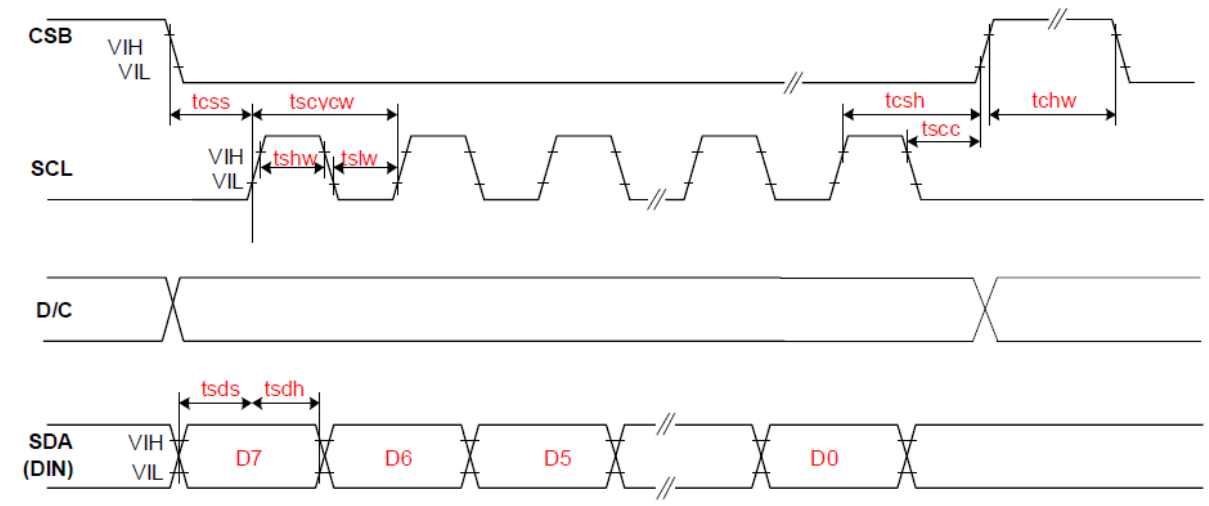


Figure : 4-wire Serial Interface – Read

Figure 4 Host Communications Timing Diagram

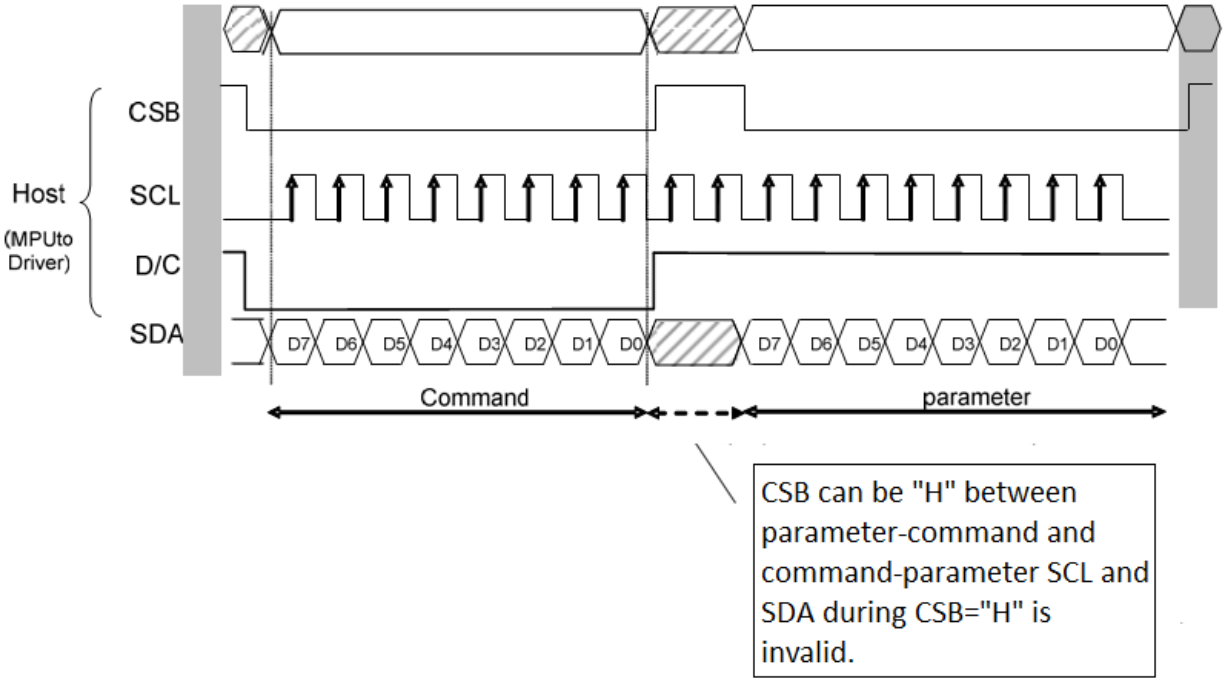
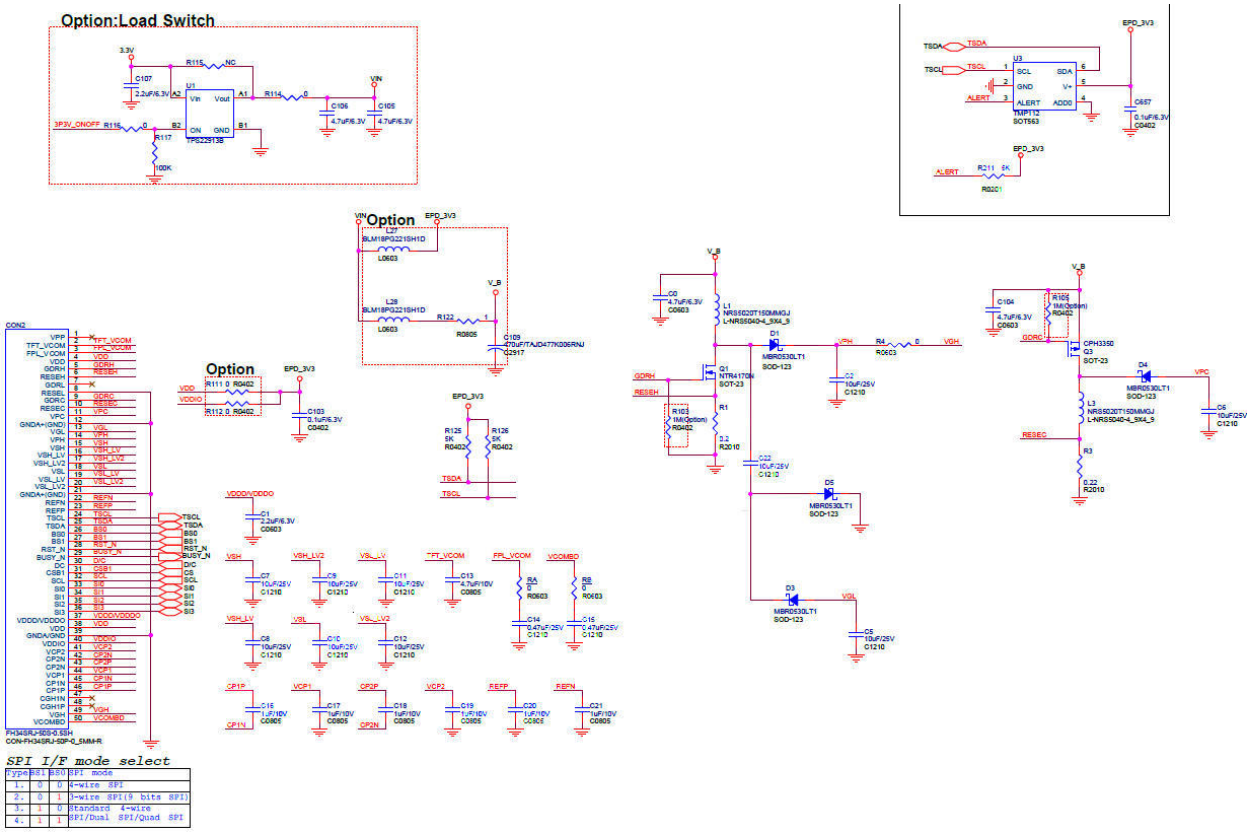


Table 2 Timing Table

Symbol	Signal			Min	Typ	Max	Unit
SERIAL COMMUNICATION							
tCSS	CSB	Chip select setup time		60			ns
tCSH		Chip select hold time		65			ns
tSCC		Chip deselect setup time		20			ns
tCHW		Chip deselect setup time		40			ns
tSCYCW	SCL	Serial clock cycle (Write)		50			ns
tSHW		SCL “H” pulse width (Write)		25			ns
tSLW		SCL “L” pulse width (Write)		25			ns
tSCYCR		Serial clock cycle (Read)		150			ns
tSHR		SCL “H” pulse width (Read)		60			ns
tSLR		SCL “L” pulse width (Read)		60			ns
tSDS	SDA (DIN) (DOUT)	Data setup time		30			ns
tSDH		Data hold time		30			ns
tACC		Access time				75	ns
tOH		Output disable time		15			ns

4 Reference circuit

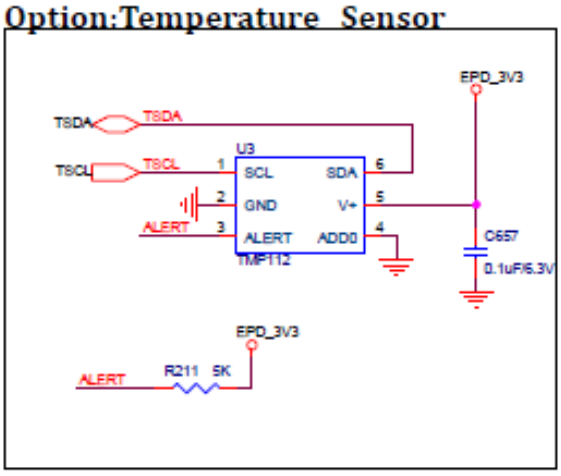
Figure 5 panel of 7.3” Reference Circuit



Note : MOS resistor, inductor and capacitor values may change to fine tune power consumption.

Note: Scheme 3 is the better power architecture for 7.3” display after optimization

Figure 6 Temperature Sensor Circuit (optional)



5 Software Programming Guide

This section describes the image update flow for the 7.3” panel. Defining the pin connection between MCU and the display is needed. The definition is customized in the file ”pindefine.h” User only needs to assign the MCU pins to connect the pins defined in this file. The definition is shown in figure 7. When the pin definition assigment is done, the display is automatically controlled by the functions in the sample code. The next two sections will describe the simulation of SPI transmission protocol and image update flow.

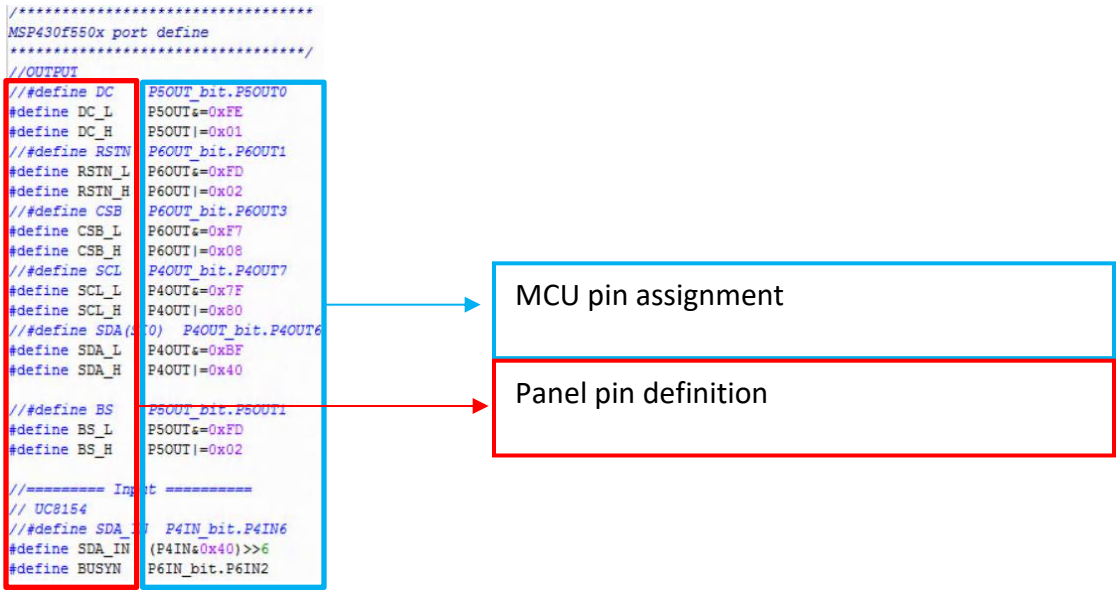


Figure 7 Program of ”pindefine.h” file.

5.1 Simulate SPI Transmission Protocol

There are four functions to simulate the SPI transmission protocol. All functions are listed in table 3.

Table 3 Simulate SPI Transmission Protocol Function Table

Function	Description
void spi_9b_init(void)	3-wire SPI initial setting.
void SPI_COMMAND (unsigned char dat)	Send command.
void SPI_DATA (unsigned char dat)	Send information of data
unsigned char SPI_GET_DATA(void)	Data read from IC.

The simulate SPI transmission protocol is based on the 3-wire mode. The SPI mode is selected by “**BS1_L**”, “**BS0_H**” for 3-wire and “**BS1_L**”, “**BS0_L**” for 4-wire in the “**void spi_9b_init(void)**” function, which is shown in table 5. Both modes can read/write registers from/to IC.

Table 4 BS High, Low Select Table

BS	Interface	BS1	BS0	CSB	DC	SCL	SSDA
High	**3-wire SPI**	Low	High	High	Low	High	High
Low	**4-wire SPI**	Low	Low	High	High	High	High

5.2 Image update flow

Figure 8 shows the programming sequence of the image update flow. Each step includes several functions. The first step is software reset for EPD. And the second step is the register setting for driver IC. The third step is to display the image. More details described in the following sections.

Figure 8 Three steps programming sequence.

```
//===============================================================================
//EPD main function
//===============================================================================
  P1OUT |=BIT0;       // Turn on LED
  EPD_Init();         // Initial
  EPD_Display_White();
  delay(200);
  EPD_Display_Black();
  delay(200);
  EPD_Display_Red();
  delay(200);
  EPD_Display_Yellow();
  delay(200);
  EPD_Display_White();
  P1OUT &=0xFE;       // Turn off LED
}
//===============================================================================
```

EPD and register initial.

Display

Figure 9 The programming sequence in "main.c".

5.2.1 EPD Software Reset

EPD software reset is include in the function " **void EPD_Init(void)**". The setting process is illustrated in figure 10. Please note that this process should be done twice as figure 8.

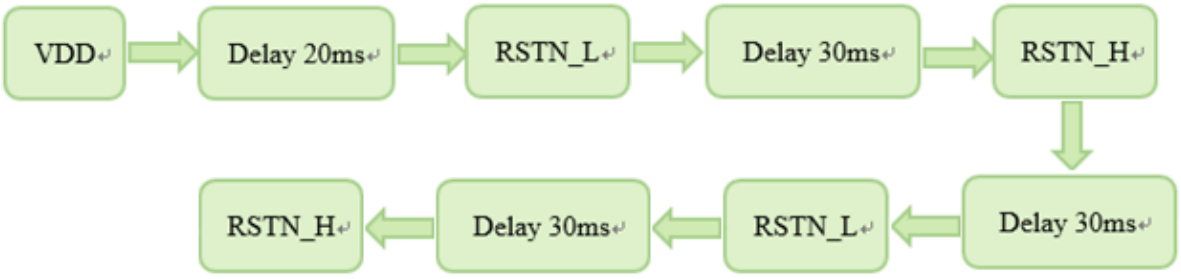


Figure 10 EPD Software Reset process.

5.2.2 Register Setting

Register setting is also included in function " **void EPD_Init(void)**". It should be executed after the EPD initial setting as shown in figure 11. The main registers should be defined as described in table 6.

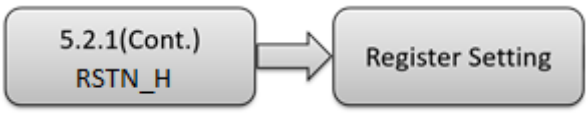


Figure 11 Register setting process.

5.2.3 DISPLAY

There are 4 image display functions, which are listed in table 5 with frame buffer settings (DTM). The display process is shown in figure 12 which is the way of short-term. Frame buffer settings will be introduced next chapter. The step "**check_busy"** is important for the programming sequence. The main idea is to check the device is powered up. Two functions are defined in table 6.

Table 5 Display Function Table

Function	Description	DTM
void EPD_Display_Black(void)	Display black image	0x00
void EPD_Display_White(void)	Display white image	0x11
void EPD_Display_Yellow(void)	Display yellow image	0x55
void EPD_Display_Red(void)	Display red image	0x44

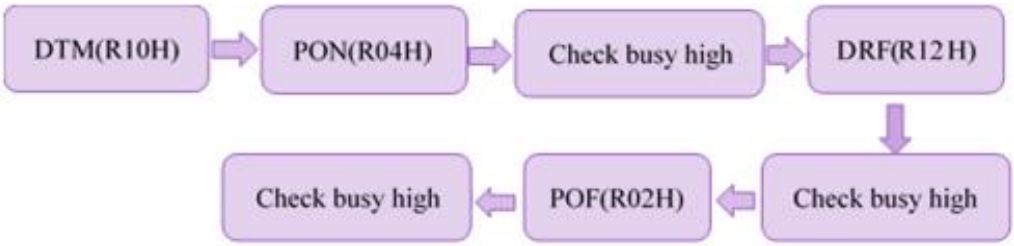


Figure 12 Display process.

Table 6 check_busy Function Table

Function	Description
void check_busy_high(void)	Check high peak finish.
void check_busy_low(void)	Check low peak finish.

5.2.4 DEEP SLEEP MODE AND WAKE UP PRODUCE

After the deep sleep Command, EPD will enter the deep sleep mode. The only way to return to standby is hardware reset.

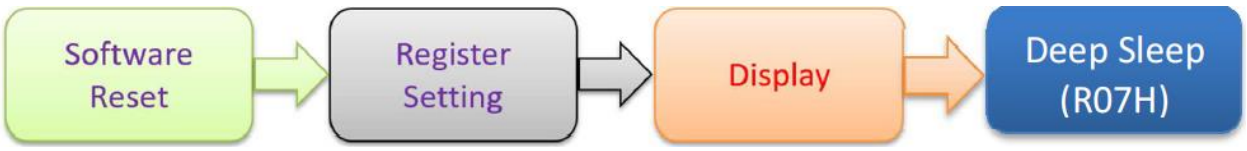


Figure 13 Deep sleep mode setting process

Figure 14 Wake up from deep sleep mode process.

6 Color mapping table for 7.3” Display

Color images (24-bit RGB) require convert into 4 colors. The color mapping is shown as below.

Color	Color index	Raw data of image
Black	000000	000
White	FFFFFF	001
Green	00FF00	010
Blue	0000FF	011
Red	FF0000	100
Yellow	FFFF00	101
Orange	FF7D00	110

Table 7 Color Mapping Table

Revision History

Version	Date	Page	Description	Author
0.1	2021/11/22		Initial	Jennifer Chen
0.2	2022/1/10	7	Correct reference circuit	Jennifer Chen
0.31	2022/4/21	9	“Software Reset” twice	Jennifer Chen