Integrated Solutions Technology,Inc.	Title IST7134 Specification 2 level-voltage output & 120 channels driver IC for EPD application	文件編號 DOC# IST-RD-0217	版次 Rev 002
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Specification

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
Research & Development	David 10/17/2019	Bonnie Lee 10/17/2019	Bonnie Lee 10/17/2019

Controlled by DCC

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Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
P001		New Release	E03160003	Michael	2016/03/11
P002	P15~16	Change BG mapping	E06160007	David	2016/06/27
001	P18	Updated Topr from 85℃ to 90℃ Delete output leakage item Updated Fosc condition Updated output voltage condition Updated driver outputs ON resistance	E04170010	Michael	2017/04/25
	P19	Updated dynamic current Add AC characteristics			
002	P14~P16	Add IIC interface information	E10190003	David	2019/10/17

接續頁 CONTINUATION --- ■ 是 YES; □ 否 NO

INTRODUCTION

The IST7134 is an all-in-one driver with timing controller for E-Paper. It has 120 segments plus 2 backgrounds and 1 common signal output. The outputs have 1-bit output per pixel. The timing controller provides control signals for the segments driver.

A high performance charge pump allows the IST7134 to generate the driver output voltage V0 (from 4V to 18V). It is possible to make the lowest power consumption display system with the fewest components for high performance portable systems. User can choose 2 level-voltage driver outputs, which consists of V0 and VSS. The chip also includes a temperature compensation for outputs driving time. User can easily choose one compensation curve for your application. The system is configurable through a 3-wire, 4-wire (SPI) serial interface or IIC interface.

FEATURES

Power Supply

- Logic Power: VDD1 – VSS1 = 1.6V ~ 3.6V
- Analog Power: VDD2 – VSS2 = 2.4V ~ 3.6V
  VDD3 – VSS3 = 2.4V ~ 3.6V
- Driving Voltage: V0 – VSS1/2/3 = 18V (Max)

Display Driver Output Circuits

- 120 Segment outputs + 2 Background + 1 VCOM
  - Output dynamic range: VSS ~ V0
  - Output deviation: 50mV

Functions Highlight

- Fewest components (None or 1 capacitor only)
- High performance voltage converter (with booster ratios x5/x6/x7/x8)
- Temperature compensation on outputs driving time, 4 curves optional
- Latch Pre-Frame display data for reducing refreshing time.
- Serial 3-wire/4-wire Write/Read interface
- IIC Write/Read interface
- Display On/Off control
- Software reset
- SEG output direction control
- COG package

BLOCK DIAGRAM

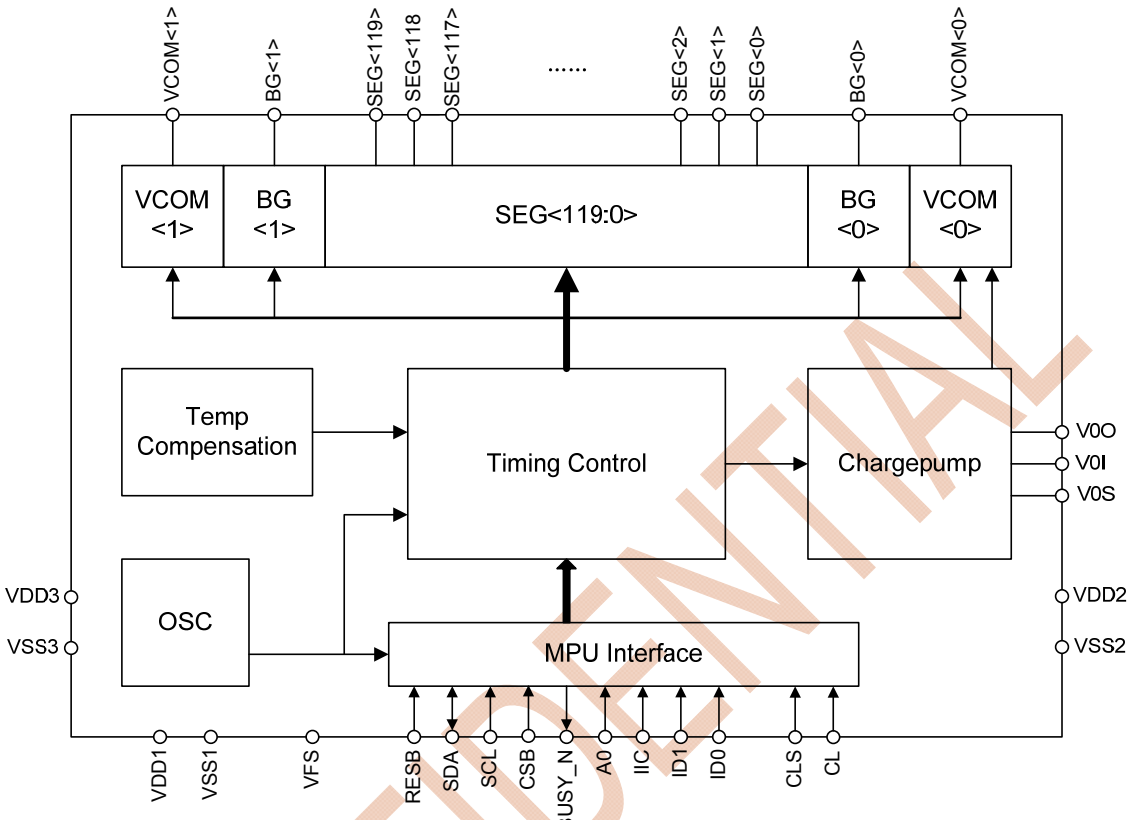


Fig. 1 IST7134 Block Diagram

*Note: VCOM<1> is the same as VCOM<0>.

PAD CONFIGURATION

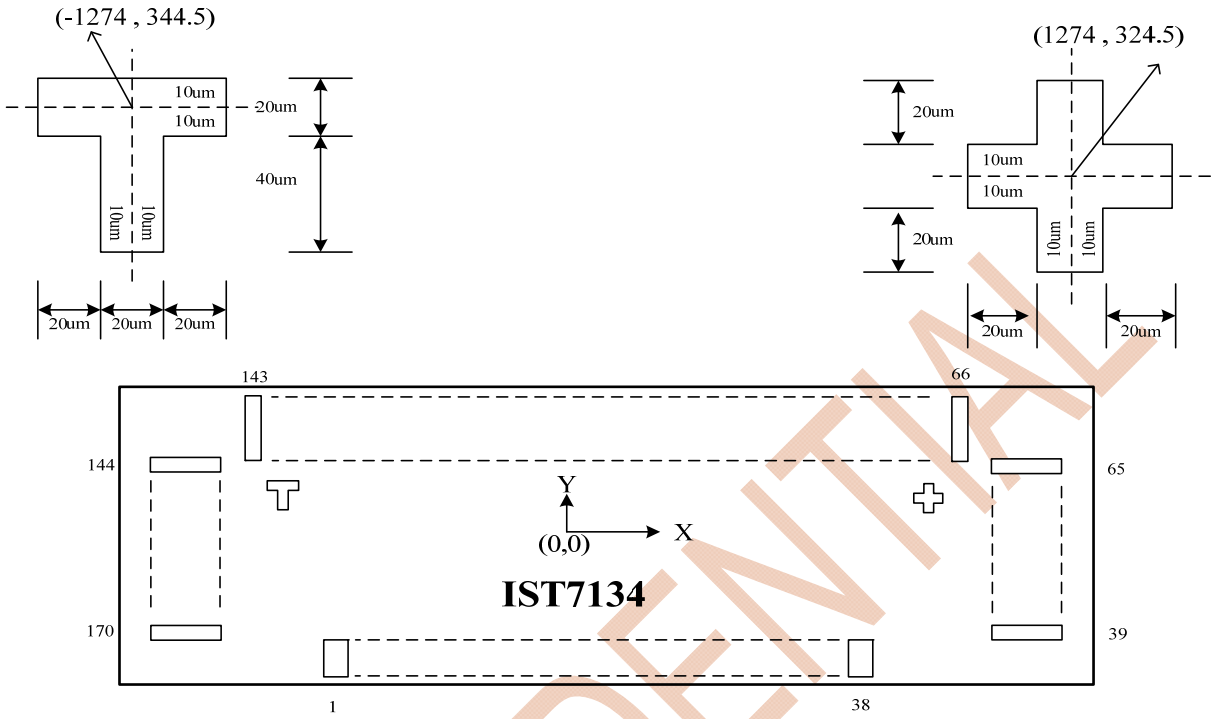


Fig. 2 IST7134 PAD Configuration

Chip Size	2858 um x 1021 um (Exclude Scribe Lane)	
Bump Pitch	34um (min)	
Bump Spacing	17um (min)	
Bump Size(X*Y)	30 x 40 um2	Pad No = 1 ~ 38
	71 x 17 um2	Pad No = 39 ~ 65, 144 ~ 170
	17 x 71 um2	Pad No = 66 ~ 143
Bump Height	12um (Typ.)	
Chip Thickness	300um (Typ.)	

PAD CENTER COORDINATES

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
1	NC	-1110	-481.5	51	SEG<8>	1385.5	-47.5	101	SEG<56>	119	467
2	V0I	-1050	-481.5	52	SEG<9>	1385.5	-13.5	102	SEG<57>	85	467
3	V0I	-990	-481.5	53	SEG<10>	1385.5	20.5	103	SEG<58>	51	467
4	V0I	-930	-481.5	54	SEG<11>	1385.5	54.5	104	SEG<59>	17	467
5	V0O	-870	-481.5	55	SEG<12>	1385.5	88.5	105	SEG<60>	-17	467
6	V0O	-810	-481.5	56	SEG<13>	1385.5	122.5	106	SEG<61>	-51	467
7	V0S	-750	-481.5	57	SEG<14>	1385.5	156.5	107	SEG<62>	-85	467
8	VSS3	-690	-481.5	58	SEG<15>	1385.5	190.5	108	SEG<63>	-119	467
9	VSS3	-630	-481.5	59	SEG<16>	1385.5	224.5	109	SEG<64>	-153	467
10	VSS2	-570	-481.5	60	SEG<17>	1385.5	258.5	110	SEG<65>	-187	467
11	VSS2	-510	-481.5	61	SEG<18>	1385.5	292.5	111	SEG<66>	-221	467
12	VSS1	-450	-481.5	62	SEG<19>	1385.5	326.5	112	SEG<67>	-255	467
13	VSS1	-390	-481.5	63	SEG<20>	1385.5	360.5	113	SEG<68>	-289	467
14	TEST3	-330	-481.5	64	SEG<21>	1385.5	394.5	114	SEG<69>	-323	467
15	VDD3	-270	-481.5	65	NC	1385.5	428.5	115	SEG<70>	-357	467
16	VDD3	-210	-481.5	66	NC	1309	467	116	SEG<71>	-391	467
17	VDD2	-150	-481.5	67	SEG<22>	1275	467	117	SEG<72>	-425	467
18	VDD2	-90	-481.5	68	SEG<23>	1241	467	118	SEG<73>	-459	467
19	VDD1	-30	-481.5	69	SEG<24>	1207	467	119	SEG<74>	-493	467
20	VDD1	30	-481.5	70	SEG<25>	1173	467	120	SEG<75>	-527	467
21	RESB	90	-481.5	71	SEG<26>	1139	467	121	SEG<76>	-561	467
22	SDA	150	-481.5	72	SEG<27>	1105	467	122	SEG<77>	-595	467
23	SCL	210	-481.5	73	SEG<28>	1071	467	123	SEG<78>	-629	467
24	CSB	270	-481.5	74	SEG<29>	1037	467	124	SEG<79>	-663	467
25	BUSY_N	330	-481.5	75	SEG<30>	1003	467	125	SEG<80>	-697	467
26	TEST2	390	-481.5	76	SEG<31>	969	467	126	SEG<81>	-731	467
27	TEST1	450	-481.5	77	SEG<32>	935	467	127	SEG<82>	-765	467
28	A0	510	-481.5	78	SEG<33>	901	467	128	SEG<83>	-799	467
29	IIC	570	-481.5	79	SEG<34>	867	467	129	SEG<84>	-833	467
30	ID1	630	-481.5	80	SEG<35>	833	467	130	SEG<85>	-867	467
31	ID0	690	-481.5	81	SEG<36>	799	467	131	SEG<86>	-901	467
32	VDD1	750	-481.5	82	SEG<37>	765	467	132	SEG<87>	-935	467
33	VSS1	810	-481.5	83	SEG<38>	731	467	133	SEG<88>	-969	467
34	CLS	870	-481.5	84	SEG<39>	697	467	134	SEG<89>	-1003	467
35	CL	930	-481.5	85	SEG<40>	663	467	135	SEG<90>	-1037	467
36	VFS	990	-481.5	86	SEG<41>	629	467	136	SEG<91>	-1071	467
37	VFS	1050	-481.5	87	SEG<42>	595	467	137	SEG<92>	-1105	467
38	NC	1110	-481.5	88	SEG<43>	561	467	138	SEG<93>	-1139	467
39	NC	1385.5	-455.5	89	SEG<44>	527	467	139	SEG<94>	-1173	467
40	COMR	1385.5	-421.5	90	SEG<45>	493	467	140	SEG<95>	-1207	467
41	BG<0>	1385.5	-387.5	91	SEG<46>	459	467	141	SEG<96>	-1241	467
42	NC	1385.5	-353.5	92	SEG<47>	425	467	142	SEG<97>	-1275	467
43	SEG<0>	1385.5	-319.5	93	SEG<48>	391	467	143	NC	-1309	467
44	SEG<1>	1385.5	-285.5	94	SEG<49>	357	467	144	NC	-1385.5	428.5
45	SEG<2>	1385.5	-251.5	95	SEG<50>	323	467	145	SEG<98>	-1385.5	394.5
46	SEG<3>	1385.5	-217.5	96	SEG<51>	289	467	146	SEG<99>	-1385.5	360.5
47	SEG<4>	1385.5	-183.5	97	SEG<52>	255	467	147	SEG<100>	-1385.5	326.5
48	SEG<5>	1385.5	-149.5	98	SEG<53>	221	467	148	SEG<101>	-1385.5	292.5
49	SEG<6>	1385.5	-115.5	99	SEG<54>	187	467	149	SEG<102>	-1385.5	258.5
50	SEG<7>	1385.5	-81.5	100	SEG<55>	153	467	150	SEG<103>	-1385.5	224.5

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
151	SEG<104>	-1385.5	190.5								
152	SEG<105>	-1385.5	156.5								
153	SEG<106>	-1385.5	122.5								
154	SEG<107>	-1385.5	88.5								
155	SEG<108>	-1385.5	54.5								
156	SEG<109>	-1385.5	20.5								
157	SEG<110>	-1385.5	-13.5								
158	SEG<111>	-1385.5	-47.5								
159	SEG<112>	-1385.5	-81.5								
160	SEG<113>	-1385.5	-115.5								
161	SEG<114>	-1385.5	-149.5								
162	SEG<115>	-1385.5	-183.5								
163	SEG<116>	-1385.5	-217.5								
164	SEG<117>	-1385.5	-251.5								
165	SEG<118>	-1385.5	-285.5								
166	SEG<119>	-1385.5	-319.5								
167	NC	-1385.5	-353.5								
168	BG<1>	-1385.5	-387.5								
169	COML	-1385.5	-421.5								
170	NC	-1385.5	-455.5								
（END）											

PAD DESCRIPTION

Power Supply

Name	I/O	Description
VDD1	Power Supply	IO power supply, the input voltage range is 1.6V ≤ VDD1 ≤ 3.6V.
VDD2/3	Power Supply	Analog power supply, the input voltage range is 2.4V ≤ VDD2 ≤ 3.6V.
VSS1	Power Supply	Logic Ground.
VSS2/3	Power Supply	Analog Ground.
V0I V0O V0S	Driver Outputs Power Supply	V0I is the power of SEG, BG and VCOM; V0S is the sensing input of the V0 generator; V0O is the output of V0 generator; V0O/V0S/V0I should be separated in ITO and connected together in FPC.
VFS	Power Supply	E-Fuse power supply, keep it open in normal operation.

System Control

Name	I/O	Description
CLS	I	Built-in oscillator circuit enable / disable select pin - CLS = “H” : enable (this pin is used together with digital command) - CLS = “L” : disable (external display clock input through CL pin)
CL	I/O	External clock input pin, when use built-in oscillator, let it “H”
TEST1/2/3	O	Test pins, NC in normal operation.

Micro-Controller Interface

Name	I/O	Description
RESB	I	Hardware Reset input pin. When RESB is “L”, initialization is executed.
SDA	I/O	Serial data for SPI/IIC interface.
SCL	I	Serial clock for SPI/IIC interface.
CSB	I	Chip select input pin, interface is enabled only when CSB is “L”.
BUSY_N	O	L: interface is BUSY and not ready for write command and data. H: interface is ready for write command and data.
A0	I	Register select input pin A0 = “H”: Write display data; A0 = “L”: Write control data.
IIC	I	Interface selection pin. Pull low to select SPI interface, pull high to select IIC interface.
ID1/ID0	I	When IIC = “L” ID0=0, ID1=0 select SPI3 interface ID0=1, ID1=0 select SPI4 interface When IIC = “H” ID1/ID0 is slave address for activate IST7134.

EPD Driver Outputs

Name	I/O	Description
SEG<119:0>	O	Segment driver outputs
BG<1:0>	O	Background driver outputs
VCOM<1:0>	O	VCOM Output.

Command Table

NO.	INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1	OSC Set	0	0	0	0	0	0	0	0	1	OSC OFF	OSCOFF=1， Oscillator OFF
2	Display ON/OFF （refresh）	0	0	1	0	1	0	1	1	1	DISP ON	DISPON=1， Driver output enable
3	Sleep Mode Set	0	0	1	0	1	0	1	1	0	SLEEP	SLEEP=1，Enter sleep mode
4	DATA1 latch Set	0	0	1	0	1	0	1	0	0	LTCH0	Ltch0=1，latch data
5	DATA2 latch set	0	0	1	0	1	0	1	0	1	LTCH1	Ltch1=1，latch data
6	RAM address set	0	0	0	1	0	RAM ADDR4	RAM ADDR3	RAM ADDR2	RAM ADDR1	RAM ADDR0	Set ram address
7	Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write ram data
8	Power Control	0	0	0	0	1	0	1	0	VC	VS	Set internal power
9	Regulation Ratio	0	0	0	1	1	1	RR3	RR2	RR1	RR0	Select regulation resistor ratio
10	CT set	0	0	1	0	0	0	0	0	0	1	Refer to Command Description
		0	0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	
11	V0 Generator CLK	0	0	1	0	1	0	0	0	VCK_ SEL<1>	VCK_ SEL<0>	Refer to Command Description
12	Set Boost Ratio	0	0	1	0	1	0	0	1	BT1	BT0	Refer to Command Description
13	TSON Set	0	0	1	1	1	0	0	0	0	TSON	TSON=1， Temp compensation enable
14	Temperature Sensor Data	0	0	1	1	1	0	0	1	0	0	Read temperature sensor register
		0	0	1	TS6	TS5	TS4	TS3	TS2	TS1	TS0	
15	Frame Time Set	0	0	1	0	1	1	0	1	FTS1	FTS0	Set temp compensation curve
16	TST & TSMT Set	0	0	1	1	1	0	0	1	0	1	Refer to Command Description
		0	0	0	TST2	TST1	TST0	0	TSNT2	TSMT1	TSMT0	
17	RESET	0	0	1	1	1	0	0	0	1	0	Soft reset
18	LNDIV Set	0	0	1	1	1	0	0	1	1	1	Set default frame time
		0	0	Indiv7	Indiv6	Indiv5	Indiv4	Indiv3	Indiv2	Indiv1	Indiv0	
19	Wave Form Set	0	0	1	0	0	0	0	0	1	0	Set wave form
		0	0	wave_ bb7	wave_ bb6	wave_ bb5	wave_ bb4	wave_ bb3	wave_ bb2	wave_ bb1	wave_ bb0	
		0	0	wave_ bw7	wave_ bw6	wave_ bw5	wave_ bw4	wave_ bw3	wave_ bw2	wave_ bw1	wave_ bw0	
		0	0	wave_ wb7	wave_ wb6	wave_ wb5	wave_ wb4	wave_ wb3	wave_ wb2	wave_ wb1	wave_ wb0	
		0	0	wave_ ww7	wave_ ww6	wave_ ww5	wave_ ww4	wave_ ww3	wave_ ww2	wave_ ww1	wave_ ww0	
		0	0	wave_ com7	wave_ com6	wave_ com5	wave_ com4	wave_ com3	wave_ com2	wave_ com1	wave_ com0	
20	Frame Set	0	0	0	1	1	0	frame3	fram2	frame1	frame0	Set frame number
21	Read Status	0	0	0	0	1	1	0	1	1	0	Read chip status
		0	1	BUSY_N	IBUSY	D	IRESB	0	0	0	0	
22	Register Read	0	0	1	0	0	0	1	1	0	0	Register read enable

COMMAND DESCRIPTION

OSC on/off

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	OSCOFF

The oscillator circuit will be turned off when OSCOFF set “H”

Display ON / OFF

EPD display ON / OFF select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1 Display ON;
DON = 0 Display OFF, power save mode.

Sleep Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	Sleep

Sleep mode only happen at SLP=1, It’ll stop all the operations in this chip, as long as there are no accesses from the MPU, the power consumption is close to the static leakage current.
Set SLP=0 to exit sleep mode.

Data1 Latch

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	LCTH0

ltch0= 1 first SRAM data latch;

Data2 Latch

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	LCTH1

ltch1= 1 second SRAM data latch;

Ram Address

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	RAM Addr4	RAM Addr3	RAM Addr2	RAM Addr1	RAM Addr0

Write RAM address

RAM Data

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

8-bit display data can be written to the display RAM location specified by the column address and row address by this instruction. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed rows.

Power Control

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	0	VC	VS

VS="0"/"1" Internal voltage reference circuit OFF/ON;
VC="0"/"1" V0 voltage generator OFF/ON.

Regulation Ratio

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	RR3	RR2	RR1	RR0

This instruction controls the regulation ratio of the built-in regulator.

RR3	RR2	RR1	RR0	Regulation Ratio (RR)
0	0	0	0	2.0
0	0	0	1	2.5
0	0	1	0	3.0
0	0	1	1	3.5
0	1	0	0	4.0
0	1	0	1	4.5
0	1	1	0	5.0
0	1	1	1	5.5
1	0	0	0	6.0
1	0	0	1	6.5
1	0	1	0	7.0
1	0	1	1	7.5
1	1	0	0	8.0
1	1	0	1	8.5
1	1	1	0	9.0
1	1	1	1	9.5

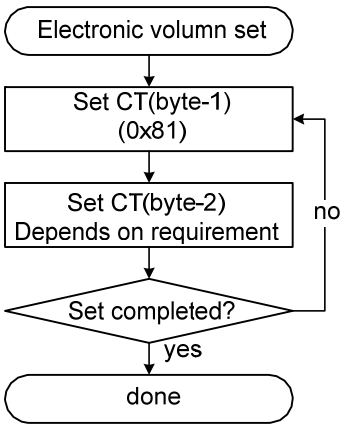
The operation voltage (V0) calculation formula is shown below:
(RR comes from Regulation Ratio, CT comes from CT[7:0])
V0 = RR X [1 – (255 – CT) / 648] X 2.1, or V0 = RR X [(393 + CT) / 648] X 2.1

SYMBOL	REGISTER	VALUE
RR	RR[3:0]	2, 2.5, 3, 3.5 …… and 9.5
CT	CT[7:0]	0 ~ 255

CT Set

This is double byte instruction. The first byte set IST7134 into CT adjust mode and the following instruction will change the CT setting. That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the EPD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1
0	0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0



The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of EPD module. There are 16 V0 voltage curves can be selected. It is recommended the CT should be close to the center (7FH) for easy contrast adjustment. Please refer to the “Selection of Application Voltage” section for detailed information.

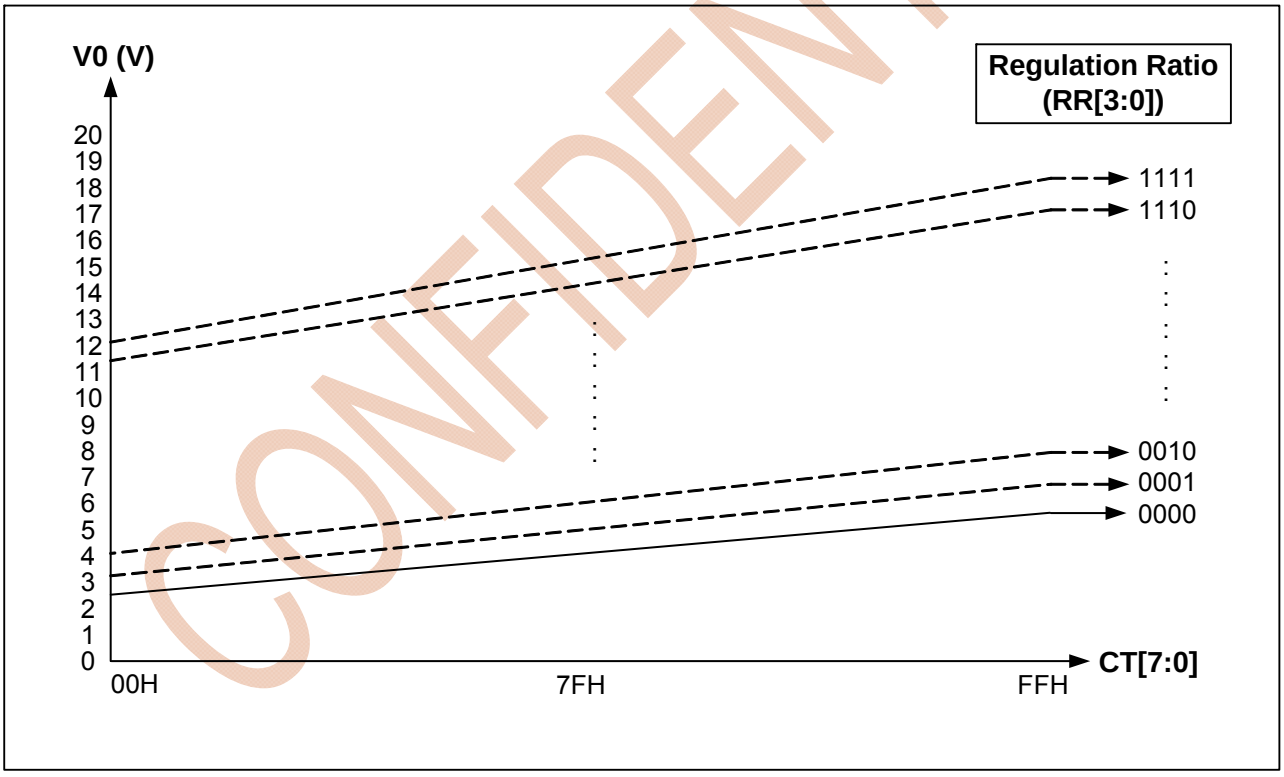


Fig. 3 V0 Regulation

V0 Generator Clock Frequency Select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	VCK_ SEL<1>	VCK_ SEL<0>

VCK_SEL1	VCK_SEL0	F_div
0	0	1/8 (default)
0	1	1/4
1	0	1/2
1	1	1/1

Boost Set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	BT1	BT0

BT1-0: Define the DCDC booster operation mode; select the suitable BT1-0 will save the power consumption.

BT<1:0>	00	01	10	11
$V0_{MAX}$	X5	X6	X7	X8

TSON Set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	TSON

TSON: The instruction determines the temperature auto compensation which is ON/OFF. When TSON=1, the temperature auto compensation turns on. When TSON=0, it turns off.

Temperature Sensor (Read sensor register)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0
0	1	1	TS6	TS5	TS4	TS3	TS2	TS1	TS0

The instruction has double byte. When use it, send the command E1H first and then send read signal.

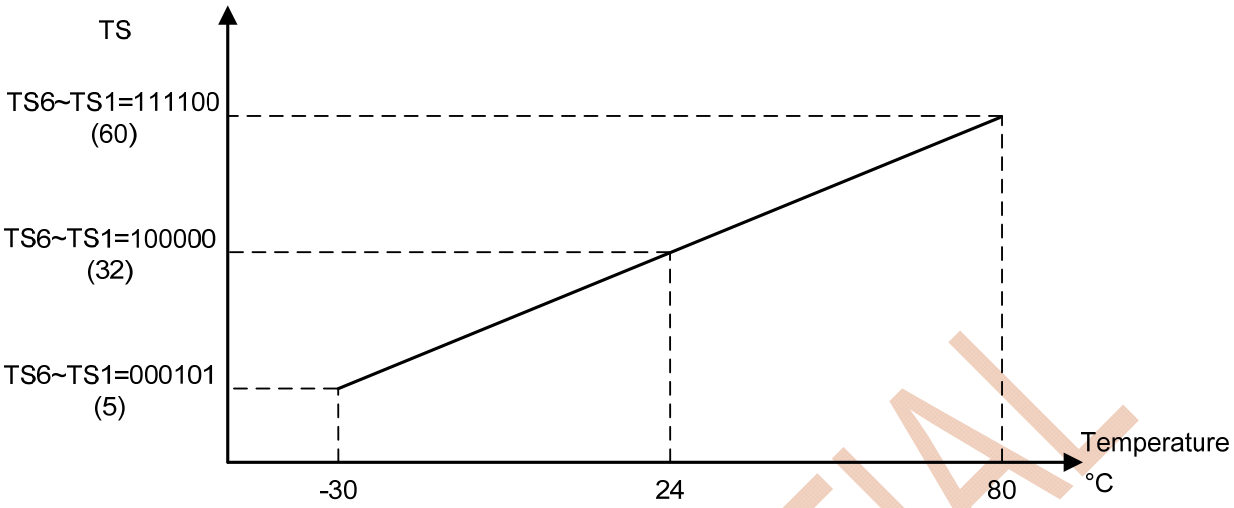


Fig. 4 Temperature Compensation on Refreshing time

6-bit output, resolution is 2℃/bit, we can get Temperature reading from the following formula.

TS = (Temperature+40)/2, Temperature = TS*2 – 40℃

Temperature Sensor Measure Times

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	1
		*	TST2	TST1	TST0	*	TSMT2	TSMT1	TSMT0

TSMT: It provide to select the times which the temperature sensor measure, and average the values.

TSMT2	TSMT1	TSMT0	Average times
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

TST: It provide to select the frequency which the temperature sensor measure.

TST2	TST1	TST0	Frequency (KHz)
0	0	0	100
0	0	1	59
0	1	0	37
0	1	1	27
1	0	0	20
1	0	1	15
1	1	0	12
1	1	1	10

Frame Time Set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	1	FTS1	FTS0

Default frame time is T_{LN}=300ms (Set by "LNDIV"), when temperature>10℃;

When temperature<10℃, frame time auto expend to 500ms as default, it also can be set to T_{LN}+0ms, T_{LN}+100ms, T_{LN}+200ms(default), T_{LN}+300ms and T_{LN}+400ms.

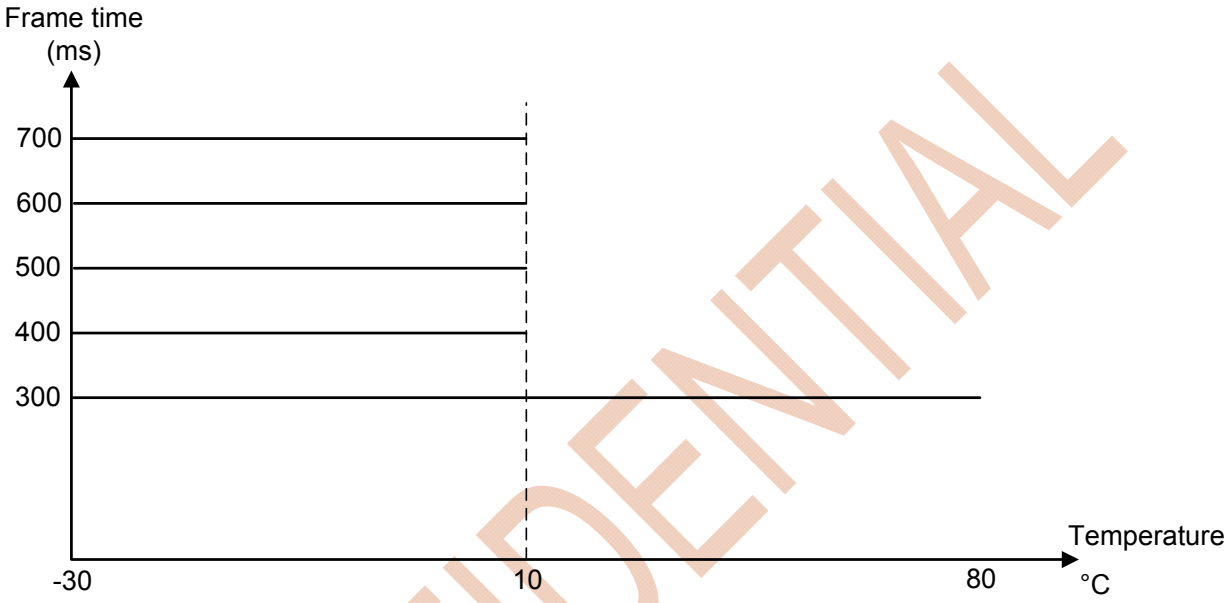


Fig. 5 Frame Time

TSON	FTS1	FTS0	Frame time (ms)
0	x	x	T_{LN}+0
1	0	0	T_{LN}+100
1	0	1	T_{LN}+200(default)
1	1	0	T_{LN}+300
1	1	1	T_{LN}+400

S/W Reset

This instruction will activate the internal S/W reset operation. The covered ranged is different with H/W reset, for details please refer to the "Reset Initialization" section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	1	0

LNDIV set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	1	1
0	0	Indiv7	Indiv6	Indiv5	Indiv4	Indiv3	Indiv2	Indiv1	Indiv0

Oscillator cycle set.

Lndiv7	Lndiv6	Lndiv5	Lndiv4	Lndiv3	Lndiv2	Lndiv1	Lndiv0	Oscillator cycle (ms)
0	0	0	0	0	0	0	0	20
0	0	0	0	0	0	0	1	40
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	0	-
1	1	1	1	1	1	1	1	-

Wave Form Set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	1	0
0	0	wave_bb7	wave_bb6	wave_bb5	wave_bb4	wave_bb3	wave_bb2	wave_bb1	wave_bb0
0	0	wave_bw7	wave_bw6	wave_bw5	wave_bw4	wave_bw3	wave_bw2	wave_bw1	wave_bw0
0	0	wave_wb7	wave_wb6	wave_wb5	wave_wb4	wave_wb3	wave_wb2	wave_wb1	wave_wb0
0	0	wave_ww7	wave_ww6	wave_ww5	wave_ww4	wave_ww3	wave_ww2	wave_ww1	wave_ww0
0	0	wave_com7	wave_com6	wave_com5	wave_com4	wave_com3	wave_com2	wave_com1	wave_com0

User can write scan timing in this mode.

Frame set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	frame3	frame2	frame1	frame0

Frame number set.

Read Status

Indicate the internal status of the IST7134. When use SPI3, SPI4 or IIC interface, command 36H must be write before read operation.

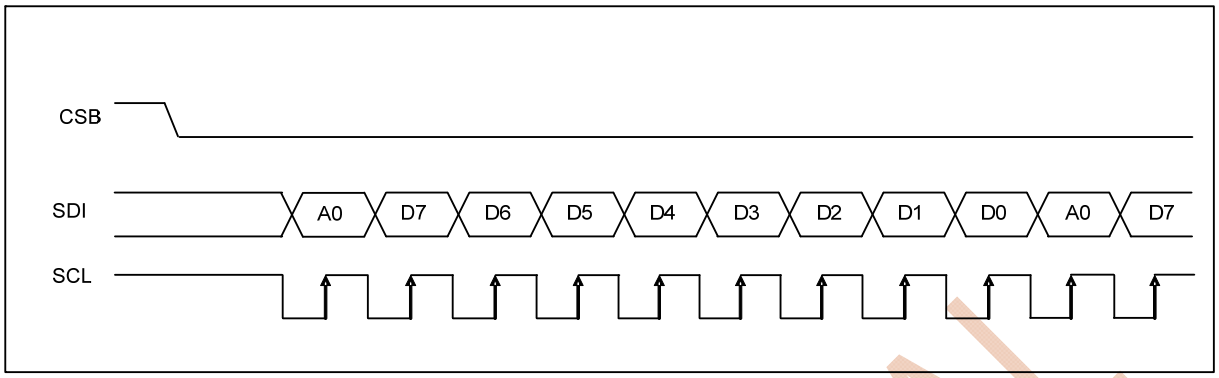
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	1	0

Only use in SPI3, SPI4 or IIC interface

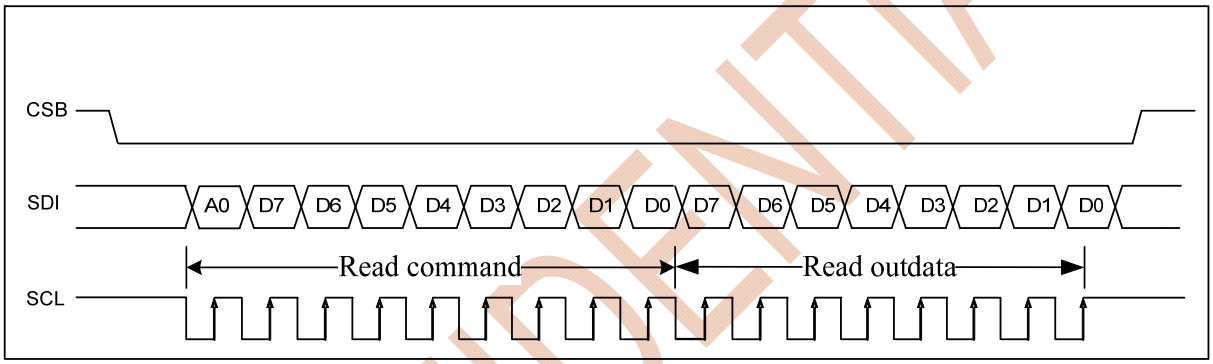
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	BUSY_N	DON	IRESB	0	0	0	0

FUNCTIONAL DESCRIPTION

3-Line Serial Interface Timing

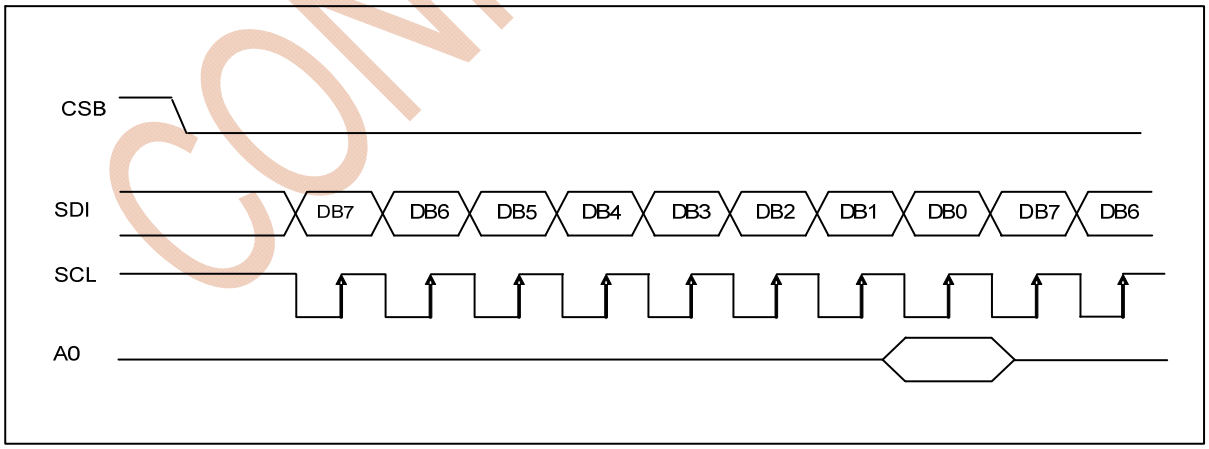


Write operation of 3-Line SPI

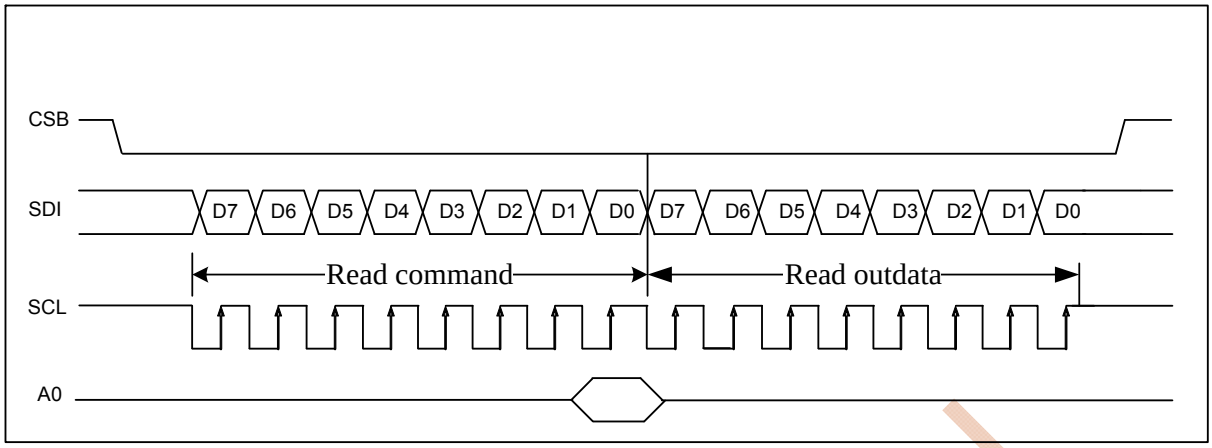


Read operation of 3-Line SPI

4-Line Serial Interface Timing



Write operation of 4-Line SPI



Read operation of 4-Line SPI

Note: 1.After read enable command is set, SDI must set Hiz

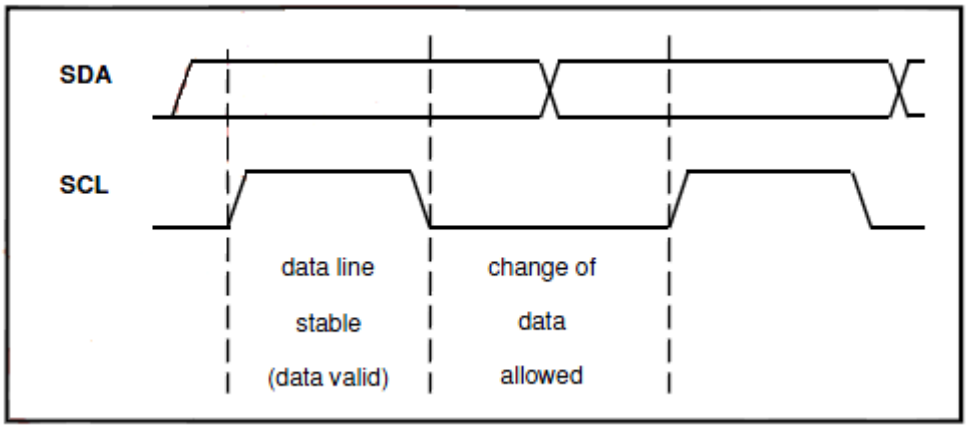
2. When read operation is done, CSB must set high once to quit read operation.

IIC Serial Interface Timing

The IST7134 also supports IIC interface for command & display data communication. The IIC interface is a bi-directional, two-line serial interface, the two lines are a Serial Data line(SDA) and a Serial Clock line(SCL), if MCU(IIC master) IO is open-drain mode, both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

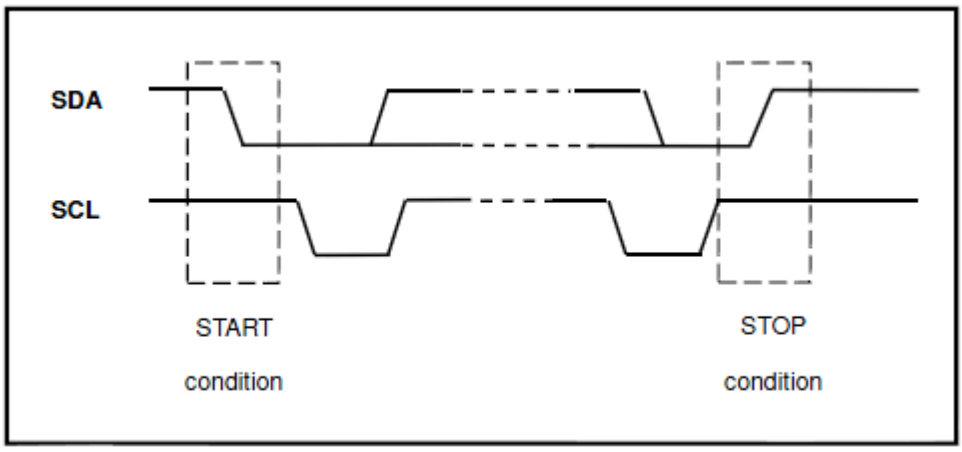
Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes in the data line at this time will be interpreted as a control signal



START and STOP Conditions

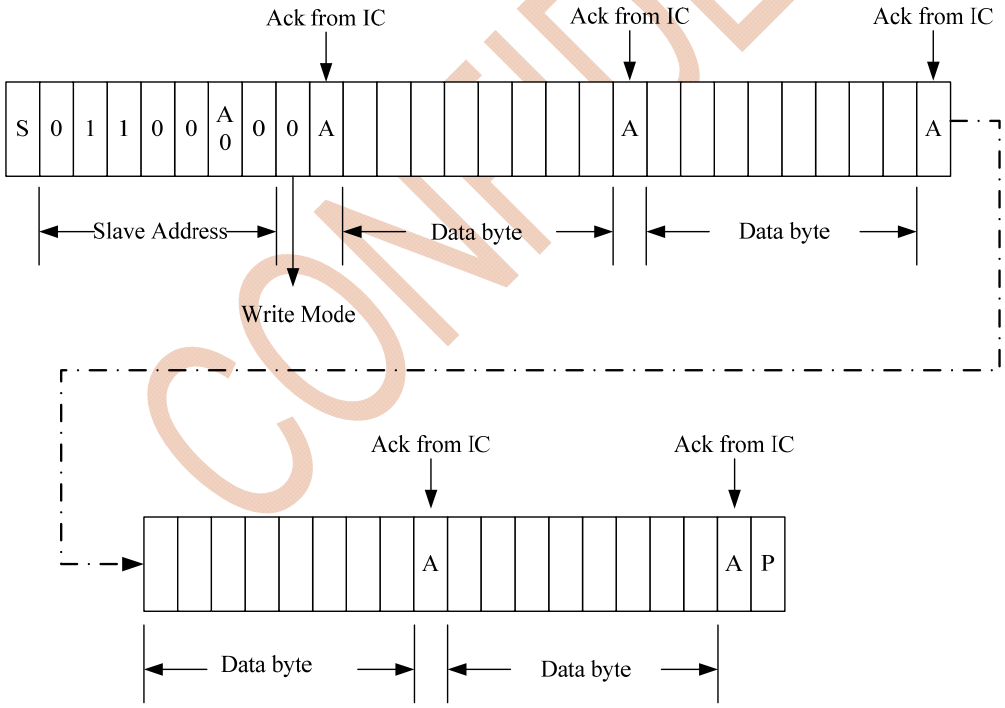
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).



IIC Interface Protocol

The IIC transmitting is initiated with a START condition (S) from the IIC–bus Master and followed by a slave address. Two 6-bit slave addresses (011000, 011010, 011100, and 011110) are reserved for the IST7134. The least significant bit of the slave address (ID) is configured by ID0 and ID1 pin to decide is the slave address is 011000 (ID0=0/ID1=0) or 011010 (ID0=0/ID1=1) or 011100(ID0=1/ID1=0) or 011110(ID0=1/ID1=1). The 7th bit follows the previous 6bit address is A0(indicates write data or write command).The 8th bit follows the previous 6-bit address is the data direction bit (R/W) -- '0' indicates Master data transmission (WRITE), '1' indicates Master data request (READ).

WRITE Mode (Master transmits data to Slave, R/W=0)



A0=1 : write data

A0=0: write command

Default Output Waveform

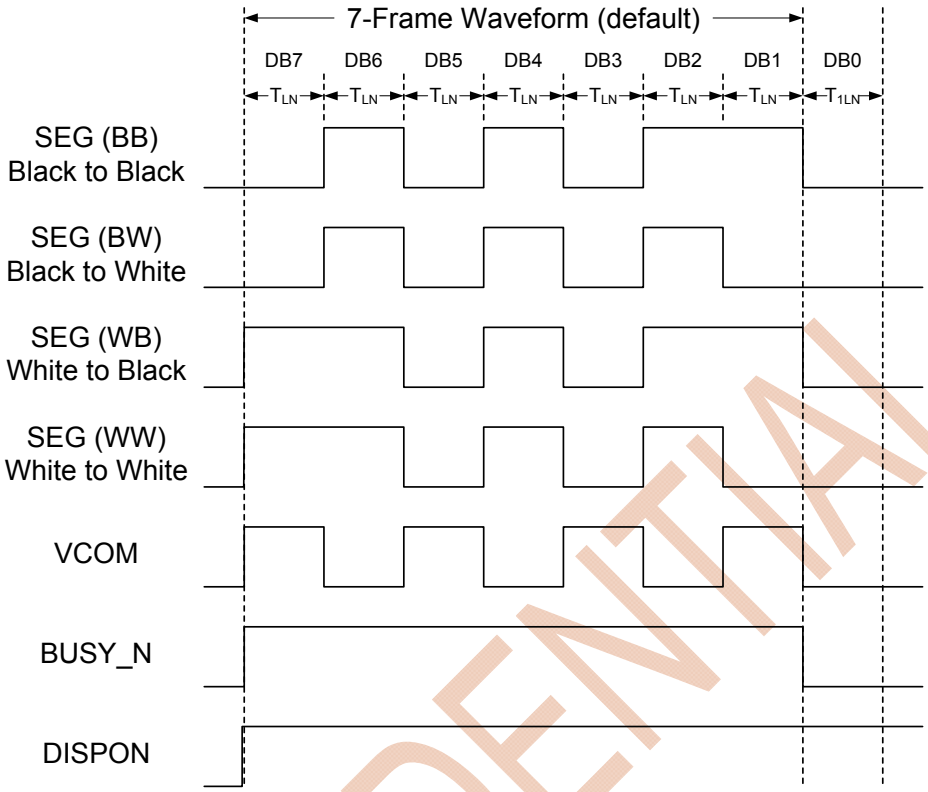


Fig. 6 Default Output Waveform

This waveform is a default driver output waveform. The high level is equal to V0, and the low level is equal to VSS. T_{LN} is 300ms as default when user doesn't modify the command resister "LNDIV". The beginning of display refreshing is when display enable signal DISPON become from "L" to "H", then the 8-bit setting "Wave Form Set" of SEG and VCOM will perform as outputs waveform from DB7 to DB0. The default values of "Wave Form Set" are as follows:

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
SEG (BB)		0	1	0	1	0	1	1	0
SEG (BW)		0	1	0	1	0	1	0	0
SEG (WB)		1	1	0	1	0	1	1	0
SEG (WW)		1	1	0	1	0	1	0	0
VCOM		1	0	1	0	1	0	1	0

How many bits to be performed at output are controlled by "Frame Set", default value is 0x07, the output waveform will only perform from DB7 to DB1, the DB0 output will keep at low level. If the "Frame Set" were set

To 0x03, the output waveform will only perform from DB7 to DB5, the DB4 to DB0 output will keep at low level.Total 8 is the maximum frames from DB7 to DB0, exceed this, all the driver outputs will keep at low level

until DISPON rising edge. BUSY_N output signal shows the refreshing status set by “Frame Set”.Segment and BG driver outputs mapping.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SEG<7>	SEG<6>	SEG<5>	SEG<4>	SEG<3>	SEG<2>	SEG<1>	SEG<0>
SEG<15>	SEG<14>	SEG<13>	SEG<12>	SEG<11>	SEG<10>	SEG<9>	SEG<8>
SEG<23>	SEG<22>	SEG<21>	SEG<20>	SEG<19>	SEG<18>	SEG<17>	SEG<16>
SEG<31>	SEG<30>	SEG<29>	SEG<28>	SEG<27>	SEG<26>	SEG<25>	SEG<24>
SEG<39>	SEG<38>	SEG<37>	SEG<36>	SEG<35>	SEG<34>	SEG<33>	SEG<32>
SEG<47>	SEG<46>	SEG<45>	SEG<44>	SEG<43>	SEG<42>	SEG<41>	SEG<40>
SEG<55>	SEG<54>	SEG<53>	SEG<52>	SEG<51>	SEG<50>	SEG<49>	SEG<48>
SEG<63>	SEG<62>	SEG<61>	SEG<60>	SEG<59>	SEG<58>	SEG<57>	SEG<56>
SEG<71>	SEG<70>	SEG<69>	SEG<68>	SEG<67>	SEG<66>	SEG<65>	SEG<64>
SEG<79>	SEG<78>	SEG<77>	SEG<76>	SEG<75>	SEG<74>	SEG<73>	SEG<72>
SEG<87>	SEG<86>	SEG<85>	SEG<84>	SEG<83>	SEG<82>	SEG<81>	SEG<80>
SEG<95>	SEG<94>	SEG<93>	SEG<92>	SEG<91>	SEG<90>	SEG<89>	SEG<88>
SEG<103>	SEG<102>	SEG<101>	SEG<100>	SEG<99>	SEG<98>	SEG<97>	SEG<96>
SEG<111>	SEG<110>	SEG<109>	SEG<108>	SEG<107>	SEG<106>	SEG<105>	SEG<104>
SEG<119>	SEG<118>	SEG<117>	SEG<116>	SEG<115>	SEG<114>	SEG<113>	SEG<112>
						BG<1>	BG<0>

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD1/2/3	-0.3 ~ 5	V
	V0O/V0I/V0S	-0.3 ~ 18	V
Input voltage range	V_{IN}	-0.3 to VDD1+0.3	V
Operating temperature range	T_{OPR}	-40 to +90	℃
Storage temperature range (Bare chip)	T_{STR}	-55 to +125	℃

NOTES:
1. VDD1/2/3 and V0O/V0I/V0S are based on VSS1/2/3 = 0V;
2. The voltage levels relation V0O/V0I/V0S ≥ VDD1/2/3 ≥VSS1/2/3 = 0V must be always satisfied;
3. If supply voltage exceeds the absolute maximum range, this LSI may be damaged permanently.

DC CHARACTERISTICS

(Ta = -30 to 85℃)

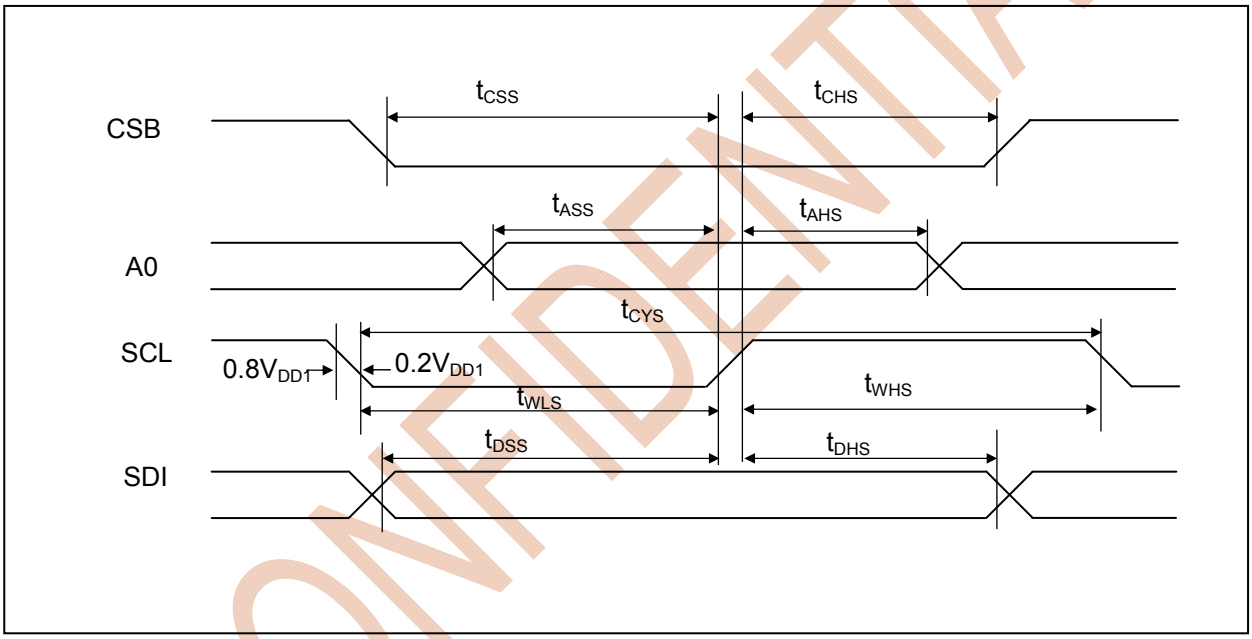
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage(1)		VDD1		1.6	3.0	3.6	V
Operating Voltage(2)		VDD2/3		2.4	3.0	3.6	V
Operating Voltage(3)		V0O/V0I/V0S		4.0	-	18	V
Input voltage	High	V_{IH}		0.8*VDD1	-	VDD1	V
	Low	V_{IL}		VSS1	-	0.2*VDD1	
Output voltage	High	V_{OH}	IOUT = 1mA, VDD1=3V	0.8*VDD1	-	VDD1	V
	Low	V_{OL}	IOUT = -1mA, VDD1=3V	VSS1	-	0.2*VDD1	
Input leakage current		I_{IL}	V_{IN} = VDD1 or VSS1	-1.0	-	+1.0	μA
Driver Outputs ON Resistance		R_{ON}	Ta = 25℃, V0 = 15V	-	4.5	-	kΩ
Oscillator frequency (internal)		F_{OSC}	Ta = 25℃, VDD1=3.3V	2.8	3.0	3.2	MHz
Oscillator frequency (External)		F_{CL}	Ta = 25℃	-	3.0	-	MHz

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Dynamic current consumption	I_{VDD}	VDD1=VDD2=VDD3=3.0V Booster X6, V0 = 15V, COM cycle time=640ms check pattern, no loading Ta=25℃	-	65	100	μA
Sleep mode	I_{VDD}	VDD1=VDD2=VDD3=3.0V Ta=25℃	-	-	1	μA

AC CHARACTERISTICS

Serial Interface Characteristics(SPI3/SPI4)



(VDD1=1.6~3.6V, Ta = -30 to 85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	SCL (Write)	t_{CYS} t_{WHS} t_{WLS}	200 90 90		- - -	ns	
Serial clock cycle SCL high pulse width SCL low pulse width	SCL (Read)	t_{CYS} t_{WHS} t_{WLS}	540 210 300		- - -	ns	
Address setup time Address hold time	A0	t_{ASS} t_{AHS}	90 90		- -	ns	
Data setup time Data hold time	SDI	t_{DSS} t_{DHS}	90 90		- -	ns	
CSB setup time CSB hold time	CSB	t_{CSS} t_{CHS}	90 90		- -	ns	

Note: All signal Rising time and falling Time <15ns

REFERENCE APPLICATIONS

MPU Interface

1. In Case of 3-wire SPI

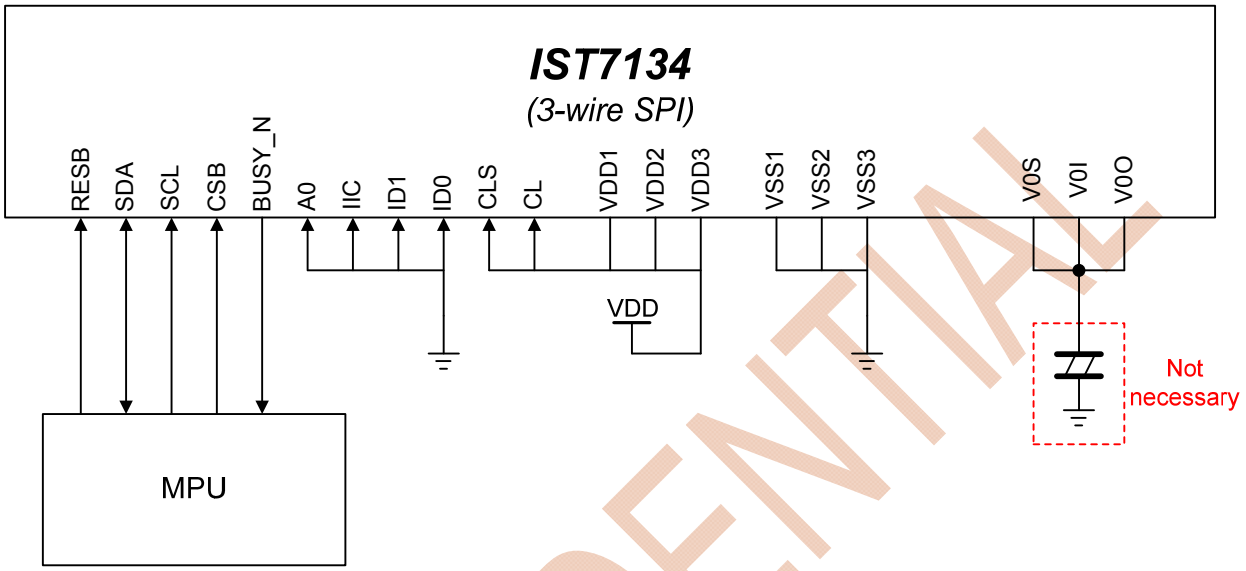


Fig. 7 3-wire SPI

2. In Case of 4-wire SPI

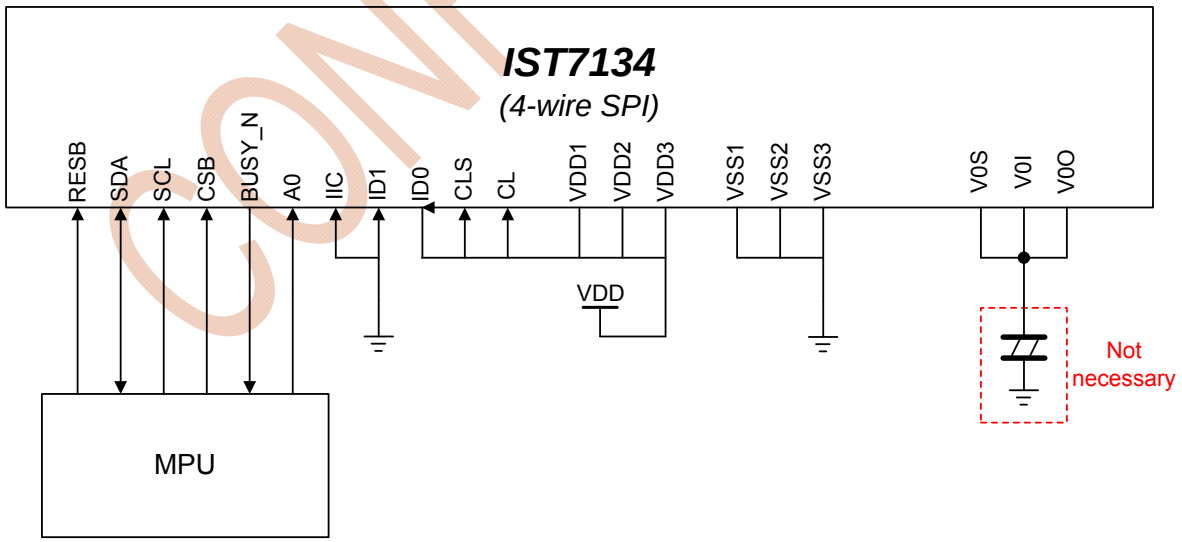


Fig. 8 4-wire SPI

3. In Case of IIC Interface

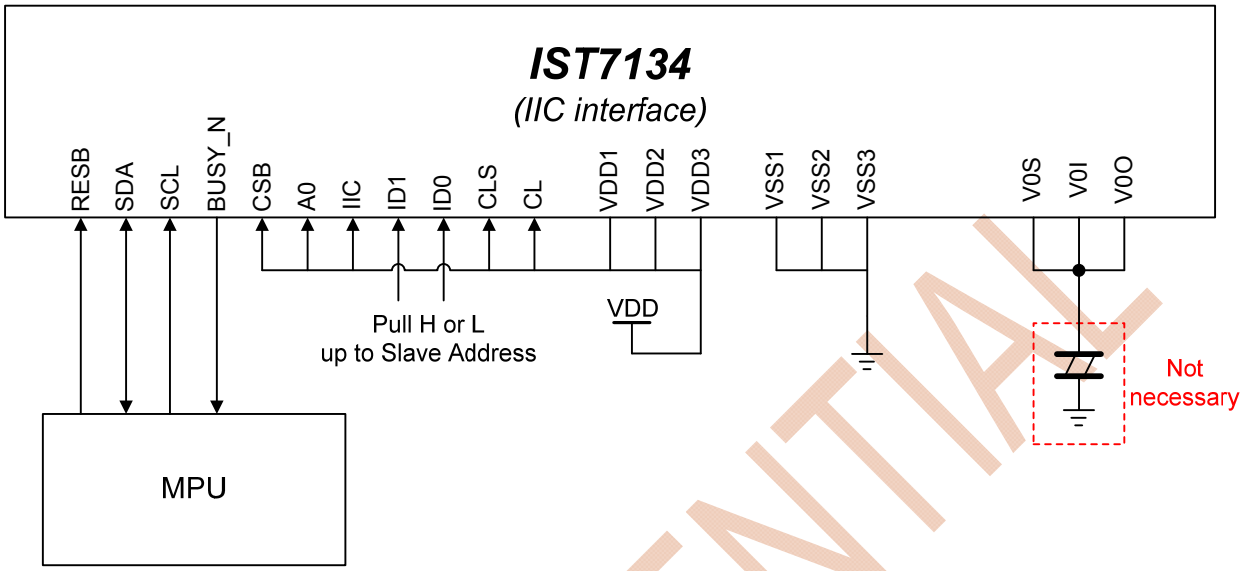


Fig. 9 IIC Interface

CAUTIONS:

1. This Specification will be subjected to modify without notice.

2. Precautions on Light:

Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light, therefore, can potentially lead to its malfunctioning.

2.1 Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation .

2.2 Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

2.3 The IC must be shielded from light in the front, back and side faces.

3.ESD control and prevention:

3.1 Humidity Control:30~70% relative humidity is recommended.

3.2 To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all sources of static fields removed.(Example: Station ionizers).

3.3 Grounding all personnel who come in contact with parts will eliminate a possible source of ESD. (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4. Storage Conditions:

Before open package	After open package
Temp.=25±5℃ Humidity:50~70% Less than 1 Years	Temp.=25±5℃ Humidity:50~70% Less than 3 Months