SPD1656

Advance Information

640 Source x 480 Gate
Active Matrix EPD Display Driver with Controller
for color application

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Appendix: IC Revision history of SPD1656 Specification

Version	Change Items	Effective Date
1.0	Initial Release	06-May-2019
1.1	1) Updated AC Characteristics 2) Updated application circuit and component list 3) Updated command description	03-Jan-2020

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1 General Description

The SPD1656 is an Active Matrix EPD Display Driver with Controller which can support Red/Black/White. It consists of 640 source outputs, 480 gate outputs, 1 VCOM and 1 VBD for border that can support a maximum display resolution 640x480. In addition, the SPD1656 has a cascade mode that can support higher display resolution up to display resolution 1280x480.

The SPD1656 embeds booster, regulators and oscillator. Data/Commands are sent from general MCU through the hardware selectable Serial peripheral.

2 Features

- Power supply:
  - VDD: 2.3 to 3.6V
  - VDDIO: Connect to VDD
  - VDDD/VDDDO: 1.8V, regulate from VDD supply
- Design for dot matrix type active matrix EPD display
- Resolution: 640 source outputs; 480 gate outputs; 1 VCOM; 1VBD for border
- On chip display RAM
  - 3bit outputs per pixel to support black/ white/ color
- On-chip booster and regulator for generating VCOM, Gate and Source driving voltage
  - Gate driving output voltage:
    - VGH: 17V to 20V (Voltage step: 1V)
    - VGL: -VGH
  - Source / VBD driving output voltage:
    - VSH: 15V
    - VSH_LV: 3V to 15V (Voltage step: 200mV)
    - VSL_LV: -3V to -15V (Voltage step: 200mV)
    - VSL_LV2: -3V to -15V (Voltage step: 200mV)
    - VSL: -15V
  - VCOM output voltage
    - DCVCOM: -4V to -0.1V (Voltage step: 50mV)
    - Built in VCOM sensing
- 640 outputs source driver with 3-bit resolution for black/ white/ color
  - 7 levels output (VSH, VSH_LV, GND, VSL_LV, VSL_LV2, VSL and floating)
  - Output deviation: 0.2V
  - Left and Right shift capability
- 1 output VBD driver for border:
  - Function same as the programmable source driver with selected LUT
  - Selected Output as VCOM
- 480 outputs gate driver
  - 2 levels output (VGH and VGL)
  - Up and down shift capability
  - Max 40Vp-p
- 1 output VCOM driver:
  - DCVCOM
  - ACVCOM for 4 levels output
    - VSH+DCVCOM, DCVCOM, VSL+DCVCOM and floating
- Pre select resolutions: 640x240;600x240;640x320;600x320; 640x480;600x450;640x448;600x448
- On-chip oscillator
- Support frame rate: 200Hz (max)
- Support LUT (LUT0~LUT7, LUTVCOM, LUTXON)
- SPI Master Interface to external SPI flash for waveform storage
- Support Low voltage detect for supply voltage
- Internal Temperature Sensor (-25 to 50 degC, +/-2degC /8 bit status)
- I2C Single Master Interface to read external temperature sensor reading
- Cascade mode to support higher display resolution
- MCU interface: Serial peripheral , Maximum SPI write speed 10MHz
- Low current consumption for operation and sleep
- Available in COG package

3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SPD1656Z0	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 180um Bump height: 12um

4 Block Diagram

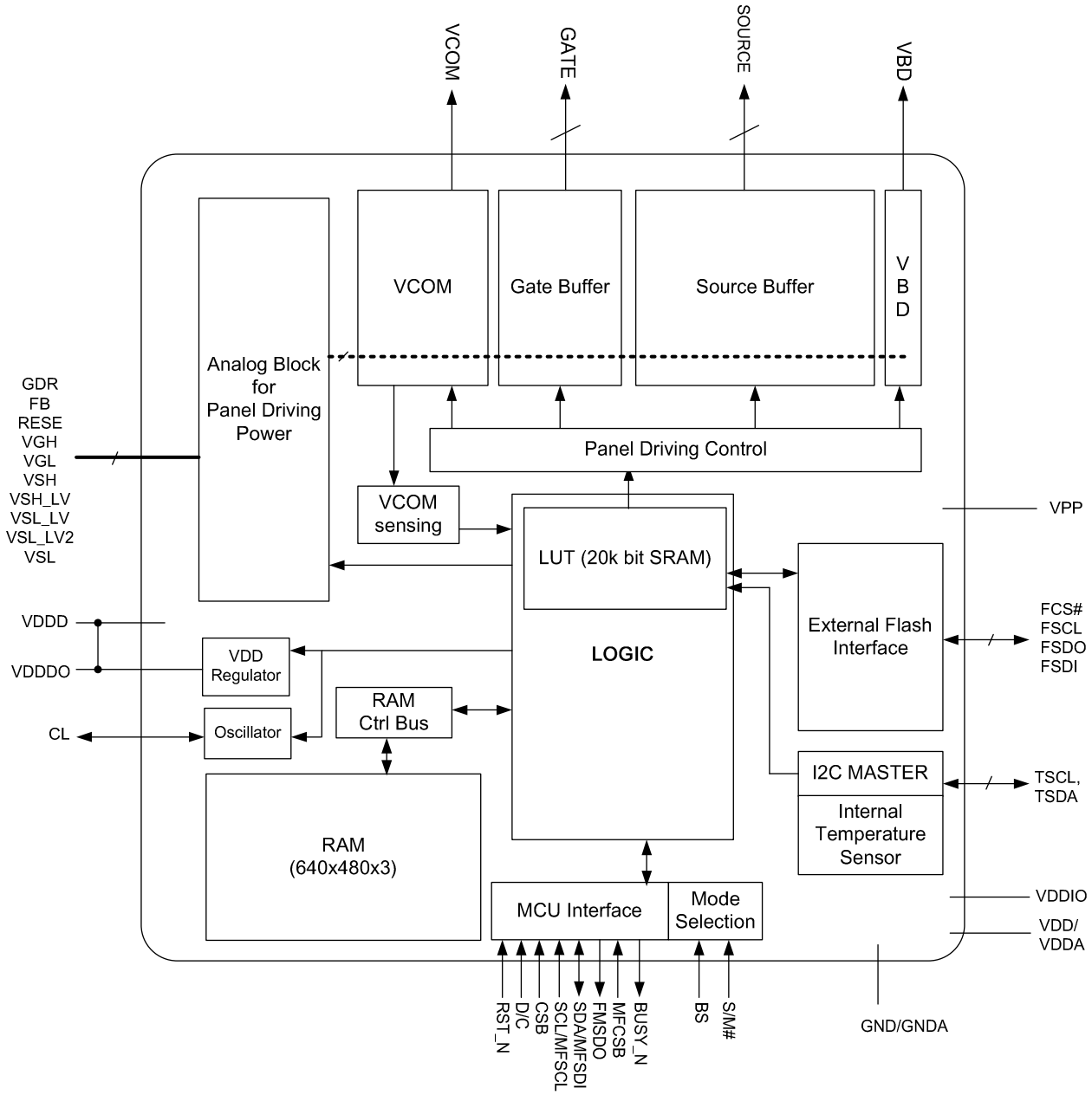


Figure 4-1 : SPD1656 Block Diagram

5 PIN DESCRIPTION

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to GND, Pull H = connect to V_{DDIO}

Pin name	Type	Connect to	Function	Description	When not in use
POWER SUPPLY					
VDD	P	Power Supply	Power Supply	Power input pin for the chip.	-
VDDA	P	Power Supply	Power Supply	Power input pin for the chip. - Connect to VDD in the application circuit.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the Interface. - Connect to VDD in the application circuit.	-
VDDD	P	Power Supply	Power for core logic	Core logic power pin - Connect to VDDDO in the application circuit.	-
VDDDO	C	Stabilizing capacitor	Regulator output for core logic	VDDDO (1.8V) can be regulated internally from VDD. - For the single chip application, a capacitor should be connected between VDDDO and GND under all circumstances. - For the cascade mode application, a capacitor should be connected between VDDDO and GND in the master chip under all circumstances. For the slave chip, the capacitor is not necessary as VDDDO will be supplied from the cascade master chip externally.	-
GND	P	GND	GND	Ground (Digital).	-
GNDA	P	GND	GND	Ground (Analog) - Connect to GND in the application circuit.	-
VPP	P	Reserved	Reserved	Reserved Keep it floating.	-
Digital IO					
SCL / MFSCL	I	MPU	Data Bus	Serial clock pin for interface: It would bypass to MFSCL by R65H command.	-
SDA / MFSDI	I/O	MPU	Data Bus	Serial data pin for interface: It would bypass to MFSDI by R65H command.	-
CSB	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU.	VDDIO or GND
D/C	I	MPU	Logic Control	This pin is Data/Command control pin connecting to the MCU.	VDDIO or GND
RST_N	I	MPU	System Reset	This pin is reset signal input. Active Low.	-
BUSY_N	O	MPU	Device Busy Signal	This pin indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver. In the cascade mode, the BUSY pin of the slave chip should be left open.	Open

<table>
<tr><th>Pin name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>S/M#</td><td>I</td><td>VDDIO/GND</td><td>Cascade Mode Selection</td><td>This pin is Master and Slave selection pin.
- For the single chip application, the S/M# pin should be connected to VSS.
- In the cascade mode:
For Master Chip, the S/M# pin should be connected to VSS.
For Slave Chip, the S/M# pin should be connected to VDDIO. The oscillator, booster and regulator circuits of the slave chip will be disabled. The corresponding pins including CL, VDDD, VDDIO, VGH, VGL, VSH, VSH_LV, VSL_LV, VSH_LV2, VSL and VCOM must be connected to the master chip.</td><td>-</td></tr>
<tr><td>CL</td><td>I/O</td><td>GND</td><td>Clock signal</td><td>This is the clock signal pin.
- For the single chip application, the CL pin should be tied GND.
- In the cascade mode, the CL pin of the slave chip should be connected to the CL pin of the master chip.</td><td>GND</td></tr>
<tr><td>BS</td><td>I</td><td>VDDIO/GND</td><td>MCU Interface Mode Selection</td><td>This pin is for selecting 3-wire or 4-wire SPI bus.
<table><tr><td>BS</td><td>MCU Interface</td></tr><tr><td>L</td><td>4-wire SPI</td></tr><tr><td>H</td><td>3-wire SPI(9 bits SPI)</td></tr></table></td><td>-</td></tr>
<tr><td>TSDA</td><td>I/O</td><td>Temperature sensor SDA</td><td>Interface to Digital Temp. Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Data pin.
External pull up resistor is required when connecting to I^2C slave.</td><td>Open</td></tr>
<tr><td>TSCL</td><td>O</td><td>Temperature sensor SCL</td><td>Interface to Digital Temp. Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Clock pin.
External pull up resistor is required when connecting to I^2C slave.</td><td>Open</td></tr>
<tr><td>FMSDO</td><td>O</td><td>MPU</td><td>Flash data output.</td><td>Serial communication data output.
It would bypass to FMSDO by R65H command.</td><td>Open</td></tr>
<tr><td>MFCSB</td><td>I</td><td>MPU</td><td>Flash chip select.</td><td>Serial communication chip select.
It would bypass to MFCSB by R65H command.</td><td>VDDIO or GND</td></tr>
<tr><td>FCSB</td><td>O</td><td rowspan="4">External SPI FLASH</td><td>Flash chip select.</td><td>Serial communication chip select for External Flash</td><td>Open</td></tr>
<tr><td>FSCL</td><td>O</td><td>Flash data clock</td><td>Serial communication clock output for External Flash</td><td>Open</td></tr>
<tr><td>FSDI</td><td>I</td><td>Flash data input</td><td>Serial communication data input for External Flash</td><td>VDDIO or GND</td></tr>
<tr><td>FSDO</td><td>O</td><td>Flash data output</td><td>Serial communication data output for External Flash</td><td>Open</td></tr>
</table>

Pin name	Type	Connect to	Function	Description	When not in use
Analog Pin					
GDR	O	POWER MOSFET Driver Control	VGH, VGL Generation	N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		Current sense input pin for the control Loop.	-
FB	I	Reserved		Reserved pin	Open
VGH	C	Stabilizing capacitor		Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and GND in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and GND in the application circuit.	-
VSH	C	Stabilizing capacitor	VSH, VSH_LV, VSL_LV, VSL_LV2, VSL Generation	This pin is Positive Source driving voltage, VSH Connect a stabilizing capacitor between VSH and GND in the application circuit.	-
VSH_LV	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH_LV Connect a stabilizing capacitor between VSH_LV and GND in the application circuit.	-
VSL_LV	C	Stabilizing capacitor		This pin is Negative Source driving voltage, VSL_LV Connect a stabilizing capacitor between VSL_LV and GND in the application circuit.	-
VSL_LV2	C	Stabilizing capacitor		This pin is Negative Source driving voltage, VSL_LV2. Connect a stabilizing capacitor between VSL_LV2 and GND in the application circuit.	-
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage, VSL. Connect a stabilizing capacitor between VSL and GND in the application circuit.	-
VCOM	C	Panel/ Stabilizing capacitor	VCOM Generation	These pins are VCOM driving voltage Connect a stabilizing capacitor between VCOM and GND in the application circuit.	-
Panel Driving					
S [639:0]	O	Panel	Source driving signal	Source output pin.	Open
G [479:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD [1:0]	O	Panel	Border driving signal	Border output pin.	Open
Others					
NC	NC	NC	Not Connected	Keep open. Don't connect with other NC pins.	Open
RSV	GND	GND	Reserved	This is a reserved pin, connect to GND	GND
TPL1, TPL2, TPL3, TPL4	NC	NC	Reserved	Reserved pins. - Keep open. - Don't connect to other NC pins and test pins	Open
TPA1, TPA2, TPA3, TPA4	NC	NC	Reserved	Reserved pins. - Keep open. - Don't connect to other NC pins and test pins	Open

6 Functional Block Description

6.1 MCU Interface

6.1.1 MCU Interface selection

The SPD1656 can support 3-wire/4-wire serial peripheral. In the SPD1656, the MCU interface is pin selectable by BS shown in Table 6-1.

Note

(1) L is connected to GND

(2) H is connected to V_{DDIO}

Table 6-1 : Interface pins assignment under different MCU interface

	Pin Name					
MCU Interface	**BS**	**RST_N**	**CSB**	**D/C**	**SCL**	**SDA**
4-wire serial peripheral interface (SPI)	Connect to GND	Required	Required	Required	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	Connect to VDDIO	Required	Required	Connect to GND	SCL	SDA

6.1.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C and CSB. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure 4-wire SPI is shown in Table 6-2

Table 6-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C pin	CSB pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C pin.

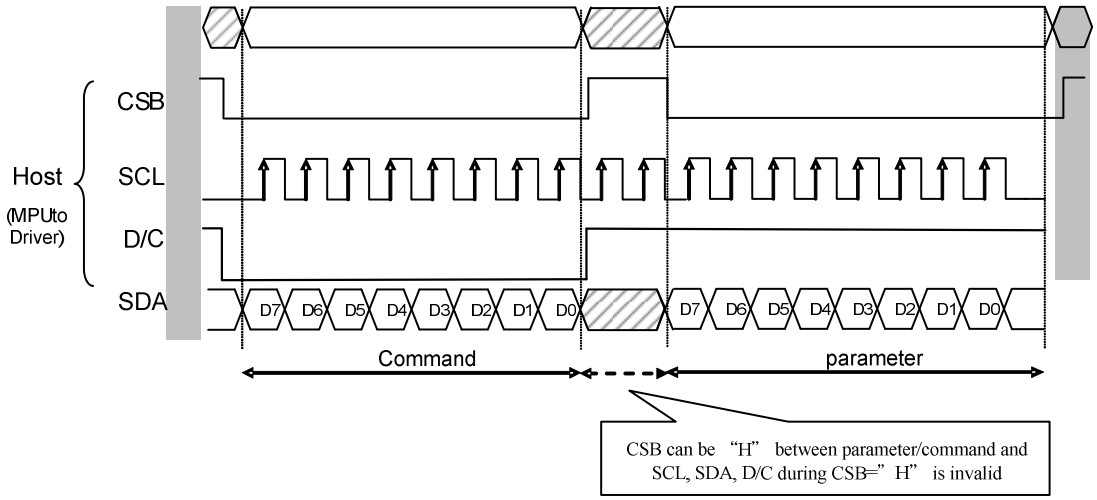


Figure 6-1 : Write procedure in 4-wire SPI mode

6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CSB. The operation is similar to 4-wire SPI while D/C pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C bit, D7 bit, D6 bit to D0 bit. The first bit is D/C bit which determines the following byte is command or data. When D/C bit is 0, the following byte is command. When D/C bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Table 6-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

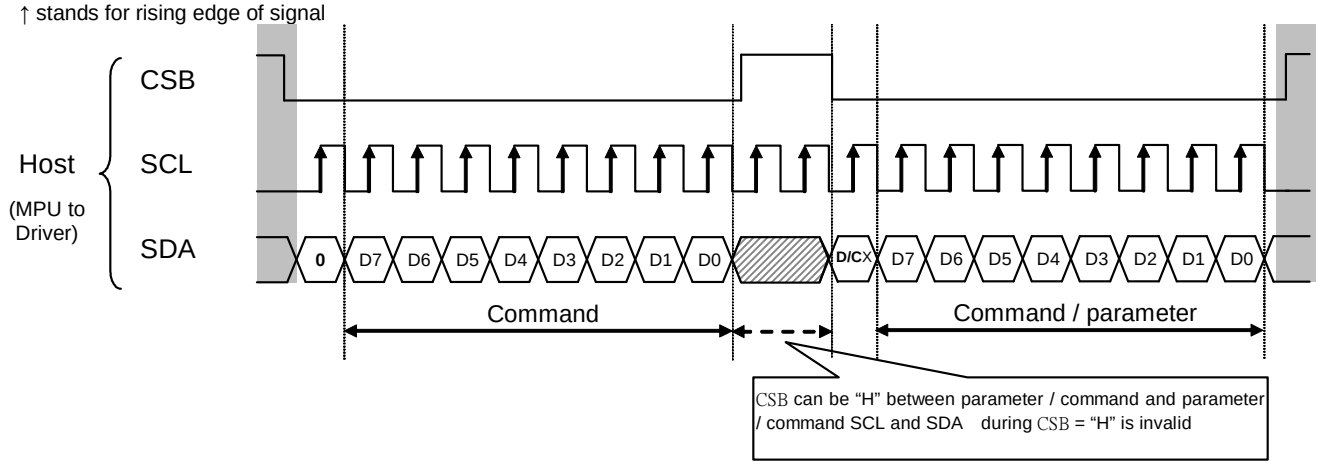


Figure 6-2 : Write procedure in 3-wire SPI mode

6.2 RAM

The On chip display RAM is holding the image data. 3bpp for 640x480 resolution
Ram content and LUT mapping is shown in below:

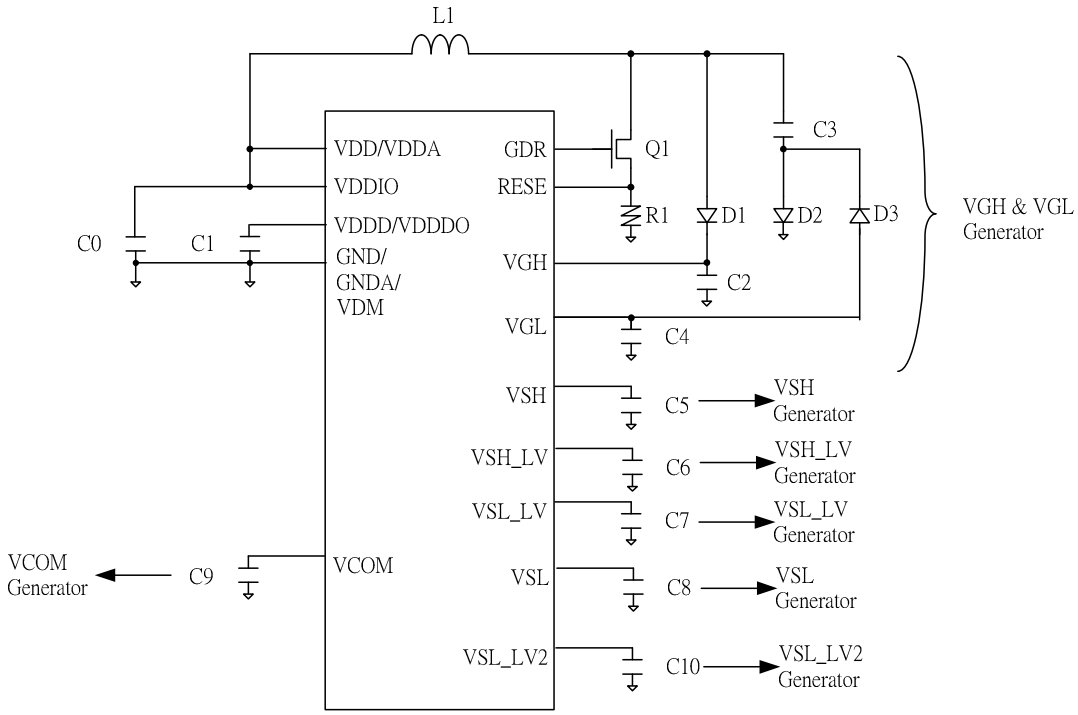
RAM content	LUTn	Refer to Register of LUT
000b	LUT0	LUTB (R21h)
001b	LUT1	LUTG1 (R23h)
010b	LUT2	LUTG2 (R24h)
011b	LUT3	LUTW (R22h)
100b	LUT4	LUTR0 (R25h)
101b	LUT5	LUTR1 (R26h)
110b	LUT6	LUTR2 (R27h)
111b	LUT7	LUTR3 (R28h)

6.3 Oscillator

The oscillator module generates the clock reference for waveform timing and analog operations.

6.4 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH, VSH_LV, VSL_LV, VSL_LV2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.



6.5 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into flash. It required PON for analog voltage ready.
The typical flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Source are GND.
- VCOM pin used for sensing.
- During Sensing period, BUSY_N is kept flagged.
- After Sensing, Active Gate return to non-select stage.

6.6 Gate waveform, Programmable Source and VCOM waveform

- There are 20 groups, each group contains 8 phases, totally 160 phases for programmable Source waveform with different phase length.

- The phase length of LUT0~LUT7, LUTVCOM, LUTXON is defined as TP[nX]
  - The range of TP[nX] is from 0 to 255.
  - n represents the Group number from 0 to 19; X represents the sub-group number from A to H.
  - TP[nX] = 0 indicates phase skipped.

- The repeat count of group is defined as RP[n], which is used for the count of repeating TP[nA] , TP[nB], TP[nC] , TP[nD], TP[nE] , TP[nF], TP[nG] and TP[nH];
  - The range of RP[n] is from 0 to 255.
  - n represents the Group number from 0 to 19;
  - RP[n] = 0 indicates No repeat, End of LUT

- Source/VCOM Voltage Level and XON setting are constant in each phase.

- VS [nX-LUTn] indicates the voltage in phase n for transition LUT0 ~ LUT7.
  - 000 – GND
  - 001 – VSH
  - 010 – VSL
  - 011 – VSH_LV
  - 100 – VSL_LV
  - 101 – VSL_LV2
  - 110 – Reserved
  - 111 – HiZ

- VS [nX- LUTVCOM] indicates the voltage in phase n for transition VCOM.
  - 00 – DCVCOM
  - 01 – VSH+DCVCOM
  - 10 – VSL+DCVCOM
  - 11 – HiZ

- VS [nX- LUTXON] indicates the voltage in phase n for XON selection.
  - 0 – All gate on [Gate keep High until the phase for normal gate scan]
  - 1 – Normal gate scan function

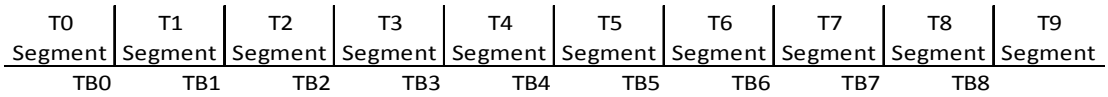
XON	1				0				0				1				1			
1st Gate	Scan	VGL	VGL	VGL	Scan	VGH	VGH	VGH	VGH	VGH	VGH	VGH	Scan	VGL	VGL	VGL	Scan	VGL	VGL	VGL
2nd Gate	VGL	Scan	VGL	VGL	VGL	Scan	VGH	VGH	VGH	VGH	VGH	VGH	VGH	Scan	VGL	VGL	VGL	Scan	VGL	VGL
	…				…				…				…				…			
Last Gate	VGL	VGL	VGL	Scan	VGL	VGL	VGL	Scan	VGH	VGH	VGH	VGH	VGH	VGH	VGH	Scan	VGL	VGL	VGL	Scan
	Scanning				Turn on one by on				Keep High				Turn off one by one				Scanning			

Figure 6-3 : Example of Gate output with XON setting change

6.7 Temperature Searching Mechanism

There are 10 temperature segments which could be selected by specifying TB0~TB8 (address: 25002~25010). The comparison

Order	Comparison Condition	Segment
1	Real Temp. < TB0	T0 Segment
2	TB0 ≦ Real Temp. < TB1	T1 Segment
3	TB1 ≦ Real Temp. < TB2	T2 Segment
4	TB2 ≦ Real Temp. < TB3	T3 Segment
5	TB3 ≦ Real Temp. < TB4	T4 Segment
6	TB4 ≦ Real Temp. < TB5	T5 Segment
7	TB5 ≦ Real Temp. < TB6	T6 Segment
8	TB6 ≦ Real Temp. < TB7	T7 Segment
9	TB7 ≦ Real Temp. < TB8	T8 Segment
10	TB8 ≦ Real Temp.	T9 Segment



The format of TB0~TB8 is as the below.

Bit7-0	Temperature (degC)
1011 0000b	-40
	…
1011 1010b	-35
	…
1101 1000b	-20
	…
1111 1110b	-1
0000 0000b	0
0000 0010b	1
	…
0011 0010b	25
	…
0111 1000b	60

6.8 External Temperature Sensor I2C Single Master Interface

The chip provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing.

TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor.

1. If the Temperature value MSByte bit D11 = 0, then
   the temperature is positive and value (DegC) = + (Temperature value) / 16
2. If the Temperature value MSByte bit D11 = 1, then
   the temperature is negative and value (DegC) = - (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
1100 1001 0000	C90	-880	-55
1100 1001 0010	C92	-878	-54.875
1110 0111 0000	E70	-400	-25
1111 1111 1110	FFE	-2	-0.125
0000 0000 0000	0	0	0
0000 0000 0010	2	2	0.125
0001 1001 0000	190	400	25
0111 1101 0000	7D0	2000	125
0111 1110 0010	7E2	2018	126.125
0111 1110 1110	7EE	2030	126.875
0111 1111 0000	7F0	2032	127

6.9 LUT (lookup table) Definition

Address		(Byte Count)		Address		Remark
0 : : :	Waveform LUT (T0~T9) (20800)	(2080)	T0	0~259 (260)	LUTB	See command LUTB (R21h) for details
				260~519 (260)	LUTW	LUTW (R22h)
				520~779 (260)	LUTG1	LUTG1 (R23h)
				780~1039 (260)	LUTG2	LUTG2 (R24h)
				1040~1299 (260)	LUTR0	LUTR0 (R25h)
				1300~1559 (260)	LUTR1	LUTR1 (R26h)
				1560~1819 (260)	LUTR2	LUTR2 (R27h)
				1820~2079 (260)	LUTR3	LUTR3 (R28h)
		(2080)	T1	2080~4159		(Same as T0)
		(2080)	T2	4160~6239		(Same as T0)
			:			
		(2080)	T8	16640~18719		(Same as T0)
20799		(2080)	T9	18720~20799		(Same as T0)
20800 : : :	VCOM LUT (T0~T9) (2200)	(220)	T0	20800~21019		See command LUTC (R20h) for details
		(220)	T1	21020~21239		
			:			
		(220)	T8	22560~22779		
22999		(220)	T9	22780~22999		
23000 : : :	XON LUT (T0~T9) (2000)	(200)	T0	23000~23199		See command LUTXON (R29h) for details
		(200)	T1	23200~23399		
			:			
		(200)	T8	24600~24799		
24999		(200)	T9	24800~24999		
25000		(2)		25000~25001		Reserved
25001						
25002 : 25010	Temperature Boundary (TB0~TB8)	(9)	--	25002~25010		
25011 : : : : 25030	T0_VSHC_LVL, T0_VSLC_LVL, : T9_VSHC_LVL, T9_VSLC_LVL	(20)	T0 : : T9	25011~25030		See VSH_LV/VSL_LV voltage setting (R01h)
25031 : : : : 25040	T0_LVL2_EN & VSLC_LVL2, T1_LVL2_EN & VSLC_LVL2, : T8_LVL2_EN & VSLC_LVL2, T9_LVL2_EN & VSLC_LVL2	(10)	T0 : : T9	25031~25040		See VSL_LV2 voltage setting (R01h)
25041~25599		(559)		25041~25599		TBD
25600	VCM_DC	(1)	--	25600		See VDCS voltage setting (R82h)
25601~25615		(15)		25601~25615		TBD
25616 : 25625	T0_Frame rate T1_Frame rate : T9_Frame rate	(10)	T0 : : T9	25616~25625		See PLL control setting (R30h)
Others						Reserved

6.10 Cascade Mode

The SPD1656 has a cascade mode that can cascade 2 chips to achieve the display resolution up to 1280 (sources) x 480 (gates). The pin S/M# is used to configure the chip. When S/M# is connected to GND, the chip is configured as a master chip. When S/M# is connected to VDDIO, the chip is configured as a slave chip.

When the chip is configured as a master chip, it will be the same as a single chip application, i.e., all circuit blocks will be worked as usual. When the chip is configured as a slave chip, its oscillator and booster & regulator circuit will be disabled. The oscillator clock and all booster voltages will be come from the master chip. Therefore, the corresponding pins including CL, VDDD, VGH, VGL, VSH, VSH_LV, VSL_LV, VSL_LV2, VSL, VGL and VCOM must be connected to the master chip.

7 COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

Command	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Registers	
PSR	W	0	0	0	0	0	0	0	0	0		00h
	W	1	#	#	#	-	#	#	#	#	RES[1:0], RESA, UD, SHL, SHD_N, RST_N	
	W	1	#	-	-	-	-	#	#	#	LUT_EN, VG_OFFstage, VCOM_OFFstage, VS_OFFstage	
PWR	W	0	0	0	0	0	0	0	0	1		01h
	W	1	-	-	-	-	#	#	#	#	VCM_HZ, VSC_EN, VS_EN, VG_EN	
	W	1	-	-	-	-	#	#	#	#	VG_LVL[1:0]	
	W	1	-	-	#	#	#	#	#	#	VSHC_LVL[5:0]	
	W	1	-	-	#	#	#	#	#	#	VSLC_LVL[5:0]	
	W	1	#	-	#	#	#	#	#	#	LVL2_EN, VSLC_LVL2[5:0]	
POF	W	0	0	0	0	0	0	0	1	0		02h
PFS	W	0	0	0	0	0	0	0	1	1		03h
	W	1	-	-	#	#	-	-	#	#	T_VDS_OFF[1:0],	
	W	1	-	-	#	#	#	#	#	#	VG_OFF[1:0], VCOM_OFF[1:0], VS_OFF[1:0]	
PON	W	0	0	0	0	0	0	1	0	0		04h
BTST	W	0	0	0	0	0	0	1	1	0		06h
	W	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	
	W	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	
	W	1	-	-	#	#	#	#	#	#	BT_PHC[5:0]	
DSLP	W	0	0	0	0	0	0	1	1	1		07h
	W	1	1	0	1	0	0	1	0	1	Check code	
DTM1	W	0	0	0	0	1	0	0	0	0		10h
	W	1	-	#	#	#	-	#	#	#	KPixel1[2:0], KPixel2[2:0]	
	W	1	..	..	..	..	..	..	..	..	…	
	W	1	-	#	#	#	-	#	#	#	Kpixel[2M-1][2:0], Kpixel[2M][2:0]	
DSP	W	0	0	0	0	1	0	0	0	1		11h
	R	1	#	-	-	-	-	-	-	-	Data_flag	
DRF	W	0	0	0	0	1	0	0	1	0		12h
WINM	W	0	0	0	0	1	0	1	0	0		14h
	W	1	-	-	-	-	-	-	-	#	WINM	
WHRES	W	0	0	0	0	1	0	1	0	1		15h
	W	1	-	-	-	-	-	-	#	#	WHRESSTART[9:0]	
	W	1	#	#	#	#	#	#	#	#		
	W	1	-	-	-	-	-	-	#	#	WHRESEND[9:0]	
	W	1	#	#	#	#	#	#	#	#		
WVRES	W	0	0	0	0	1	0	1	1	0		16h
	W	1	-	-	-	-	-	-	-	#	WVRESSTART[8:0]	
	W	1	#	#	#	#	#	#	#	#		
	W	1	-	-	-	-	-	-	-	#	WVRESEND[8:0]	
	W	1	#	#	#	#	#	#	#	#		
LUTC	W	0	0	0	1	0	0	0	0	0		20h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	#	#	#	#	#	#	#	#	1stLVL[1:0], 2nd, 3rd, 4th	
	W	1	#	#	#	#	#	#	#	#	5th, 6th, 7th, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTB	W	0	0	0	1	0	0	0	0	1		21h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	-	#	#	#	-	#	#	#	1stLVL[2:0], 2nd,	
	W	1	-	#	#	#	-	#	#	#	3rd, 4th	
	W	1	-	#	#	#	-	#	#	#	5th, 6th,	
	W	1	-	#	#	#	-	#	#	#	7th, 8th	

	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTW	W	0	0	0	1	0	0	0	1	0		22h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	-	#	#	#	-	#	#	#	1stLVL[2:0], 2nd,	
	W	1	-	#	#	#	-	#	#	#	3rd, 4th	
	W	1	-	#	#	#	-	#	#	#	5th, 6th,	
	W	1	-	#	#	#	-	#	#	#	7th, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTG1	W	0	0	0	1	0	0	0	1	1		23h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	-	#	#	#	-	#	#	#	1stLVL[2:0], 2nd,	
	W	1	-	#	#	#	-	#	#	#	3rd, 4th	
	W	1	-	#	#	#	-	#	#	#	5th, 6th,	
	W	1	-	#	#	#	-	#	#	#	7th, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTG2	W	0	0	0	1	0	0	1	0	0		24h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	-	#	#	#	-	#	#	#	1stLVL[2:0], 2nd,	
	W	1	-	#	#	#	-	#	#	#	3rd, 4th	
	W	1	-	#	#	#	-	#	#	#	5th, 6th,	
	W	1	-	#	#	#	-	#	#	#	7th, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTR0	W	0	0	0	1	0	0	1	0	1		25h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	-	#	#	#	-	#	#	#	1stLVL[2:0], 2nd,	
	W	1	-	#	#	#	-	#	#	#	3rd, 4th	
	W	1	-	#	#	#	-	#	#	#	5th, 6th,	
	W	1	-	#	#	#	-	#	#	#	7th, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	

	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTR1	W	0	0	0	1	0	0	1	1	0		26h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	-	#	#	#	-	#	#	#	1stLVL[2:0], 2nd,	
	W	1	-	#	#	#	-	#	#	#	3rd, 4th	
	W	1	-	#	#	#	-	#	#	#	5th, 6th,	
	W	1	-	#	#	#	-	#	#	#	7th, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTR2	W	0	0	0	1	0	0	1	1	1		27h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	-	#	#	#	-	#	#	#	1stLVL[2:0], 2nd,	
	W	1	-	#	#	#	-	#	#	#	3rd, 4th	
	W	1	-	#	#	#	-	#	#	#	5th, 6th,	
	W	1	-	#	#	#	-	#	#	#	7th, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTR3	W	0	0	0	1	0	1	0	0	0		28h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	-	#	#	#	-	#	#	#	1stLVL[2:0], 2nd,	
	W	1	-	#	#	#	-	#	#	#	3rd, 4th	
	W	1	-	#	#	#	-	#	#	#	5th, 6th,	
	W	1	-	#	#	#	-	#	#	#	7th, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
LUTXON	W	0	0	0	1	0	1	0	0	1		29h
	W	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	
	W	1	#	#	#	#	#	#	#	#	1stXON[0], 2nd, …, 8th	
	W	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	
	W	1	#	#	#	#	#	#	#	#	2nd	
	W	1	#	#	#	#	#	#	#	#	3rd	
	W	1	#	#	#	#	#	#	#	#	4th	
	W	1	#	#	#	#	#	#	#	#	5th	
	W	1	#	#	#	#	#	#	#	#	6th	
	W	1	#	#	#	#	#	#	#	#	7th	
	W	1	#	#	#	#	#	#	#	#	8th	
PLL	W	0	0	0	1	1	0	0	0	0		30h
	W	1	-	-	#	#	#	#	#	#	M[2:0], N[2:0]	
TSC	W	0	0	1	0	0	0	0	0	0		40h
	R	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:1]	
	R	1	#	#	#	-	-	-	-	-	D[2:0] / TS[0]	
TSE	W	0	0	1	0	0	0	0	0	1		41h
	W	1	#	-	-	-	#	#	#	#	TSE, TO[3:0]	

TSW	W	0	0	1	0	0	0	0	1	0		42h
	W	1	#	#	#	#	#	#	#	#	WATTR[7:0]	
	W	1	#	#	#	#	#	#	#	#	WMSB[7:0]	
	W	1	#	#	#	#	#	#	#	#	WLSB[7:0]	
TSR	W	0	0	1	0	0	0	0	1	1		43h
	R	1	#	#	#	#	#	#	#	#	RMSB[7:0]	
	R	1	#	#	#	#	#	#	#	#	RLSB[7:0]	
CDI	W	0	0	1	0	1	0	0	0	0		50h
	W	1	#	#	#	1	#	#	#	#	VBD[2:0], CDI[3:0]	
LPD	W	0	0	1	0	1	0	0	0	1		51h
	R	1	-	-	-	-	-	-	-	#	LPD	
TCON	W	0	0	1	1	0	0	0	0	0		60h
	W	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	
TRES	W	0	0	1	1	0	0	0	0	1		61h
	W	1	-	-	-	-	-	-	#	#	HRES[9:0]	
	W	1	#	#	#	#	#	#	#	#		
	W	1	-	-	-	-	-	-	-	#	VRES[8:0]	
	W	1	#	#	#	#	#	#	#	#		
DAM	W	0	0	1	1	0	0	1	0	1		65h
	W	1	-	-	-	-	-	-	-	#	DAM	
FLG	W	0	0	1	1	1	0	0	0	0		71h
	R	1	-	-	#	#	#	#	#	#	I^2C_ERR, I^2C_BUSYN,DATA_FLAG, PON, POF, BUSY_N	
AMV	W	0	1	0	0	0	0	0	0	0		80h
	W	1	#	#	#	#	#	#	#	#	AMVT[3:0], AMVX, AMVS, VDCS_AMV,AMVE	
VV	W	0	1	0	0	0	0	0	0	1		81h
	R	1	-	#	#	#	#	#	#	#	VV[6:0]	
VDCS	W	0	1	0	0	0	0	0	1	0		82h
	W	1	-	#	#	#	#	#	#	#	VDCS[6:0]	
CCSET	W	0	1	1	1	0	0	0	0	0		E0h
	W	1	#	#	#	#	#	#	#	#	CCSET[7:0]	
PWS	W	0	1	1	1	0	0	0	1	1		E3h
	W	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	

Note:

(1) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(2) Commands are processed on the 'stop' condition of the interface.

(3) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

(4) All write commands are "UNAVAILABLE" when BUSY_N=0 is asserted by DSP (R11h), DRF (R12h) or PON(R04h) or POF(R02h) or TSC(R40h) or LPD(R51h) or AMV(R80h). All read commands are always "AVAILABLE".

* AVAILABLE means that Host can send command/parameter to driver.
* UNAVAILABLE means that Host cannot send command/parameter to driver.

(5) Commands or Parameter not shown in above table are reserved.

(6) All write and read commands are only valid after normal power on sequence listed in Session 9.1 Power on Sequence Display.

8 COMMAND DESCRIPTION

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	A[7:0] = 07h [POR] B[7:0] = 08h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:6] ~ RES[1:0] A[5] ~ RESA Display Resolution setting (source x gate) RESA=1: 00b: 640x480; 01b: 600x450; 10b: 640x448; 11b: 600x448 RESA=0: 00b: 640x240(Default); 01b: 600x240; 10b: 640x320; 11b: 600x320 *Remark: non-select Gate keep at VGL for DSP/DRF and AMV A[4] ~ Reserved. A[3] ~ UD Gate Scan Direction: 0: Scan down. (Default) First line to Last line: Gn-1 … G0 1: Scan up. First line to Last line: G0 … Gn-1 *Remark: non-select Gate keep at VGL for DSP/DRF and AMV A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 … S0 1: Shift right. (Default) First data to Last data: S0 … Sn-1 *Remark: inactive source follow LUTC for DSP/DRF A[1] ~ SHD_N Booster and Regulator Switch: 0: Booster and Regulator OFF 1: Booster and Regulator ON (Default) *Remark: SHD_N works at Command (0x04) PON only A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. 1: Normal operation (Default). Booster OFF, Register data are set to their default values, and SOURCE/VBD/VCOM: 0V When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable.

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		B_7	0	0	0	0	B_2	B_1	B_0		B[7] ~ LUT_SEL When DSP/DRF. LUT selection: 0: LUT from flash (Default) 1: LUT from register B[2] ~ VG_OFF stage control Gate power [VGH/ VGL] Off stage triggered by POF (R02) 0 : VGH=VDD, VGL=0V (default) 1 : Floating B[1] ~ Vcom_OFF stage control Vcom power Off stage triggered by POF (R02) 0 : 0V (default) 1 : Floating B[0] ~ VS_OFF stage control Source power [VSH/ VSL/ VSH_LV/ VSL_LV/ VSL_LV2] Off stage triggered by POF (R02) 0 : 0V (default) 1 : Floating
0	0	01	0	0	0	0	0	0	0	1	PWR	A[3:0] = 08h [POR] B[3:0] = 01h [POR] C[5:0] = 05h [POR] D[5:0] = 05h [POR] E[7:0] = 05h [POR]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		A[3] ~ VCM_HZ VCOM Hi-Z function: 0: VCOM normal output. 1: VCOM floating. (default) A[2] ~ VS_EN Source power selection: 0 : External source power from VSH and VSL pin. (default) 1 : Internal DCDC function for generate source power. A[1] ~ VSC_EN Source LV power selection: 0 : External source LV power from VSH_LV and VSL_LV and VSL_LV2 pin. (default) 1 : Internal DCDC function for generate source LV power. A[0] ~ VG_EN Gate power selection: 0 : External gate power from VGH and VGL pin. (default) 1 : Internal DCDC function for generate gate power.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		0	0	0	0	B_3	B_2	B_1	B_0		B[3:2] ~ Reserved B[1:0] ~ VG_LVL[1:0] Internal VGH / VGL Voltage Level Selection: VG_LVL[1:0] | Gate Voltage Level 00 | VGH=20V 01 | VGH=19V (Default) 10 | VGH=18V 11 | VGH=17V
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		C[5:0] ~ VSHC_LVL[5:0] Internal VSH_LV Voltage Level Selection for Red LUT: VSHC_LVL[5:0] | VSH_LV Voltage Level 00h | 3.0V 01h | 3.2V 02h | 3.4V 03h | 3.6V 04h | 3.8V 05h | 4.0V(default) : | : 3Bh | 14.8V 3Ch | 15.0V Other | Reserved
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[5:0] ~ VSLC_LVL[5:0] Internal VSL_LV Voltage Level Selection for Red LUT: VSLC_LVL[5:0] | VSL_LV Voltage Level 00h | -3.0V 01h | -3.2V 02h | -3.4V 03h | -3.6V 04h | -3.8V 05h | -4.0V(default) : | : 3Bh | -14.8V 3Ch | -15.0V Other | Reserved
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		E[7] ~ LVL2_EN Internal VSL_LV2 regulator control: 0: Disable (Default) 1: Enable E[5:0] ~ VSLC_LVL2[5:0] Internal VSL_LV2 Voltage Level Selection for Red LUT: VSLC_LVL2[5:0] | VSL_LV2 Voltage Level 00h | -3.0V 01h | -3.2V 02h | -3.4V 03h | -3.6V 04h | -3.8V 05h | -4.0V(default) : | : 3Bh | -14.8V 3Ch | -15.0V Other | Reserved

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	02	0	0	0	0	0	0	1	0	POF	After power off command, driver will power off based on the Power OFF Sequence, BUSY_N signal will become “0”. The Power OFF command will turn off DCDC, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. It may have two conditions: 0V or floating. *Remark: POF works at PON only
0	0	03	0	0	0	0	0	0	1	1	PFS	A[7:0] = 00h [POR] B[7:0] = 21h [POR]
0	1		0	0	A_5	A_4	0	0	0	0		A[5:4] ~ T_VDS_OFF[1:0] Power OFF Sequence of VSH /VSL and VGH/VGL: T_VDS_OFF[1:0] / Off Sequence setting1 00 / 1 frame (Default) 01 / 2 frames 10 / 3 frames 11 / 4 frames
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		B[5:4] ~ VG_OFF[1:0] Gate power off timing after POF: VG_OFF[1:0]*TVDS_OFF[1:0] VG_OFF[1:0] / Off Sequence setting2 00 / 0 01 / 1 10 / 2 (Default) 11 / Reserved B[3:2] ~ VCOM_OFF[1:0] VCOM power off timing after POF: VCOM_OFF[1:0]*TVDS_OFF[1:0] VCOM_OFF[1:0] / Off Sequence setting2 00 / 0 (Default) 01 / 1 10 / 2 11 / Reserved B[1:0] ~ VS_OFF[1:0] Source power off timing after POF: VS_OFF[1:0]*TVDS_OFF[1:0] VS_OFF[1:0] / Off Sequence setting2 00 / 0 01 / 1 (Default) 10 / 2 11 / Reserved

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	PON	After the Power ON command, driver will power on based on the Power ON Sequence. After power on command and all power sequence are ready, then BUSY_N signal will become “1”. * Remark: PON Include 1) Load TS, 2) Load LUT (GATE/SOURCE VOLTAGE), VDCS, PLL 3) Analog On With default BTST, timing is <50ms
0	0	06	0	0	0	0	0	1	1	0	BTST	A[7:0] = 17h [POR] B[7:0] = 17h [POR] C[5:0] = 17h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:6] ~ BTPHA[7:6], B[7:6] ~ BTPHB[7:6]
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	C_5	C_4	C_3	C_2	C_1	C_0		

	Soft Start Phase Period (ms)
00	10
01	20
10	30
11	40

A[5:3] ~ BTPHA[5:3],
B[5:3] ~ BTPHB[5:3],
C[5:3] ~ BTPHC[5:3]

	Driving Strength
000b	(reserved)
001b	(reserved)
010b	1
011b	2
100b	3
101b	4
110b	5
111b	6(strongest)

A[2:0] ~ BTPHA[2:0],
B[2:0] ~ BTPHB[2:0],
C[2:0] ~ BTPHC[2:0]

	Driving Strength Minimum OFF Time (us)
000b	0.26 us
001b	0.31
010b	0.36
011b	0.52
100b	0.77
101b	1.61
110b	3.43
111b	6.77

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	07	0	0	0	0	0	1	1	1	DSLP	This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion. The only one parameter is a check code, the command would be executed if check code is A5h.
0	1		1	0	1	0	0	1	0	1		
0	0	10	0	0	0	1	0	0	0	0	DTM1	This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Stop command (R11H). Then the chip will start to send data/VCOM for panel. KPixel[2:0] Source Driver Output 000b Black 001b Gray1 010b Gray2 011b White 100b Red0 101b Red1 110b Red2 111b Red3
0	1		0	KPixel1[2:0]			0	KPixel2[2:0]				
:				:				:				
0	1		0	KPixel[2M-1] [2:0]			0	KPixel[2M] [2:0]				
0	0	11	0	0	0	1	0	0	0	1	DSP	To stop data transmission, this command must be issued to check the data flag. Data_flag: Data flag of receiving user data. 0: Driver didn't receive all the data. 1: Driver has already received all the one-frame data (DTM1). After "Data Stop" (11h) commands, BUSY_N signal will become "0" until display update is finished. A[7] ~ Data_flag
1	1		A_7	0	0	0	0	0	0	0		
0	0	12	0	0	0	1	0	0	1	0	DRF	After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY_N signal will become "0" until display update is finished.
0	0	14	0	0	0	1	0	1	0	0	WINM	A[0] = 0 [POR]
0	1		0	0	0	0	0	0	0	A_0		A[0]: WinM_EN Window Mode Enable: 0 -> normal mode [Default] 1 -> window mode * Remark: RAM data sent by DTM1 according to RAM_mode(CCSET_A[7]). The gate output are kept scanning for the window area defined by WVRES. For the source output within the window area, they will follow LUT [R21~R28]. For the source output outside the window area, they will follow LUTC [R20].

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	15	0	0	0	1	0	1	0	1	WHRES	A[9:0] = 000h [POR] B[9:0] = 27Fh [POR]
0	1		0	0	0	0	0	0	A_9	A_8		HRESStart [9:0]/ HRESEnd [9:0]: Set Horizontal resolution start/end line of the update window, HRESEnd must be larger HRESStart. If > 27Fh, work as 27Fh HRESStart should be the multiple of 8. HRESStart/ HRESEnd [2:0] will be masked as 0. WHRES cannot set outside of the RES/TRES Remark: WHRES will take effect after all 4 data byte received. After WHRES is ready, then BUSY_N signal will become "1"
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	B_9	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	16	0	0	0	1	0	1	1	0	WVRES	A[8:0] = 000h [POR] B[8:0] = 1DFh [POR]
0	1		0	0	0	0	0	0	0	A_8		A[8:0] ~ VRESStart [8:0] B[8:0] ~ VRESEnd [8:0] VRESStart [8:0]/ VRESEnd [8:0] : Set Vertical resolution start/end line of the update window, VRESEnd must be larger VRESStart. If > 1DFh, work as 1DFh WVRES cannot set outside of RES/TRES. Remark: WVRES will take effect after all 4 data byte received.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	20	0	0	1	0	0	0	0	0	LUTC	This command builds up VCOM Look-Up Table (LUT). This LUT includes 20 kinds of group, each group is of 11 bytes. Total parameter is 220 byte. All Parameter = 00h [POR] * Remark The number of Frame of LUTC need to have at least 1 Frame.
0	1		RP [7:0]								1st Group: 1st to 11th Parameter	Each group is made up 8 phases. 1st parameter: RP[7:0] ~ repeat number. 2nd and 3rd parameter: 1st LVL[1:0]…8th LVL[1:0] ~ Level selection of each phase. 4th and 11th parameter: 1st TP[7:0]…8th TP[7:0] ~ No of Frame of each phase.
0	1		1st LVL [1:0]		2nd LVL [1:0]		3rd LVL [1:0]		4th LVL [1:0]			
0	1		5th LVL [1:0]		6th LVL [1:0]		7th LVL [1:0]		8th LVL [1:0]			
0	1		1st TP[7:0]									
0	1		2nd TP[7:0]									
0	1		3rd TP[7:0]									
0	1		4th TP[7:0]									
0	1		5th TP[7:0]									
0	1		6th TP[7:0]									
0	1		7th TP[7:0]									
0	1		8th TP[7:0]									
0	1		12th to 22th Parameter								2nd Group	
0	1		23th to 33th Parameter								3rd Group	
			…								…	
0	1		199th to 209th Parameter								19th Group	
0	1		210th to 220th Parameter								20th Group	

Item	Description
RP[7:0]	00h ~ No Repeat, End of LUT. 01h ~ Sum of (1st TP to 8th TP) x 1 02h ~ Sum of (1st TP to 8th TP) x 2 … FFh ~ Sum of (1st TP to 8th TP) x 255
LVL[1:0]	00: VCOM_DC 01: VSH + VCOM_DC [VCOMH] 10: VSL + VCOM_DC [VCOML] 11: HIZ (For last phase to control end level)
TP[7:0]	00h ~ Phase Skip 01h ~ 1 Frame 02h ~ 2 Frames … FFh ~ 255 Frame

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	21	0	0	1	0	0	0	0	1	LUTB	This command builds LUTB for black. This LUT includes 20 kinds of group, each group is of 13 bytes. Total parameter is 260 byte. All Parameter = 00h [POR]
0	1		RP [7:0]								1st Group: 1st to 13th Parameter	Each group is made up 8 phases. 1st parameter: RP[7:0] ~ repeat number. 2nd and 5th parameter: 1st LVL[2:0]…8th LVL[2:0] ~ Level selection of each phase. 6th and 13th parameter: 1st TP[7:0]…8th TP[7:0] ~ No of Frame of each phase.
0	1		0	1st LVL[2:0]		0		2nd LVL[2:0]				
0	1		0	3rd LVL[2:0]		0		4th LVL[2:0]				
0	1		0	5th LVL[2:0]		0		6th LVL[2:0]				
0	1		0	7th LVL[2:0]		0		8th LVL[2:0]				
0	1		1st TP[7:0]									
0	1		2nd TP[7:0]									
0	1		3rd TP[7:0]									
0	1		4th TP[7:0]									
0	1		5th TP[7:0]									
0	1		6th TP[7:0]									
0	1		7th TP[7:0]									
0	1		8th TP[7:0]									
0	1		14th to 26th Parameter								2nd Group	
0	1		27th to 39th Parameter								3rd Group	
			…								…	
0	1		235th to 247th Parameter								19th Group	
0	1		248th to 260th Parameter								20th Group	

Item	Description
RP[7:0]	00h ~ No Repeat, End of LUT. 01h ~ Sum of (1st TP to 8th TP) x 1 02h ~ Sum of (1st TP to 8th TP) x 2 … FFh ~ Sum of (1st TP to 8th TP) x 255
LVL[1:0]	000: VSS 001: VSH 010: VSL 011: VSH_LV 100: VSL_LV 101: VSL_LV2 110: Reserve 111: HIZ(For last phase to control end level)
TP[7:0]	00h ~ Phase Skip 01h ~ 1 Frame 02h ~ 2 Frames … FFh ~ 255 Frame

0	0	22	0	0	1	0	0	0	1	0	LUTW	This command builds LUT for White. This LUT includes 20 kinds of group, each group is of 13 bytes. Total parameter is 260 byte. Please refer to register 0x21 (LUTB) for similar definition details
0	0	23	0	0	1	0	0	0	1	1	LUTG1	This command builds LUT for Gray 1. This LUT includes 20 kinds of group, each group is of 13 bytes. Total parameter is 260 byte. Please refer to register 0x21 (LUTB) for similar definition details
0	0	24	0	0	1	0	0	1	0	0	LUTG2	This command builds LUT for Gray 2. This LUT includes 20 kinds of group, each group is of 13 bytes. Total parameter is 260 byte. Please refer to register 0x21 (LUTB) for similar definition details
0	0	25	0	0	1	0	0	1	0	1	LUTR0	This command builds LUT for Red 0. This LUT includes 20 kinds of group, each group is of 13 bytes. Total parameter is 260 byte. Please refer to register 0x21 (LUTB) for similar definition details
0	0	26	0	0	1	0	0	1	1	0	LUTR1	This command builds LUT for Red 1. This LUT includes 20 kinds of group, each group is of 13 bytes. Total parameter is 260 byte. Please refer to register 0x21 (LUTB) for similar definition details

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	27	0	0	1	0	0	1	1	1	LUTR2	This command builds LUT for Red 2. This LUT includes 20 kinds of group, each group is of 13 bytes. Total parameter is 260 byte. Please refer to register 0x21 (LUTB) for similar definition details
0	0	28	0	0	1	0	1	0	0	0	LUTR3	This command builds LUT for Red 3. This LUT includes 20 kinds of group, each group is of 13 bytes. Total parameter is 260 byte. Please refer to register 0x21 (LUTB) for similar definition details
0	0	29	0	0	1	0	1	0	0	1	LUTXON	This command builds LUT for XON. This LUT includes 20 kinds of group, each group is of 10 bytes. Total parameter is 200 byte. All Parameter = 00h [POR]
0	1		RP [7:0]								1st Group: 1st to 10th Parameter	Each group is made up 8 phases. 1st parameter: RP[7:0] ~ repeat number. 2nd and 3rd parameter: 1st XON…8th XON ~ XON selection of each phase. 4th and 11th parameter: 1st TP[7:0]…8th TP[7:0] ~ No of Frame of each phase.
0	1		1st XON	2nd XON	3rd XON	4th XON	5th XON	6th XON	7th XON	8th XON		
0	1		1st TP[7:0]									
0	1		2nd TP[7:0]									
0	1		3rd TP[7:0]									
0	1		4th TP[7:0]									
0	1		5th TP[7:0]									
0	1		6th TP[7:0]									
0	1		7th TP[7:0]									
0	1		8th TP[7:0]									
0	1		11th to 20th Parameter								2nd Group	
0	1		21th to 30th Parameter								3rd Group	
			…								…	
0	1		181th to 190th Parameter								19th Group	
0	1		191th to 200th Parameter								20th Group	

Item	Description
RP[7:0]	00h ~ No Repeat, End of LUT. 01h ~ Sum of (1st TP to 8th TP) x 1 02h ~ Sum of (1st TP to 8th TP) x 2 … FFh ~ Sum of (1st TP to 8th TP) x 255
XON	0: All gate on 1: Normal gate scan function Detail refer to Figure 6-3 : Example of Gate output with XON setting change
TP[7:0]	00h ~ Phase Skip 01h ~ 1 Frame 02h ~ 2 Frames … FFh ~ 255 Frame

0	0	30	0	0	1	1	0	0	0	0	PLL	The command controls the clock frequency. A[5:0] = 3Ch [POR]
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		It supports the following frame rates.

A[5:0]	Frame Rate Selection
00h	12.5Hz
01h	25 Hz
…	…
0Eh	187.5Hz
0Fh	200Hz
39h	200Hz
3Ah	100Hz
3Ch	50Hz
Other	50Hz

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	40	0	1	0	0	0	0	0	0	TSC	This command enables internal or external temperature sensor. BUSY_N will be goes low during temperature sensor is under operation. Then the temperature value can be read. When TSE (R41h) is set to 0, this command reads internal temperature sensor value. A[11:4] ~ TS [7:0]
1	1		A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
1	1		A_3	A_2	A_1	A_0	0	0	0	0		

TS [7:0]	Return Value
E7h	-25degC
E8h	-24degC
…	…
FFh	-1degC
00h	0degC
…	…
18h	24degC
19h	25degC
…	…
3Bh	59degC
3Ch	60degC

When TSE (R41h) is set to 1, this command reads external temperature sensor value.
A[11:0] ~ Return the value according to Session 6.8 External Temperature Sensor I2C Single Master Interface

0	0	41	0	1	0	0	0	0	0	1	TSE	This command selects Internal or External temperature sensor. A[7:0] = 00h [POR]
0	1		A_7	0	0	0	A_3	A_2	A_1	A_0		A[7] ~ TSE Internal temperature sensor switch: 0: Select internal temperature sensor (default) 1: Select external temperature sensor. A[3:0] ~ TO[3:0] Temperature offset:

TO[3:0]	Calculation	TO[3:0]	Calculation
0000	+0	1000	-8
0001	+1	1001	-7
0010	+2	1010	-6
0011	+3	1011	-5
0100	+4	1100	-4
0101	+5	1101	-3
0110	+6	1110	-2
0111	+7	1111	-1

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	42	0	1	0	0	0	0	1	0	TSW	This command could write data to the external temperature sensor. A[7:0] = 00h [POR] B[7:0] = 00h [POR] C[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:0] ~ WATTR [7:0] WATTR [7:6]: I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter) WATTR [5:3]: User-defined address bits (A2, A1, A0) WATTR [2:0]: Pointer setting B[7:0] ~ WMSB[7:0]: 1st parameter of write-data to external temperature sensor C[7:0] ~ WLSB[7:0]: 2nd parameter of write-data to external temperature sensor
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	43	0	1	0	0	0	0	1	1	TSR	This command read data from the external temperature sensor A[7:0] = RMSB[7:0] : MSByte of read-data from external temperature sensor B[7:0] = RLSB[7:0] : LSByte of read-data from external temperature sensor
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	50	0	1	0	1	0	0	0	0	CDI	This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync). A[7:0] = 17h [POR] B[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	1	A_3	A_2	A_1	A_0		A[7:5]~VBD [2:0] Border Output Selection: VBD[2:0] / LUT: 000 Black (Default); 001 Gray1; 010 Gray2; 011 White; 100 Red0; 101 Red1; 110 Red2; 111 HIZ A[3:0] ~ CDI[3:0] CDI [3:0] / Vcom and Data Interval: 0h 17; 1h 16; 2h 15; 3h 14; 4h 13; 5h 12; 6h 11; 7h 10 (Default); 8h 9; 9h 8; Ah 7; Bh 6; Ch 5; Dh 4; Eh 3; Fh 2
0	1		B_7	B_6	B_5	B_4	0	0	0	0		B[7] ~ VBD[7] Select GS Transition/ Fix Level for VBD 0-> Select GS Transition for VBD[2:0] during display (Default) 1-> Select FIX level Setting VBD[6:4] for VBD VBD[6:4] / Fix Level Setting for VBD: 000 VSS; 001 VSH; 010 VSL; 011 VSH_LV; 100 VSL_LV; 101 VSL_LV2; 110 VCOM; 111 HIZ
0	0	51	0	1	0	1	0	0	0	1	LPD	This command indicates the input power condition. Host can read this flag to learn the battery condition.
1	1		0	0	0	0	0	0	0	A_0		BUSY_N will be goes low during input power condition is under operation. Then the LPD status can be read. A[0] ~ LPD status Internal temperature sensor switch: 0: Low power input (VDD<2.5V) 1: Normal status (default)

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	60	0	1	1	0	0	0	0	0	TCON	This command defines non-overlap period of Gate and Source. A[7:0] = 22h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] ~ S2G[3:0] Source to Gate Non-overlap period A[3:0] ~ G2S[3:0] Gate to Source Non-overlap period D[3:0] / Period / D[3:0] / Period 0000 / 4 unit / 1000 / 36 unit 0001 / 8 unit / 1001 / 40 unit 0010 / 12 unit (Default) / 1010 / 44 unit 0011 / 16 unit / 1011 / 48 unit 0100 / 20 unit / 1100 / 52 unit 0101 / 24 unit / 1101 / 56 unit 0110 / 28 unit / 1110 / 60 unit 0111 / 32 unit / 1111 / 64 unit Each time unit = 500ns.
0	0	61	0	1	1	0	0	0	0	1	TRES	This command defines alternative resolution Refer to RESA [POR]
0	1		0	0	0	0	0	0	A_9	A_8		A[9:0] ~ HRES[9:0] Horizontal Display Resolution Remark: Horizontal resolution should be 8-multiple. B[8:0] ~ VRES[8:0] Vertical Display Resolution Remark: 1) TRES needs all 4 data byte to take effect. 2) The Data byte will be updated after RES command (register 0x00) 3) VRES[8:0] >= 240
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	65	0	1	1	0	0	1	0	1	DAM	This command defines how MCU host directly access external flash/EEPROM mode.
0	1		0	0	0	0	0	0	0	A_0		A[0] ~ DAM[POR=0] 0: Disable (Default) 1: Enable. By pass MFSCL*, MFSDI*, FMSDO*, and MFCSB* to external flash.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	71	0	1	1	1	0	0	0	1	FLG	This command reads the IC status. A[7:0] = 13h [POR]
1	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		A[5] ~ I2C_ERR: I2C master error status A[4] ~ I2C_BUSYN: I2C master busy status (low active) A[3] ~ Data_flag: Driver has already received all the one frame data A[2] ~ PON: Power ON status A[1] ~ POF: Power OFF status A[0] ~ BUSY_N: Driver busy status (low active)
0	0	80	1	0	0	0	0	0	0	0	AMV	This command implements related VCOM sensing setting. A[7:0] = 40h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	0	A_0		A[7:4] ~ AMVT[3:0] Auto Measure Vcom Time: min 5frame (100ms) , with extra gate scanning time from 0second to 15second A[3] ~ AMVX Gate scan setting for AMV: 0: After Measure VCOM, Gate scan will be disable (default) 1: After Measure VCOM, Gate scan keep enable. Remark: when this bit is set 1. It needs user to set back to 0 for the last AMV command issued. A[2] ~ AMVS Source output of AMV: 0: Set Source output to 0V during Auto Measure VCOM period. (default) 1: Set Source output to VSH_LV during Auto Measure VCOM period. A[0] ~ AMVE Auto Measure Vcom Enable (/Disable) : 0: Disabled (Default) 1: Enabled Remark: 1) AMV works at PON only 2) BUSY_N become low after AMC command, Vcom value will be updated to both VV and VDCS.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	81	1	0	0	0	0	0	0	1	VV	This command gets the Vcom value after AMV.
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[6:0] ~ VV[6:0]: Vcom read Value

VV[6:0]	Vcom read value
00h	Reserved
01h	Reserved
02h	-0.10V
03h	-0.15V
04h	-0.20V
…	…
50h	-4.00V
others	-4.00V

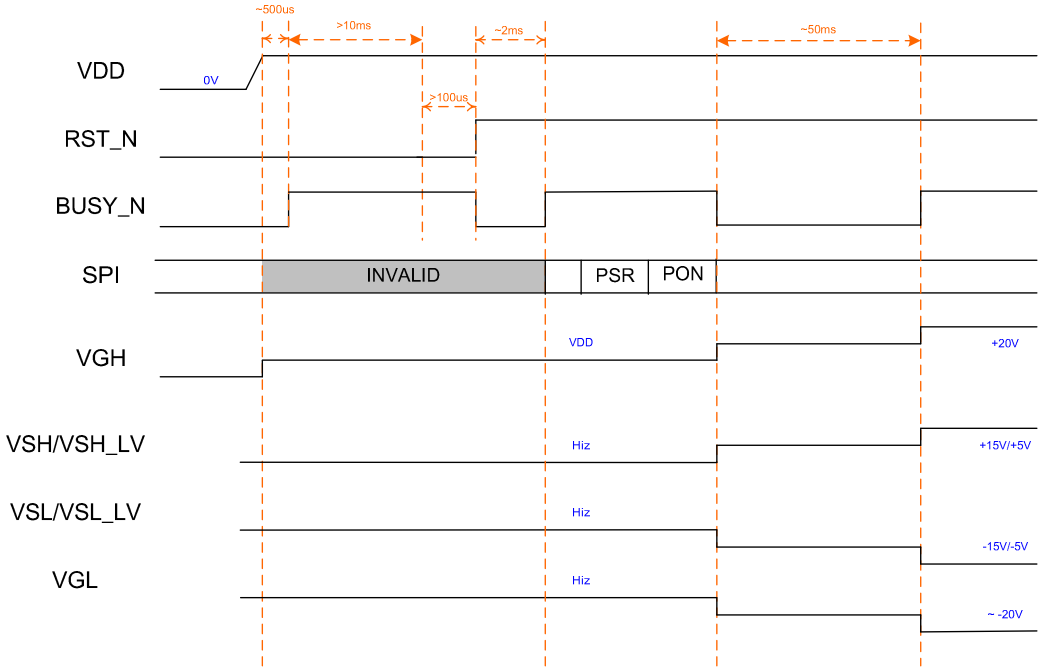
0	0	82	1	0	0	0	0	0	1	0	VDCS	This command sets VCOM_DC value. A[7:0] = 02h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[6:0] ~ VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM_DC Setting
00h	Reserved
01h	Reserved
02h	-0.10V (Default)
03h	-0.15V
04h	-0.20V
…	…
50h	-4.00V
others	-4.00V

0	0	E0	1	1	1	0	0	0	0	0	CCSET	A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7] = RAM_Mode 0 – FullRAM, DTM1 control follow RES/TRES 1 – PartialRAM, DTM1 control follow command of 0xA1, 0xD4, 0xD5, 0xDE and 0xDF A[0] = Cascade_EN 0 – Normal Mode 1 – Cascade Mode
0	0	E3	1	1	1	0	0	0	1	1	PWS	This command is sets for saving power VCOM/Source power saving during display refresh period. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. A[7:4]~ VCOM_W[3:0]: VCOM_power saving width. (unit : line period) A[3:0] ~ SD_W[3:0]: Source power saving width. (unit : 500ns)

9 Power on/off Sequence

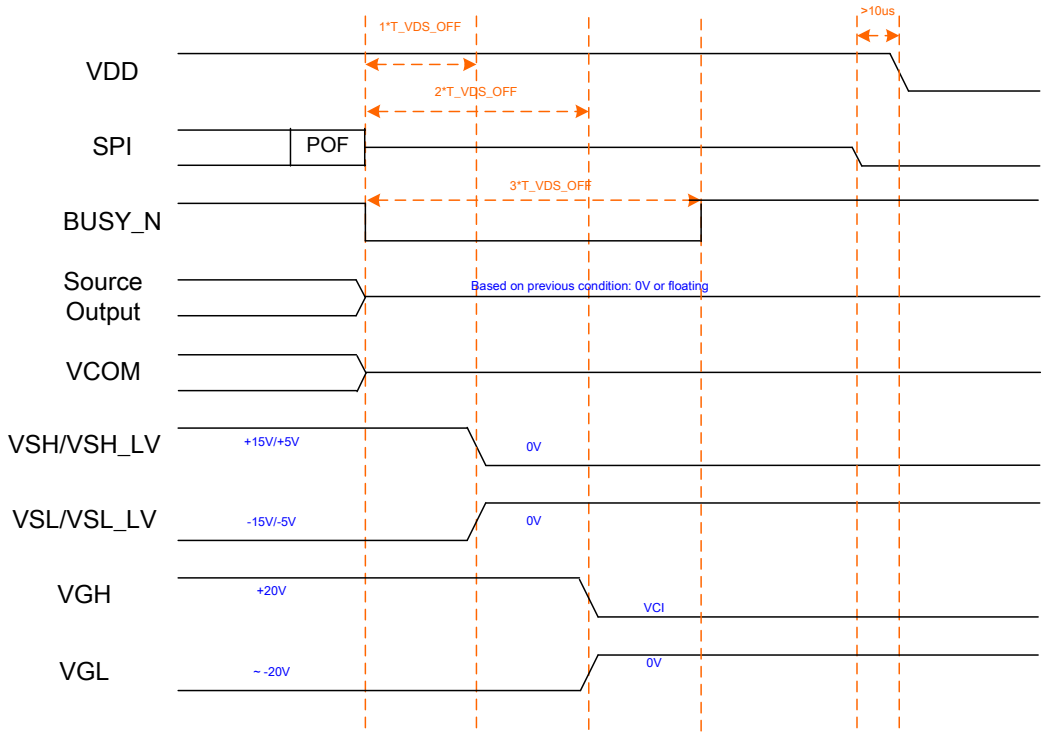
9.1 Power on Sequence Display



Power ON sequence:

1. Power ON VDD
2. After VDD become stable, wait at least 10ms , keep RST_N pin LOW (logic low) for at least 100us and then HIGH (logic high).
3. After set RST_N pin High (logic high), wait for BUSY_N pin output High (logic high). Then send command for initial setting by SPI interface.

9.2 Power off Sequence Display



Remark: VCOM, Source Power [VSH/VSH_LV/VSL/VSL_LV], Gate Power [VGH/VGL] off position can be selected by PFS (register 0x03 B byte).

10 Operation Flow and Code Sequence

10.1 General operation flow to drive display panel

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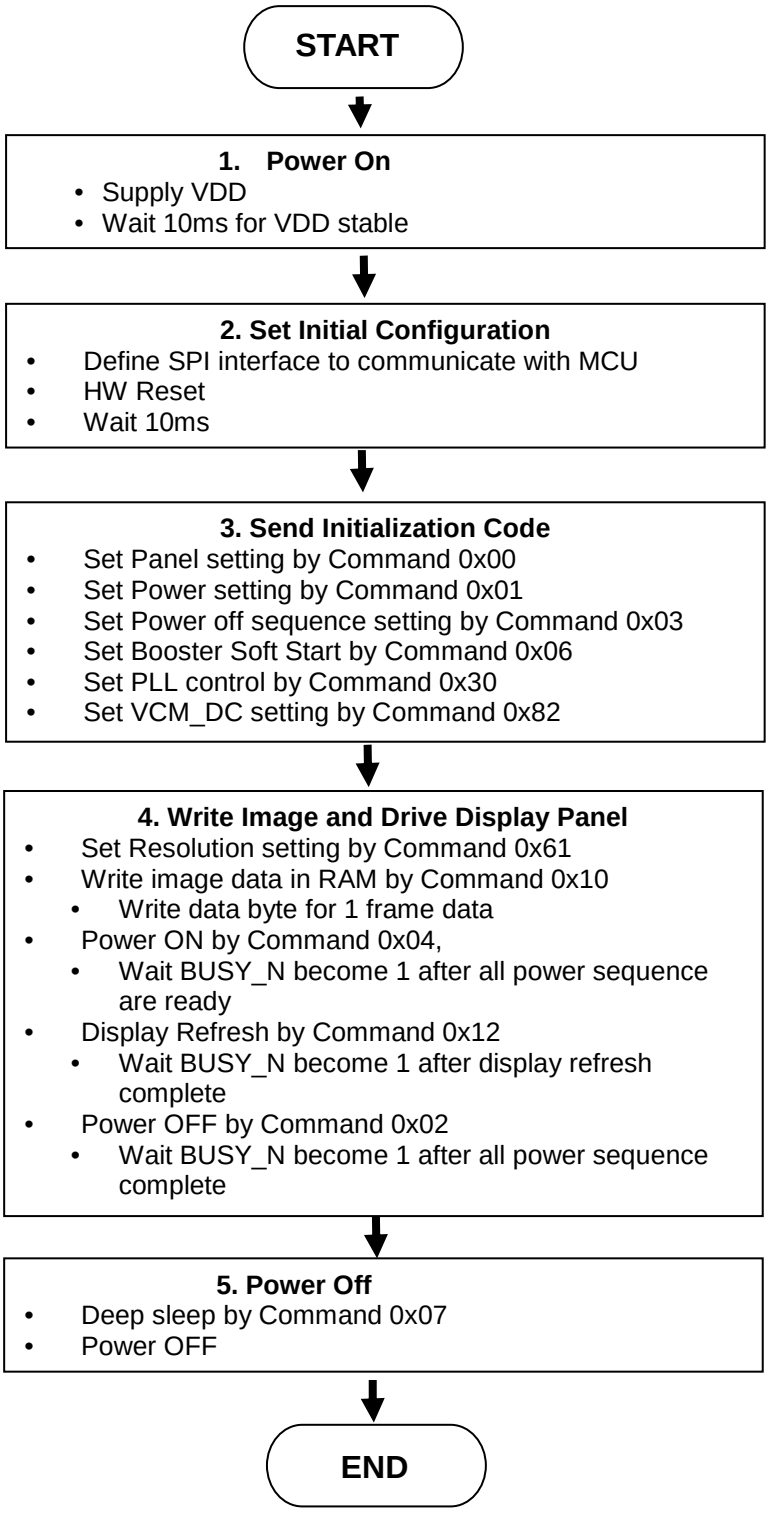


Figure 10-1: Operation flow to drive display panel

11 Absolute Maximum Rating

Table 11-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-30 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VDD be constrained to the range GND < VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either GND or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 Electrical Characteristics

The following specifications apply for: GND=0V, VDD=3.0V, VDDD=1.8V, T_{OPR}=25ºC.

Table 12-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	VDD supply operation voltage	VDD		2.3	3.0	3.6	V
V_{DDD}	VDDD logic operation voltage	VDDD		1.7	1.8	1.9	V
V_{COM_DC}	VCOM_DC output voltage	VCOM		-4.0		-0.1	V
dV_{COM_DC}	VCOM_DC output voltage deviation	VCOM		-200		200	mV
V_{COM_AC}	VCOM_AC output voltage	VCOM		V_{SL} + V_{COM_DC}	V_{COM_DC}	V_{SH}+ V_{COM_DC}	V
V_{GATE}	Gate output voltage	G0~G479		-20		+20	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage	G0~G479				40	V
V_{SH}	Positive Source output voltage	VSH			+15		V
V_{SH_LV}	Positive Source output voltage	VSH_LV		+3	+5	+15	V
dV_{SH}	VSH/VSH_LV output voltage deviation	VSH/ VSH_LV		-200		200	mV
V_{SL}	Negative Source output voltage	VSL			-15		V
V_{SL_LV}	Negative Source output voltage	VSL_LV		-15	-5	-3	V
V_{SL_LV2}	Negative Source output voltage	VSL_LV2		-15	-11	-3	V
dV_{SL}	VSL/VSL_LV/VSL_LV2 output voltage deviation	VSL/ VSL_LV/VSL_LV2		-200		200	mV
V_{IH}	High level input voltage	SDA, SCL, CSB, D/C, RST_N, BS, S/M#, CL		0.8V_{DDIO}			V
V_{IL}	Low level input voltage					0.2V_{DDIO}	V
V_{OH}	High level output voltage	SDA, BUSY, CL	IOH = -100uA	0.8V_{DDIO}			V
V_{OL}	Low level output voltage		IOL = 100uA			0.2V_{DDIO}	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Islp_VDD	Sleep mode current	VDD	- DC/DC off - No clock - No output load - MCU interface access - RAM data access		20	40	uA
Idslp_VDD	deep sleep current	VDD	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data		1	3	uA
Iopr_VDD	Operating Mode current	VDD	VDD=3.3V After PON Command VGH=20V VGL=-VGH VSH=15V VSH_LV=5V VSL_LV=-5V VSL_LV2=-11V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No FLASH read /write			2000	uA
V_{GH}	Operating Mode Output Voltage	VGH		19.0	20	21	V
V_{SH}		VSH		14.8	15	15.2	V
V_{SH_LV}		VSH_LV		4.8	5	5.2	V
V_{SL_LV}		VSL_LV		-5.2	-5	-4.8	V
V_{SL_LV2}		VSL_LV2		-11.2	-11	-10.8	V
V_{SL}		VSL		-15.2	-15	-14.8	V
V_{COM}		VCOM		-2.2	-2	-1.8	V

Table 12-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVSH	VSH current	VSH = +15V	VSH			6000	uA
IVSH_LV	VSH_LV current	VSH_LV = +5V	VSH_LV			6000	uA
IVSL_LV	VSL_LV current	VSL_LV = -5V	VSL_LV			6000	uA
IVSL_LV2	VSL_LV2 current	VSL_LV2 = -11V	VSL_LV2			6000	uA
IVSL	VSL current	VSL = -15V	VSL			6000	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			6000	uA

13 AC Characteristics

13.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - GND = 2.3V to 3.6V, T_{OPR} = 25°C, CL=20pF

Table 13-1 : Serial Peripheral Interface Timing Characteristics

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB select setup time	60			ns
t_{CSH}	CSB select hold time	65			ns
t_{SCC}	CSB deselect setup time	20			ns
t_{CHW}	CSB deselect hold time	40			ns
t_{SCYCW}	Serial clock cycle (Write)	100			ns
t_{SHW}	SCL “H” pulse width (Write)	35			ns
t_{SLW}	SCL “L” pulse width (Write)	35			ns
t_{SCYCL}	Serial clock cycle (Read)	300			ns
t_{SHR}	SCL “H” pulse width (Read)	60			ns
t_{SLR}	SCL “L” pulse width (Read)	60			ns
t_{SDS}	Data setup time	30			ns
t_{SDH}	Data hold time	30			ns
t_{ACC}	Access time			150	ns
t_{OH}	Output disable time	15			ns

Note: All timings are based on 20% to 80% of VDDIO-GND

Figure 13-1: 3 pin serial interface characteristics (write mode)

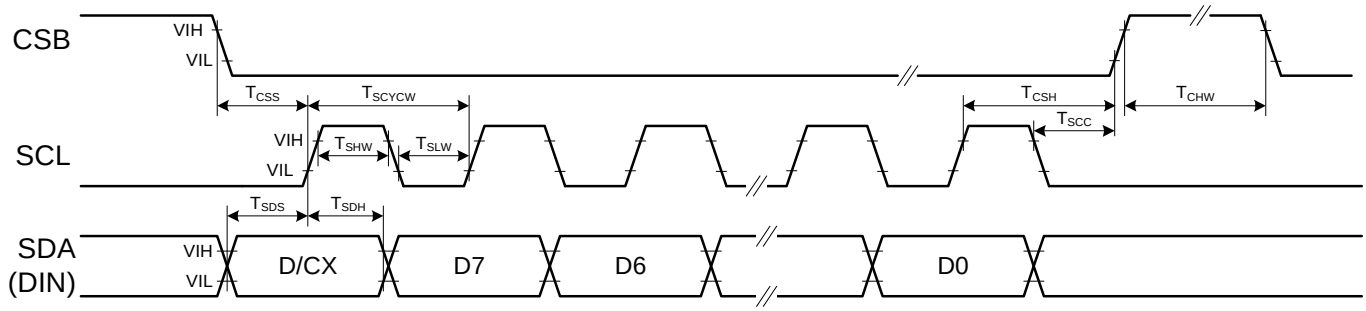


Figure 13-2: 3 pin serial interface characteristics (read mode)

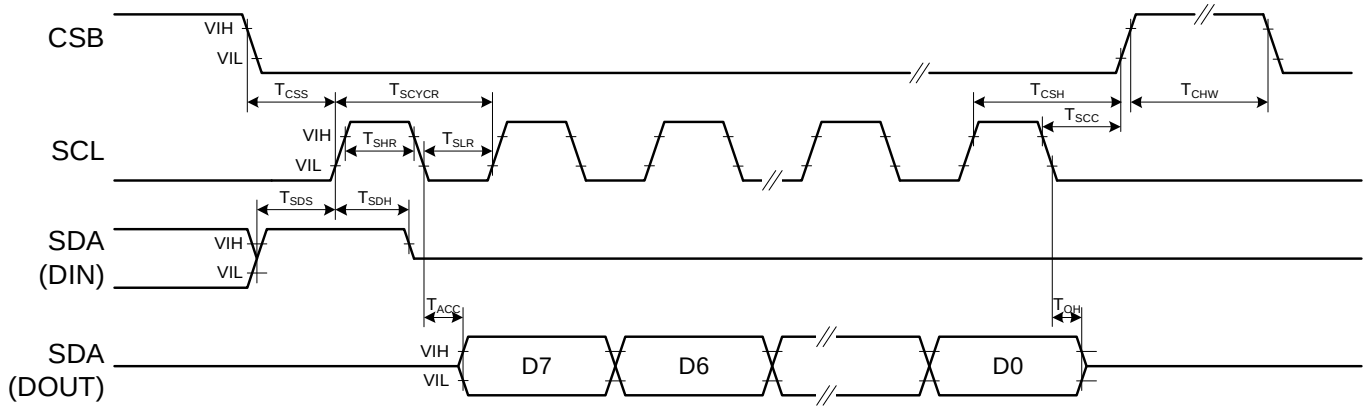
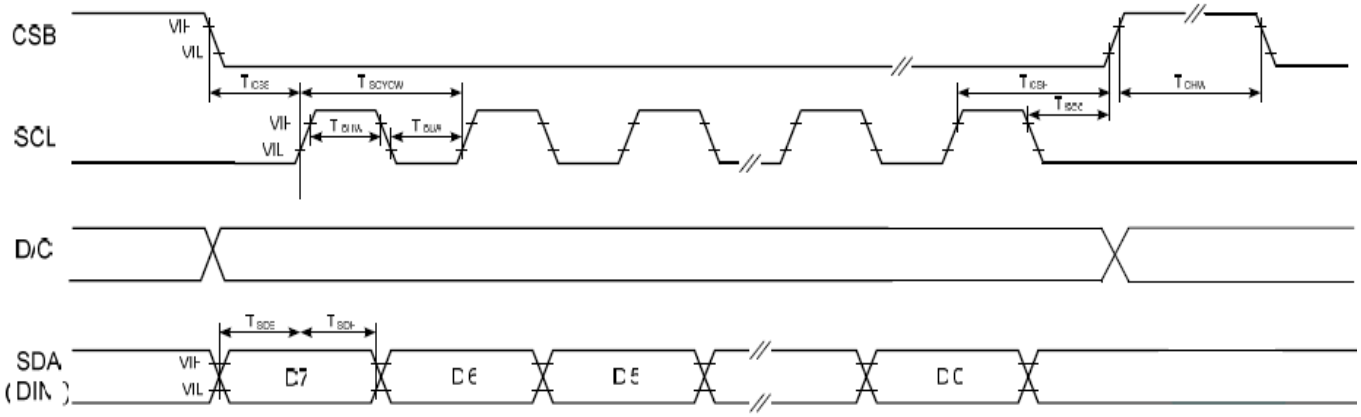


Figure 13-3: 4 pin serial interface characteristics (write mode)



14 Application Circuit

Figure 14-1: Schematic of SPD1656 application circuit for 3-color application

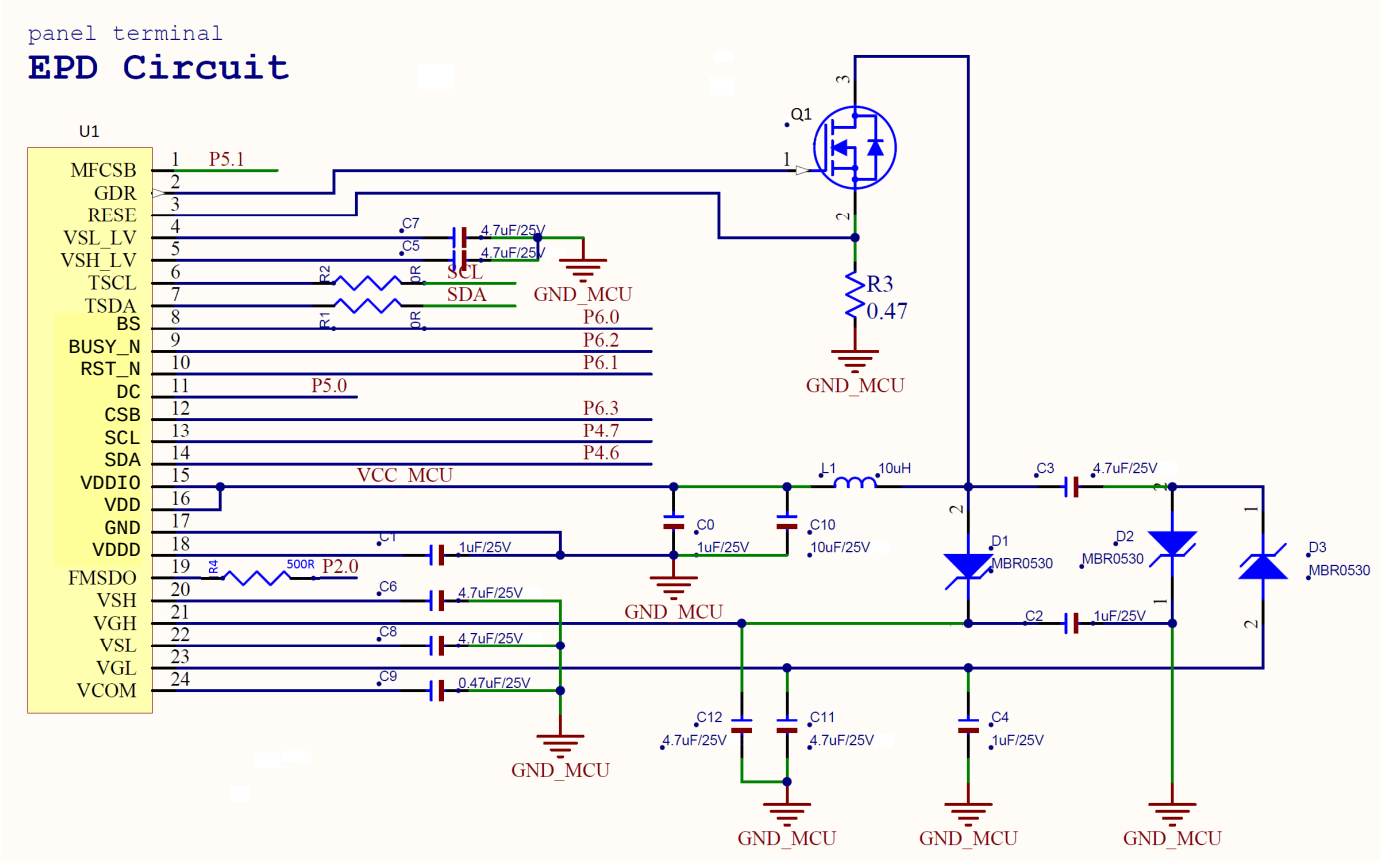


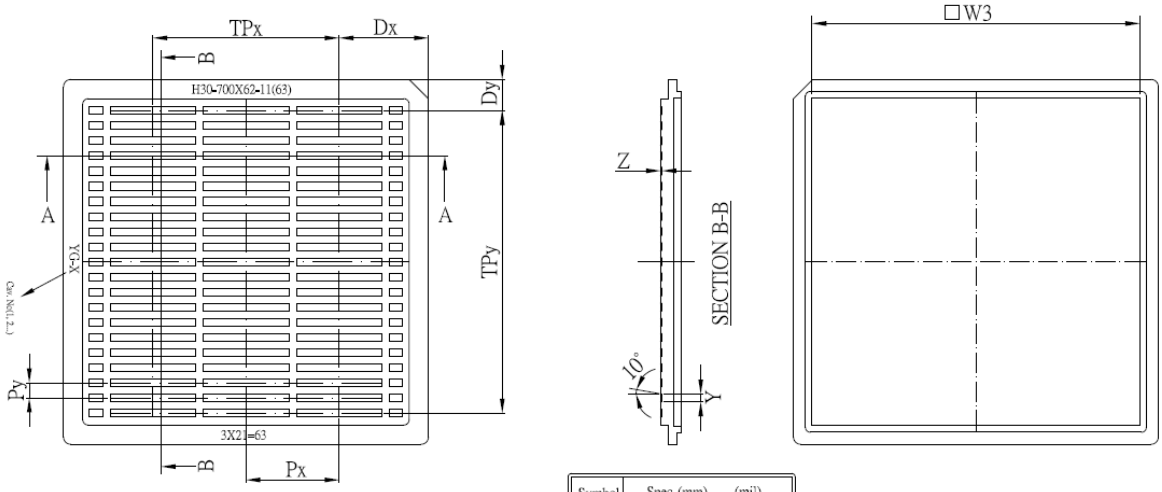
Table 14-1: Component list for SPD1656 application circuit

Part Name	Value / Type	Reference Part
C0, C1	1uF	0603/0805; X5R/X7R; Voltage Rating : 6V or 25V
C5~C8, C11~C12	4.7uF	0603/0805; X5R/X7R; Voltage Rating : 25V
C9	0.47uF	0603/0805; X5R/X7R; Voltage Rating : 25V
C10	10uF	0603/0805; X5R/X7R; Voltage Rating : 6V or 25V
C2,C4	1uF	0603/0805; X5R/X7R; Voltage Rating : 25V
C3	4.7uF	0603/0805; X5R/X7R; Voltage Rating : 25V
L1	10uH	CDRH2D18/LDNP-100NC Io= 1A (Max)
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
R1	0.47 Ohm	0805; 1% variation, ≥ 0.2W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥1A 3) Forward voltage ≤ 430mV
R2~R3	0 Ohm	0402, 0603, 0805; 10% variation, ≥ 0.05W
R4	510 Ohm	0402, 0603, 0805; 10% variation, ≥ 0.05W
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

Remarks:

1) The recommended component value and reference part in Table 14-1 is subject to change depending on panel loading.
2) Customer is required to review if the selected component value and part is suitable for their application.

15 Package Information



Symbol	Spec (mm)	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
Dx	18.60±0.10	(732)
TPx	38.80±0.10	(1528)
Dy	6.50±0.10	(256)
TPy	63.00±0.10	(2480)
Px	19.40±0.05	(764)
Py	3.15±0.05	(124)
X	17.79±0.05	(700)
Y	1.57±0.05	(62)
Z	0.28±0.05	(11)
N	63(pocket number)	

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard GB/T 26572-2011 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)”. Hazardous Substances test report is available upon request.

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