LSF0204x 4-Bits Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Application

1 Features

- Provides Bidirectional Voltage Translation With No Direction Terminal
- Supports up to 100-MHz up Translation and Greater Than 100-MHz Down Translation at ≤ 30-pF Capacitor Load and up to 40-MHz Up/Down Translation at 50-pF Capacitor Load
- Supports $I_{off}$, Partial Power Down Mode (Refer to Feature Description)
- Allows Bidirectional Voltage Level Translation Between
  - $0.8 \text{ V} \leftrightarrow 1.8, 2.5, 3.3, 5 \text{ V}$
  - $1.2 \text{ V} \leftrightarrow 1.8, 2.5, 3.3, 5 \text{ V}$
  - $1.8 \text{ V} \leftrightarrow 2.5, 3.3, 5 \text{ V}$
  - $2.5 \text{ V} \leftrightarrow 3.3, 5 \text{ V}$
  - $3.3 \text{ V} \leftrightarrow 5 \text{ V}$
- Low Standby Current
- 5 V Tolerance I/O Port to Support TTL
- Low $R_{on}$ Provides Less Signal Distortion
- High-Impedance I/O Terminals For $EN = \text{Low}$
- Flow-Through Pinout for Ease PCB Trace Routing
- Latch-Up Performance Exceeds 100 mA Per JESD17
- −40°C to 125°C Operating Temperature Range
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I²C, and Other Interfaces in Telecom Infrastructure
- Industrial
- Automotive
- Personal Computing

3 Description

The LSF family consists of bidirectional voltage level translators that operate from 0.8 V to 4.5 V ($V_{\text{ref,A}}$) and 1.8 V to 5.5 V ($V_{\text{ref,B}}$). This range allows for bidirectional voltage translations between 0.8 V and 5.0 V without the need for a direction terminal in open-drain or push-pull applications. The LSF family supports level translation applications with transmission speeds greater than 100 MHz for open-drain systems that utilize a 15-pF capacitance and 165-Ω pull-up resistor.

When the $A_n$ or $B_n$ port is LOW, the switch is in the ON-state and a low resistance connection exists between the $A_n$ and $B_n$ ports. The low $R_{on}$ of the switch allows connections to be made with minimal propagation delay and signal distortion. The voltage on the A or B side will be limited to $V_{\text{ref,A}}$ and can be pulled up to any level between $V_{\text{ref,A}}$ and 5 V. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSF0204x</td>
<td>TSSOP (14)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
<tr>
<td></td>
<td>UQFN (12)</td>
<td>2.00 mm × 1.70 mm</td>
</tr>
<tr>
<td></td>
<td>VQFN (14)</td>
<td>3.50 mm × 3.50 mm</td>
</tr>
<tr>
<td></td>
<td>DSBGA (12)</td>
<td>1.90 mm × 1.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

![Simplified Schematic Diagram]
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2018) to Revision F  Page
  • Changed location of YZP-package indicator dot to A3 position .................................................. 3
  • Added YZP package to Thermal Information table ................................................................. 5

Changes from Revision D (December 2015) to Revision E  Page
  • Changed location of YZP-package A1-pin indicator dot. View is looking through the device, as in an X-ray. ............... 3

Changes from Revision C (August 2015) to Revision D  Page
  • Added Type Column to Pin Functions table ................................................................. 4
  • Added Junction Temperatures to Thermal Information table ............................................. 5

Changes from Revision B (April 2015) to Revision C  Page
  • Removed "Less than 1.5 ns max propagation delay" from Features ............................................. 1
  • Updated "Supports High Speed Translation, Greater Than 100 MHz" bullet in Features ..................... 1

Changes from Revision A (December 2014) to Revision B  Page
  • Added YZP package to device ........................................................................................................... 1
5 Description (continued)

The supply voltage ($V_{pu#}$) for each channel may be individually set up with a pull up resistor. For example, CH1 may be used in up-translation mode (1.2 V ↔ 3.3 V) and CH2 in down-translation mode (2.5 V ↔ 1.8 V).

When EN is HIGH, the translator switch is on, and the An I/O is connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by $V_{ref_A}$. EN must be LOW to ensure the high-impedance state during power-up or power-down.

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>EN</th>
<th>An Description</th>
<th>Bn Description</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSF0204D</td>
<td>H</td>
<td>Place all data pins in 3 state mode (Hi-Z)</td>
<td>Place all data pins in 3 state mode (Hi-Z)</td>
<td>3-state output mode enable (active Low; referenced to $V_{ref_A}$)</td>
</tr>
<tr>
<td>LSF0204D</td>
<td>L</td>
<td>Input or output</td>
<td>Input or output</td>
<td></td>
</tr>
<tr>
<td>LSF0204</td>
<td>H</td>
<td>Input or output</td>
<td>Input or output</td>
<td></td>
</tr>
<tr>
<td>LSF0204</td>
<td>L</td>
<td>Place all data pins in 3 state mode (Hi-Z)</td>
<td>Place all data pins in 3 state mode (Hi-Z)</td>
<td>3-state output mode enable (active High, referenced to $V_{ref_A}$)</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

![Diagram of pin configuration and functions]
## Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>NO.</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V&lt;sub&gt;ref&lt;/sub&gt;_A</td>
<td>1</td>
<td>1</td>
<td>PW, RGY</td>
</tr>
<tr>
<td>A1</td>
<td></td>
<td>2</td>
<td>2</td>
<td>RUT</td>
</tr>
<tr>
<td>A2</td>
<td></td>
<td>3</td>
<td>3</td>
<td>RUT</td>
</tr>
<tr>
<td>A3</td>
<td></td>
<td>4</td>
<td>4</td>
<td>RUT</td>
</tr>
<tr>
<td>A4</td>
<td></td>
<td>5</td>
<td>5</td>
<td>RUT</td>
</tr>
<tr>
<td>NC</td>
<td></td>
<td>6</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>7</td>
<td>6</td>
<td>RUT</td>
</tr>
<tr>
<td>EN</td>
<td></td>
<td>8</td>
<td>12</td>
<td>RUT</td>
</tr>
<tr>
<td>NC</td>
<td></td>
<td>9</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>B4</td>
<td></td>
<td>10</td>
<td>7</td>
<td>RUT</td>
</tr>
<tr>
<td>B3</td>
<td></td>
<td>11</td>
<td>8</td>
<td>RUT</td>
</tr>
<tr>
<td>B1</td>
<td></td>
<td>13</td>
<td>10</td>
<td>RUT</td>
</tr>
<tr>
<td>V&lt;sub&gt;ref&lt;/sub&gt;_B</td>
<td></td>
<td>14</td>
<td>11</td>
<td>RUT</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_i) Input voltage (^{(2)})</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IO}) Input/output voltage (^{(2)})</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IK}) Input clamp current</td>
<td>128</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(T_J) Junction temperature</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>(T_{stg}) Storage temperature</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>ESD model</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (^{(2)})</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IO}) Input/output voltage</td>
<td>0</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{REF_A/B/EN}) Reference voltage</td>
<td>0</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>(I_{PASS}) Pass transistor current</td>
<td>64</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(T_A) Operating free-air temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (^{(1)})</th>
<th>LSF0204</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RGY (VQFN)</td>
</tr>
<tr>
<td>(R_{UA}) Junction-to-ambient thermal resistance</td>
<td>83.2</td>
</tr>
<tr>
<td>(R_{U_C(top)}) Junction-to-case (top) thermal resistance</td>
<td>98.2</td>
</tr>
<tr>
<td>(R_{UB}) Junction-to-board thermal resistance</td>
<td>59.2</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>17.4</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>59.4</td>
</tr>
<tr>
<td>(R_{U_C(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>38.7</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(1)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IK} )</td>
<td>( I_I = -18 , mA, V_{EN} = 0 )</td>
<td>-1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>( V_I = 5 , V, V_{EN} = 0 )</td>
<td>5.0</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{CCB} )</td>
<td>Leakage from ( V_{ref_B} ) to ( V_{ref_A} )</td>
<td>3.3 V, ( V_{ref_A} = 1.8 , V, V_{EN} = V_{ref_A}, I_O = 0, V_I = 3.3 , V ) or GND</td>
<td>3.5</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{CCB} )</td>
<td>Total Current through GND</td>
<td>3.3 V, ( V_{ref_A} = 1.8 , V, V_{EN} = V_{ref_A}, I_O = 0, V_I = 3.3 , V ) or GND</td>
<td>0.2</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{IN} )</td>
<td>Control pin current</td>
<td>5.5 V, ( V_{ref_A} = 4.5 , V, V_{EN} = 0 ) to ( V_{Vref_A}, I_O = 0 )</td>
<td>( \pm 1 , \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IO} )</td>
<td>Power Off Leakage Current</td>
<td>( V_{ref_B} = 3.3 , V, V_{ref_A} = 1.8 , V, V_{EN} = GND, I_O = 0, V_I = 5 , V ) or GND</td>
<td>( \pm 1 , \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{V(ref_A/B/EN)} )</td>
<td>( V_I = 3 , V ) or 0</td>
<td>7</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{IO(on)} )</td>
<td>( V_O = 3 , V ) or 0, ( V_{EN} = V_{ref_A} )</td>
<td>5.0</td>
<td>6.0</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( C_{IO(off)} )</td>
<td>( V_O = 3 , V ) or 0, ( V_{EN} = V_{ref_A} )</td>
<td>10.5</td>
<td>13</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( V_{IH} ) (EN pin)</td>
<td>High-level input voltage</td>
<td>( V_{ref_A} = 1.5 , V ) to 4.5 V</td>
<td>0.7×Vref_A</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{IL} ) (EN pin)</td>
<td>Low-level input voltage</td>
<td>( V_{ref_A} = 1.5 , V ) to 4.5 V</td>
<td>0.3×Vref_A</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{IH} ) (EN pin)</td>
<td>High-level input voltage</td>
<td>( V_{ref_A} = 1.0 , V ) to 1.5 V</td>
<td>0.8×Vref_A</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{IL} ) (EN pin)</td>
<td>Low-level input voltage</td>
<td>( V_{ref_A} = 1.0 , V ) to 1.5 V</td>
<td>0.3×Vref_A</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( \Delta t/\Delta V ) (EN pin)</td>
<td>Input transition rise or fall rate for EN pin</td>
<td>10</td>
<td>ns/V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) All typical values are at \( T_A = 25^\circ C \).
(2) The actual supply current for LSF0204 is \( I_{CCB} + I_{CCB} \): the leakage from \( V_{ref_B} \) to \( V_{ref_A} \) can be measured on \( V_{ref_A} \) and \( V_{ref_B} \) pin.
(3) Enable pin test conditions are for the LSF0204. The enable pin test conditions for LSF0204D are oppositely set.
(4) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

7.6 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.8 V)

over recommended operating free-air temperature range, \( V_{ref_A} = 1.8 \, V, V_{ref_B} = 3.3 \, V, V_{EN} = 1.8 \, V, V_{pu_1} = 3.3 \, V, V_{pu_2} = 1.8 \, V, R_L = NA, V_{IH} = 3.3 \, V, V_{IL} = 0 \, V, R_M = 1.15 \, V \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>( C_L = 50 , pF )</th>
<th>( C_L = 30 , pF )</th>
<th>( C_L = 15 , pF )</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{PLH} )</td>
<td>A or B</td>
<td>B or A</td>
<td>TYP</td>
<td>MAX</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>( I_{PLH} )</td>
<td>0.7</td>
<td>5.49</td>
<td>0.5</td>
<td>5.29</td>
<td>0.3</td>
<td>5.19</td>
</tr>
<tr>
<td>( I_{PLH} )</td>
<td>0.9</td>
<td>4.9</td>
<td>0.7</td>
<td>4.7</td>
<td>0.5</td>
<td>4.5</td>
</tr>
<tr>
<td>( I_{PLZ} )</td>
<td>13</td>
<td>18</td>
<td>12</td>
<td>16.5</td>
<td>11</td>
<td>15</td>
</tr>
<tr>
<td>( I_{PZL} )</td>
<td>33</td>
<td>45</td>
<td>30</td>
<td>40</td>
<td>23</td>
<td>37</td>
</tr>
<tr>
<td>( I_{MAX} )</td>
<td>50</td>
<td>100</td>
<td>100</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
7.7 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.2 V)
over recommended operating free-air temperature range $V_{rev-A} = 1.2$ V, $V_{rev-B} = 3.3$ V, $V_{EN} = 1.2$ V, $V_{pu_1} = 3.3$ V, $V_{pu_2} = 1.2$ V, $R_L = NA$, $V_{ih} = 3.3$V, $V_{il} = 0$ V $V_M = 0.85$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$C_L = 50$ pF</th>
<th>$C_L = 30$ pF</th>
<th>$C_L = 15$ pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A or B</td>
<td>B or A</td>
<td>0.8</td>
<td>4.1</td>
<td>0.5</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td></td>
<td></td>
<td>0.9</td>
<td>4.7</td>
<td>0.7</td>
</tr>
<tr>
<td>$t_{MAX}$</td>
<td></td>
<td></td>
<td>50</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

7.8 Switching Characteristics: AC Performance (Translating Up, 1.8 V to 3.3 V)
over recommended operating free-air temperature range $V_{rev-A} = 1.8$ V, $V_{rev-B} = 3.3$ V, $V_{EN} = 1.8$ V, $V_{pu_1} = 3.3$ V, $V_{pu_2} = 1.8$V, $R_L = 500$ Ω, $V_{ih} = 1.8$V, $V_{il} = 0$ V $V_M = 0.9$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$C_L = 50$ pF</th>
<th>$C_L = 30$ pF</th>
<th>$C_L = 15$ pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A or B</td>
<td>B or A</td>
<td>0.6</td>
<td>5.7</td>
<td>0.4</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td></td>
<td></td>
<td>1.3</td>
<td>6.7</td>
<td>1</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td></td>
<td></td>
<td>13</td>
<td>18</td>
<td>12</td>
</tr>
<tr>
<td>$t_{PZL}$</td>
<td></td>
<td></td>
<td>33</td>
<td>45</td>
<td>30</td>
</tr>
<tr>
<td>$t_{MAX}$</td>
<td></td>
<td></td>
<td>50</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

7.9 Switching Characteristics: AC Performance (Translating Up, 1.2 V to 1.8 V)
over recommended operating free-air temperature range, $V_{rev-A} = 1.2$ V, $V_{rev-B} = 1.8$ V, $V_{EN} = 1.2$ V, $V_{pu_1} = 1.8$ V, $V_{pu_2} = 1.2$ V, $R_L = 500$ Ω, $V_{ih} = 1.2$V, $V_{il} = 0$ V $V_M = 0.6$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$C_L = 50$ pF</th>
<th>$C_L = 30$ pF</th>
<th>$C_L = 15$ pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A or B</td>
<td>B or A</td>
<td>0.65</td>
<td>7.25</td>
<td>0.4</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td></td>
<td></td>
<td>1.6</td>
<td>7.03</td>
<td>1.3</td>
</tr>
<tr>
<td>$t_{MAX}$</td>
<td></td>
<td></td>
<td>50</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

7.10 Typical Characteristics

![Figure 1. Signal Integrity (1.8 V to 3.3 V Translation Up at 50 MHz)](image-url)
8 Parameter Measurement Information

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit for Outputs

Figure 3. Load Circuit for Enable/Disable Time Measurement
8.1 Load Circuit AC Waveform for Outputs

Figure 4. $t_{PLH}$, $t_{PHL}$

Figure 5. $t_{PLZ}$, $t_{PZL}$
9 Detailed Description

9.1 Overview
The LSF Family may be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The LSF Family is ideal for use in applications where an open-drain driver is connected to the data I/Os. LSF can achieve 100 MHz with the appropriate pull-up resistors and layout. The LSF Family may also be used in applications where a push-pull driver is connected to the data I/Os.

9.2 Functional Block Diagram
9.3 Feature Description

9.3.1 Support High Speed Translation, Greater than 100 MHz
Allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO).

9.3.2 Bidirectional Voltage Translation Without DIR Terminal
Minimizes system effort to develop voltage translation for bidirectional interface (PMBus, I2C, or SMbus).

9.3.3 5-V Tolerance on IO Port and 125°C Support
The LSF family, with 5-V tolerance and 125°C support, is flexible and compliant with TTL levels in industrial and telecom applications.

9.3.4 Channel Specific Translation
The LSF family is able to set up different voltage translation levels on each channel.

9.3.5 Ioff, Partial Power Down Mode
When Vref_A, Vref_B = 0, all of data pins and EN pin are Hi-Z.
EN logic circuit is supplied by Vref_A, once Vref_A power up first and all of data pins are unknown state until Vref_B and EN ready. No power sequence is required to enable LSF0204 and operate function normally.

9.4 Device Functional Modes
Table 1 lists the device functional modes of the LSF0204x family of devices.

<table>
<thead>
<tr>
<th>INPUT</th>
<th>EN(1) TERMINAL</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>An = Bn</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>Hi-Z</td>
<td></td>
</tr>
</tbody>
</table>

(1) EN is controlled by Vref_A logic levels.
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
LSF performs voltage translation for open-drain or push-pull interface. Table 2 provides some consumer/telecom interfaces as reference in regards to the different channel numbers that are supported by the LSF family.

Table 2. Voltage Translator for Consumer/Telecom Interface

<table>
<thead>
<tr>
<th>PART NAME</th>
<th>CH#</th>
<th>INTERFACE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSF0101</td>
<td>1</td>
<td>GPIO</td>
</tr>
<tr>
<td>LSF0102</td>
<td>2</td>
<td>GPIO, MDIO, SMBus, PMBus, I2C</td>
</tr>
<tr>
<td>LSF0204</td>
<td>4</td>
<td>GPIO, SPI, MDIO, SMBus, PMBus, I2C, UART, SVID</td>
</tr>
<tr>
<td>LSF0108</td>
<td>8</td>
<td>GPIO, MDIO, SDIO, SVID, UART, SMBus, PMBus, I2C, SPI</td>
</tr>
</tbody>
</table>

10.2 Typical Applications

10.2.1 I2C PMBus, SMBus, GPIO, Application

10.2.1.1 Design Requirements

10.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines
The LSF family has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF family is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF family for bidirectional application (I2C, SMBus, PMBus, or MDIO).
Typical Applications (continued)

Table 3. Application Operating Condition

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vref_A</td>
<td>Reference voltage (A)</td>
<td>0.8</td>
<td>4.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Vref_B</td>
<td>Reference voltage (B)</td>
<td>Vref_A + 0.8</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V(EN)(1)</td>
<td>Input voltage on EN terminal</td>
<td>0</td>
<td>Vref_A</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Vpu</td>
<td>Pull-up supply voltage</td>
<td>0</td>
<td>Vref_B</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

(1) Refer \( V_{IH} \) and \( V_{IL} \) for \( V_{I(EN)} \)

Also Vref_B is recommended to be at 1.0 V higher than Vref_A for best signal integrity.

The LSF Family is able to set different voltage translation level on each channel.

**NOTE**

Vref_A must be set as lowest voltage level.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Bidirectional Translation

The master output driver may be push-pull or open-drain (pull-up resistors may be required) and the slave device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

**NOTE**

However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

In Figure 6, the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through to a 3.3 V Vpu power supply, and Vref_A is set 1.0V. The output of A3 and B4 has a maximum output voltage equal to Vref_A, and the bidirectional interface (Ch1/2, MDIO) has a maximum output voltage equal to Vpu.

10.2.1.2.1.1 Pull-up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, to calculate the pull-up resistor value use Equation 1.

\[
R_{pu} = \frac{(V_{pu} - 0.35 \text{ V})}{0.015 \text{ A}}
\]  

(1)

Table 4 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175 V, although the 15 mA applies only to current flowing through the LSF family device.
### Table 4. Pullup Resistor Values (1)(2)

<table>
<thead>
<tr>
<th>$V_{DPU}$</th>
<th>15 mA NOMINAL</th>
<th>10 mA NOMINAL</th>
<th>3 mA NOMINAL</th>
<th>+10% (3) NOMINAL</th>
<th>+10% (3) NOMINAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V</td>
<td>310</td>
<td>341</td>
<td>465</td>
<td>512</td>
<td>1550</td>
</tr>
<tr>
<td>3.3 V</td>
<td>197</td>
<td>217</td>
<td>295</td>
<td>325</td>
<td>983</td>
</tr>
<tr>
<td>2.5 V</td>
<td>143</td>
<td>158</td>
<td>215</td>
<td>237</td>
<td>717</td>
</tr>
<tr>
<td>1.8 V</td>
<td>97</td>
<td>106</td>
<td>145</td>
<td>160</td>
<td>483</td>
</tr>
<tr>
<td>1.5 V</td>
<td>77</td>
<td>85</td>
<td>115</td>
<td>127</td>
<td>383</td>
</tr>
<tr>
<td>1.2 V</td>
<td>57</td>
<td>63</td>
<td>85</td>
<td>94</td>
<td>283</td>
</tr>
</tbody>
</table>

(1) Calculated for $V_{OL} = 0.35$ V  
(2) Assumes output driver $V_{OL} = 0.175$ V at stated current  
(3) +10% to compensate for $V_{DD}$ range and resistor tolerance

#### 10.2.1.2.2 LS Family Bandwidth

The maximum frequency of the LSF family is dependent on the application. The device may operate at speeds of >100MHz gave the correct conditions. The maximum frequency is dependent upon the loading of the application. The LSF family behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

Figure 7 shows a bandwidth measurement of the LSF family using a two-port network analyzer.

![Figure 7. 3-dB Bandwidth](image)

The 3-dB point of the LSF family is ≈600MHz; however, this measurement is an analog type of measurement. For digital applications, the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is important in determining the overall shape of the digital signal. In the case of the LSF family, a digital clock frequency of greater than 100 MHz may be achieved.

The LSF family does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the LSF family is being driven by standard CMOS totem pole output driver. Best practice is to minimize the trace length from the LSF family on the sink side (1.8 V) to minimize signal degradation.

All fast edges have an infinite spectrum of frequency components; however, there is an inflection (or knee) in the frequency spectrum of fast edges where frequency components higher than $f_{knee}$ are insignificant in determining the shape of the signal.
To calculate the maximum practical frequency component, or the knee frequency ($f_{\text{knee}}$), use the following equations:

$$f_{\text{knee}} = 0.5/RT \ (10\%-80\%)$$  \hspace{1cm} (2)

$$f_{\text{knee}} = 0.4/RT \ (20\%-80\%)$$  \hspace{1cm} (3)

For signals with rise time characteristics based on 10- to 90-percent thresholds, $f_{\text{knee}}$ is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20% to 80% thresholds, which is very common in many of today's device specifications, $f_{\text{knee}}$ is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the LSF family close to the $I^2C$ output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

### 10.2.1.3 Application Curve

![Capture Waveform From Above I²C Set-Up (1.8 V to 3.3 V at 2.5 MHz)](image)

**Figure 8. Captured Waveform From Above I²C Set-Up (1.8 V to 3.3 V at 2.5 MHz)**
10.2.2 MDIO Application

10.2.2.1 Design Requirements
Refer to Design Requirements.

10.2.2.2 Detailed Design Procedure
Refer to Detailed Design Procedure

10.2.2.3 Application Curve

Figure 9. Typical Application Circuit (MDIO/Bidirectional Interface)

Figure 10. Captured Waveform From Above MDIO Setup
10.2.3 Multiple Voltage Translation in Single Device, Application

10.2.3.1 Design Requirements
Refer to Design Requirements.

10.2.3.2 Detailed Design Procedure
Refer to Detailed Design Procedure

10.2.3.3 Application Curve

Figure 11. Translation Down (3.3 V to 1.8 V) at 150 MHz
11 Power Supply Recommendations

There are no power sequence requirements for the LSF Family. Refer to the Enable, Disable, and Reference Voltage Guidelines for enabling and reference voltage guidelines.

12 Layout

12.1 Layout Guidelines

The signal integrity is highly related with pull-up resistor and PCB capacitance condition because LSF Family is switch-type level translator

- Short signal trace as possible to reduce capacitance and minimize stub from pull-up resistor.
- Place LSF close to high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

12.2 Layout Example

![Figure 12. Short Trace Layout](image)

![Figure 13. Device Placement](image)

GND
Vref_A
A1
A2
EN
Vref_B
B1
B2
LSF0102
SD Controller (1.8V IO)
SDIO Connector (3.3V IO)
Device PCB

Submit Documentation Feedback

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Product Folder Links: LSF0204 LSF0204D
Figure 14. Waveform From TP1 (Pullup Resistor: 160-Ω and 50-pF Capacitance 3.3 to 1.8 V at 100 MHz)

Figure 15. Waveform From TP2 (Pullup Resistor: 160-Ω and 50-pF Capacitance 1.8 to 3.3 V at 100 MHz)
13 Device and Documentation Support

13.1 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSF0204</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>LSF0204D</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

13.2 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support*  Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary
**SLYZ022** — *TI Glossary.*
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
14.1 Package Option Addendum

14.1.1 Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status  (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (3)</th>
<th>MSL Peak Temp (4)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (5)(6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSF0204DPWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>–40 to 125</td>
<td>LSF04D</td>
</tr>
<tr>
<td>LSF0204DRGYR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-UNLIM</td>
<td>–40 to 125</td>
<td>LSF24D</td>
</tr>
<tr>
<td>LSF0204DRUTR</td>
<td>ACTIVE</td>
<td>UQFN</td>
<td>RUT</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>–40 to 125</td>
<td>SIO</td>
</tr>
<tr>
<td>LSF0204DYZPR</td>
<td>ACTIVE</td>
<td>DSBGA</td>
<td>YZP</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>–40 to 125</td>
<td>G6</td>
</tr>
<tr>
<td>LSF0204PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>–40 to 125</td>
<td>LSF04D</td>
</tr>
<tr>
<td>LSF0204RGYR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-UNLIM</td>
<td>–40 to 125</td>
<td>LSF24</td>
</tr>
<tr>
<td>LSF0204RUTR</td>
<td>ACTIVE</td>
<td>UQFN</td>
<td>RUT</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>–40 to 125</td>
<td>G5</td>
</tr>
<tr>
<td>LSF0204YZPR</td>
<td>ACTIVE</td>
<td>DSBGA</td>
<td>YZP</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>–40 to 125</td>
<td>G6</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
   **ACTIVE:** Product device recommended for new designs.
   **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   **PRE_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
   **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
   **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.
   **RoHS Exempt:** TI defines “RoHS Exempt” to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
   **Green:** TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement

(3) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) **MSL, Peak Temp.** -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “-“ will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LSF0204:
– Automotive: LSF0204-Q1

NOTE: Qualified Version Definitions:
Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
PACKAGE OUTLINE

DSBGA - 0.5 mm max height

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

![Diagram of TAPE DIMENSIONS](image)

**A0** Dimension designed to accommodate the component width  
**B0** Dimension designed to accommodate the component length  
**K0** Dimension designed to accommodate the component thickness  
**W** Overall width of the carrier tape  
**P1** Pitch between successive cavity centers

### REEL DIMENSIONS

![Diagram of REEL DIMENSIONS](image)

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Q1**: Upper-left quadrant  
- **Q2**: Lower-left quadrant  
- **Q3**: Upper-right quadrant  
- **Q4**: Lower-right quadrant

*User Direction of Feed*

*Sprocket Holes*

*Pocket Quadrants*

### PACKAGES AND MATERIALS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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*All dimensions are nominal.*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. OFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
   The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal via, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SOIC PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout.
E. Laser cutting aperture with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
RUT (R-PUQFN-N12)  PLASTIC QUAD FLATPACK NO-LEAD

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0.1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for larger area ratio is not advised due to land width and bridging potential. Exercise extreme caution.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.
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