10.2inch e-Paper (G)

User Manual

Revision History

Version	Content	Date	Page
1.0	New creation	2025/03/13	All

Contents

1. OVERVIEW

The display is a 10.2inch TFT active matrix electrophoretic display, featuring a welldesigned interface and reference system. It boasts a resolution of 960×640 pixels, offering 1-bit grayscale with full display capabilities in black, white, red and yellow. Each panel is equipped with an integrated circuit that includes a gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC converter, SRAM, look-up table (LUT), VCOM support, and border features.

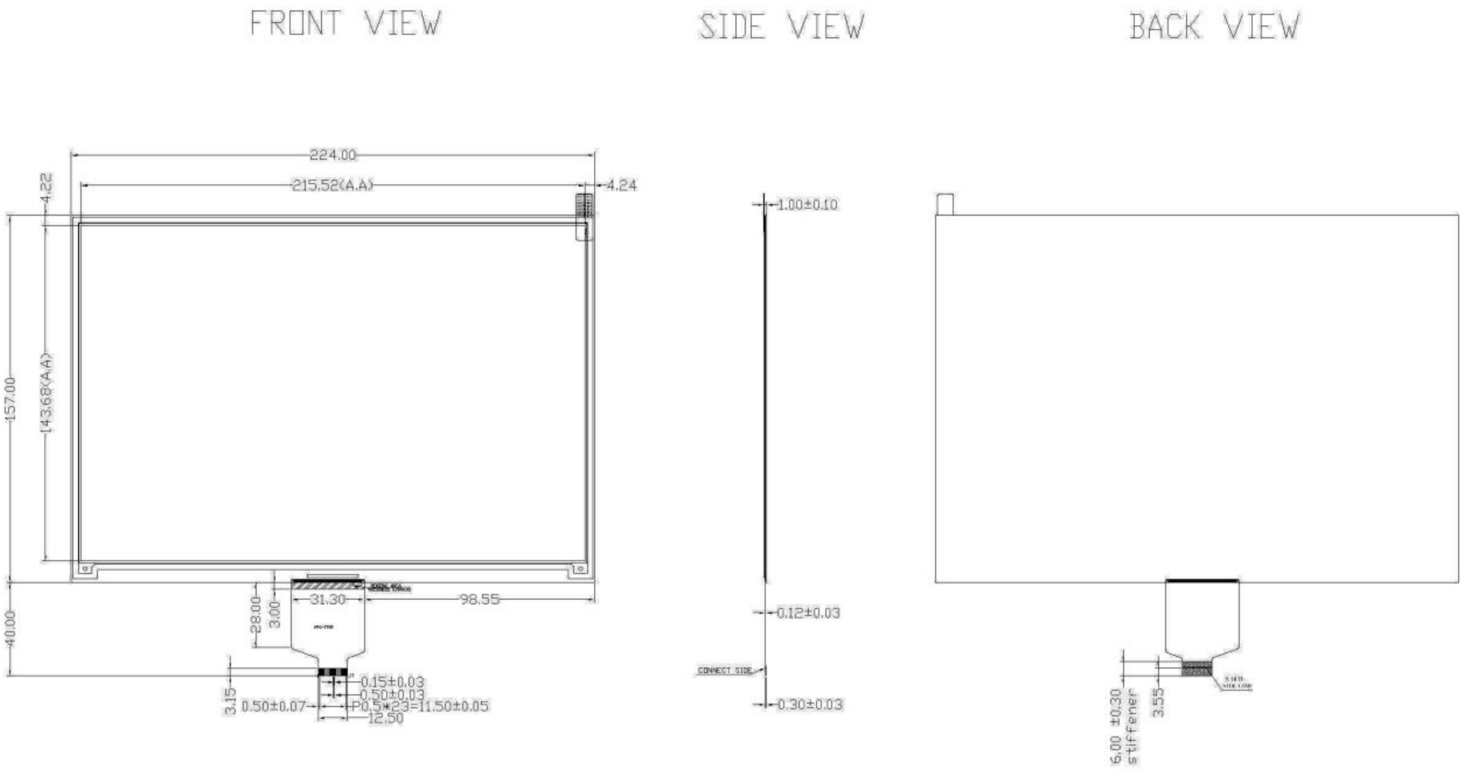
2. FEATURES

- 960 × 640 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape and portrait modes
- Hard-coat antiglare display surface
- Ultra low current deep sleep mode
- On-chip display RAM
- Waveform can be stored in on-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor
- Built-in temperature sensor

3. MECHANICAL AND OPTICAL SPECIFICATIONS

Parameter	Specifications	Unit	Remark
Screen Size	10.2	Inch	
Display Resolution	960(H)×640(V)	Pixel	DPI:113
Active Area	215.52(H)×143.68(V)	mm	
Pixel Pitch	0.2245×0.2245	mm	
Pixel Configuration	Rectangle		
Outline Dimension	224(H)×157(V)×1.0±0.1(D)	mm	
Weight	62.2±0.5	g	

4. MECHANICAL DRAWING OF EPD MODULE



Notes:

4-1: Display module 10.2″ array for EPD;

4-2: Driver IC: SSD2677;

4-3: Resolution: 960source×640gate;

4-4: Pixel size: 0.2245mm×0.2245mm;

4-5: For JX.

5. PIN ASSIGNMENT

NO.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep open
5	VSH2	C	Positive Source driving voltage (Red)	
6	NC		Do not connect with other NC pins	
7	NC		Do not connect with other NC pins	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low	Note 5-3
11	D/C#	I	Data / Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins. It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O = Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Notes:

5-1: This pin(CS#) is the chip select input pin connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

5-2: This pin(D/C#) is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

5-3: This pin(RES#) is reset signal input. The Reset is active low.

5-4: This pin is Busy state output pin. When Busy is Low, the operation of the chip should not be interrupted, the command should not be sent. The chip would put Busy pin Low when

- Outputting display waveform
- Communicating with digital temperature sensor

5-5: Bus interface selection pin.

BS1 State	MCU Interface
L	4-line serial peripheral interface(SPI) - 8 bits SPI
H	3-line serial peripheral interface(SPI) - 9 bits SPI

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CI}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to VCI +0.5	V
Logic Output voltage	V_{OUT}	-0.5 to VCI +0.5	V
Operating Temp range	T_{OPR}	0 to +40	℃
Storage Temp range	T_{STG}	-25 to +70	℃
Optimal Storage Temp	T_{STGO}	23±2	℃
Optimal Storage Humidity	H_{STGO}	55±10	%RH

Note:

6-1-1: Maximum ratings are those values beyond which damages to the device may occur. Functional operations should be restricted to the limits in the Panel DC Characteristics table.

6-1-2: The storage time is within 10 days for -25℃～70℃.

The display screen should be kept white and face up.

6.2 PANEL DC CHARACTERISTICS

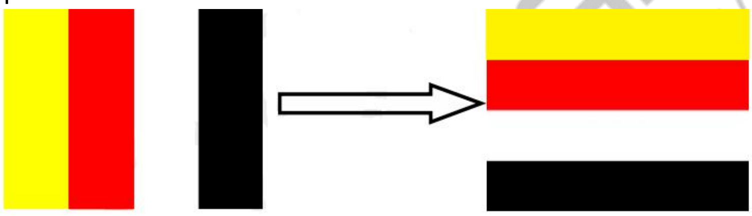
The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, T_{OPR} =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-	-	-	0	-	V
Logic supply voltage	V_{CI}	-	V_{CI}	2.3	3.0	3.6	V
Core logic voltage	V_{DD}	-	V_{DD}	2.3	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2V_{CI}	V
High level output voltage	V_{OH}	I_{OH} = -100Ma	-	0.8V_{CI}	-	-	V
Low level output voltage	V_{OL}	I_{OL} = 100Ma	-	-	-	0.2V_{CI}	V
Typical power	P_{TYP}	V_{CI}=3.0V	-	-	66	-	mW
Deep sleep mode	P_{STPY}	V_{CI}=3.0V	-	-	0.0012	-	mW
Typical operating current	I_{opr}_V_{CI}	V_{CI}=3.0V	-		22	-	mA
Image update time	-	23℃	-	-	20	-	sec

Deep sleep mode current	I_{dslp}_V_{CI}	DC/DC OFF No clock No input load Ram data not retain	-	-	0.4	-	μA

Notes:

6-2-1: The typical power is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern.



6-2-2: The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

6-2-3: The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.

6-2-4: Electrical measurement: Tektronix oscilloscope - MDO3024,
Tektronix current probe - TCP0030A.

6.3 PANEL AC CHARACTERISTICS

6.3.1 MCU Interface Selection

The pin assignment at different interface modes is summarized in Table 6-3-1. Different MCU modes can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 6-3-1: MCU interface assignment under different bus interface modes

6.3.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table 6-3-2: Control pins of 4-wire Serial Peripheral Interface

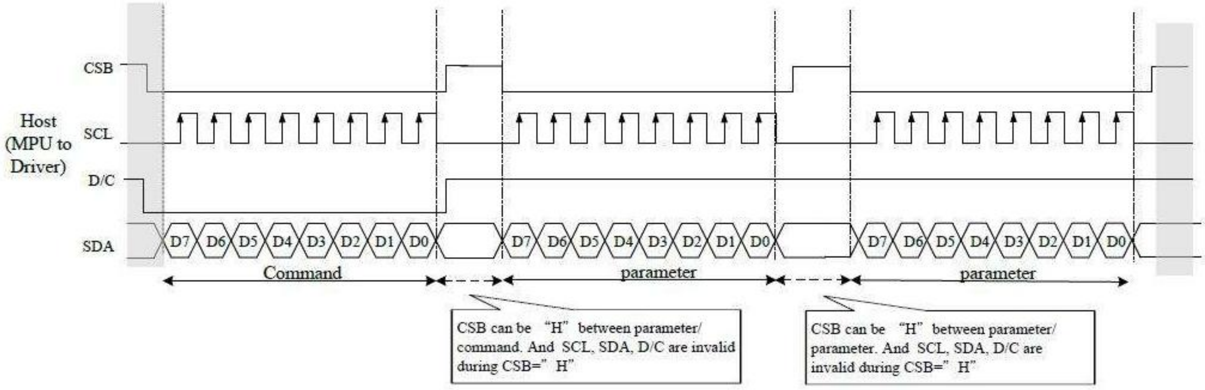


Figure 6-3-1: 4-wire SPI mode

6.3.3 MCU Serial Interface (3-wire SPI)

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

Table 6-3-3: Control pins of 3-wire Serial Peripheral Interface

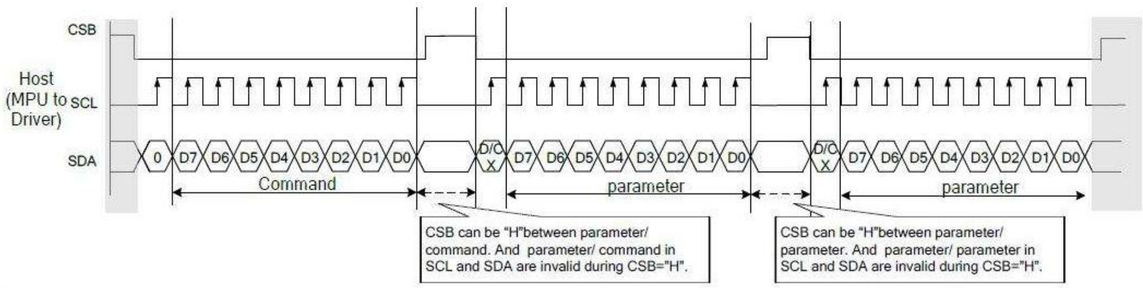
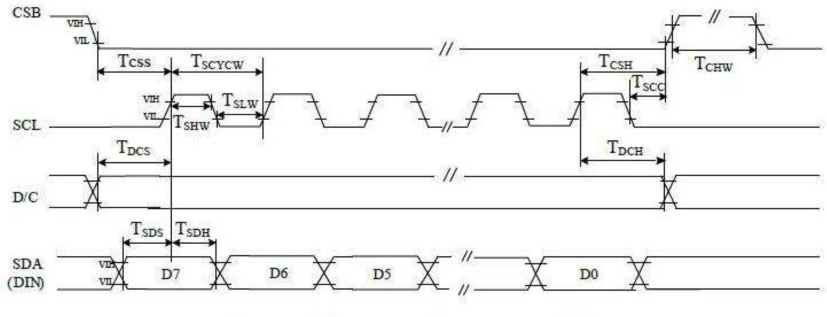
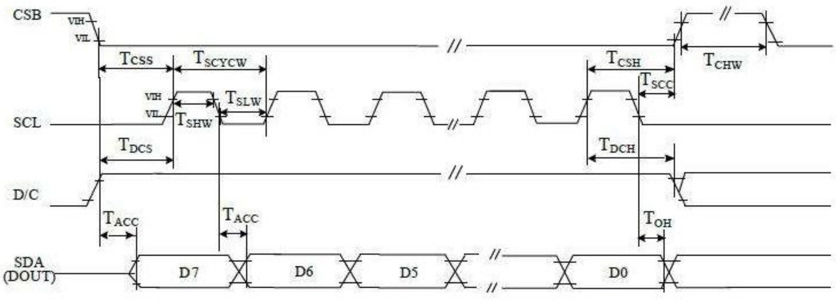


Figure 6-3-2: 3-wire SPI mode

6.3.4 Interface Timing



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics (read mode)

Figure 6-3-3: 4-pin serial interface characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB select setup time	TBD			ns
t_{SCH}	CSB select hold time	TBD			ns
t_{SCC}	CSB deselect setup time	TBD			ns
t_{CHW}	CSB deselect hold time	TBD			ns
t_{SCYCW}	Serial clock cycle (Write)	TBD			ns
t_{SHW}	SCL "H" pulse width (Write)	TBD			ns
t_{SLW}	SCL "L" pulse width (Write)	TBD			ns
t_{SCYCL}	Serial clock cycle (Read)	TBD			ns
t_{SHR}	SCL "H" pulse width (Read)	TBD			ns
t_{SLR}	SCL "L" pulse width (Read)	TBD			ns
t_{SDS}	Data setup time	TBD			ns
t_{SDH}	Data hold time	TBD			ns
t_{ACC}	Access time			TBD	ns
t_{OH}	Output disable time	TBD			ns

Table 6-3-4: Serial Interface Timing Characteristics

7. COMMAND TABLE

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0] = 0Fh [POR] B[7:0] = 09h [POR]
0	1		A_7	A_6	A_5	0	A_3	A_2	A_1	A_0		A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: 960 x 680 (Default) 01b: 960 x 672 10b: 960 x 640 11b: 880 x 528 A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 … G0 1: Scan up. (Default) First line to Last line: G0 … Gn-1 A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 … S0 1: Shift right. (Default) First data to Last data: S0 … Sn-1 A[1] ~ SHD_N Booster and Regulator Switch: 0: PON / POF command will not execute 1: PON / POF command will execute (Default) A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N signal will become "0" until Soft reset is finished.
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

<table>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="3">PWR</td><td>Power setting Register
A[5:0] = 07h [POR]
B[7:0] = F0h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td><td>A[2:0] = 111 [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>B_1</td><td>B_0</td><td>B[1:0] ~ VGPN [1:0]
Internal VGH / VGL Voltage Level Selection:
<table>
<tr><td>VGPN [1:0]</td><td>Gate Voltage Level</td></tr>
<tr><td>00</td><td>VGH=20V,VGL=-20V (Default)
VSH=15V, VSL=-15V</td></tr>
<tr><td>01</td><td>VGH=17V ,VGL=-17V
VSH=15V, VSL=-15V</td></tr>
<tr><td>10</td><td>VGH=15V,VGL=-15V
VSH=15V, VSL=-15V</td></tr>
<tr><td>11</td><td>Reserved.</td></tr>
</table></td></tr>
<tr><td colspan="13"></td></tr>
</table>

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	02	0	0	0	0	0	0	1	0	POF	Power OFF Command Register
0	1		0	0	0	0	0	0	0	0		After power off command, driver will power off based on the Power OFF Sequence, then BUSY_N signal will become "0". The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. *Remark: POF works at PON only
0	0	04	0	0	0	0	0	1	0	0	PON	Power ON Command Register After the Power ON command, driver will power on based on the Power ON Sequence. After power on command and all power sequence are ready, then BUSY_N signal will become "1". * Remark: PON Include booster on, VSHx/VSLx regulator on With default BTST, timing is >80ms

0	0	06	0	0	0	0	0	1	1	0	BTST	VGH Booster Soft Start Setting Register (for VGH) A[6:0] = 0Fh [POR] B[6:0] = 8Bh [POR] C[6:0] = 93h [POR] D[6:0] = A1h [POR] A[3:2] ~ T_VGHSSA [1:0] = 11 (Default) VGH booster soft start Phase A duration A[1:0] ~ T_VGHSSB [1:0] = 11 (Default) VGH booster soft start Phase B duration (Soft Start Phase Period (ms)): 00 → 10; 01 → 20; 10 → 30; 11 → 40 B[6:4] ~ VGHSSA_DRV [2:0], = 000 (Default) VGH Phase A Driving Strength C[6:4] ~ VGHSSB_DRV [2:0], = 001 (Default) VGH Phase B Driving Strength D[6:4] ~ VGHSSC_DRV [2:0] = 001 (Default) VGH Phase C Driving Strength 000~011 for Driving Strength 0~3. Others are reserved. B[3:0] ~ VGHSSA_OFFT[[3:0], = 1011 (Default) VGH Phase A Minimum OFF Time C[3:0] ~ VGHSSB_OFFT[[3:0], = 0011 (Default) VGH Phase B Minimum OFF Time D[3:0] ~ VGHSSC_OFFT[[3:0], = 0011 (Default) VGH Phase C Minimum OFF Time 0000~1111 for Minimum OFF Time (setting) OFFH0 to OFFHF.
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		1	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

	Soft Start Phase Period (ms)
00	10
01	20
10	30
11	40

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>07</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="2">DSLP</td><td rowspan="2">Deep Sleep Register
This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion.
The only one parameter is a check code, the command would be executed if check code is A5h.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>17</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="2">AUTO</td><td>Auto Sequence Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>This command makes the chip enter the auto sequence
Single-chip application ONLY.
Auto Sequence Option
0xA5: Start Auto Sequence (PON > DRF > POF)
0xA7: Start Auto Sequence (PON > DRF > POF > DSLP).
Others: No effect
BUSY_N signal will become “0” until Auto Sequence is finished.</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="5">DTM</td><td rowspan="5">Data Start transmission Register
This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.

KPixel[1:0] Source Driver Output
<table><tr><td></td><td>DDX=1
(Default)</td></tr><tr><td>00b</td><td>Gray 0</td></tr><tr><td>01b</td><td>Gray 1</td></tr><tr><td>10b</td><td>Gray 2</td></tr><tr><td>11b</td><td>Gray 3</td></tr></table>After issue this command, the host must send at least 1 byte data to the device.</td></tr>
<tr><td colspan="11">2 bit per pixel</td></tr>
<tr><td>0</td><td>1</td><td></td><td colspan="2">KPixel1
[1:0]</td><td colspan="2">KPixel2
[1:0]</td><td colspan="2">KPixel3
[1:0]</td><td colspan="2">KPixel4
[1:0]</td></tr>
<tr><td>:</td><td></td><td></td><td colspan="2"></td><td colspan="2"></td><td colspan="2"></td><td colspan="2"></td></tr>
<tr><td>0</td><td>1</td><td></td><td colspan="2">KPixel
(4M-3)
[1:0]</td><td colspan="2">KPixel
(4M-2)
[1:0]</td><td colspan="2">KPixel
(4M-1)
[1:0]</td><td colspan="2">KPixel
(4M)
[1:0]</td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">DRF</td><td rowspan="2">Display Refresh Command Register
After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. LUT can define DCVCOM/ACVCOM.
After Display Refresh command, BUSY_N signal will become “0” until display update is finished.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		This command enables internal temperature sensor. BUSY_N will go low during temperature sensor is under operation. Then the temperature value can be read in 1degC step A[7:0] ~ TS [7:0]

TS [7:0]	Return Value(degC)
E7h	-25
…	…
FFh	-1
00h	0
01h	1
…	…
19h	25
…	…
31h	49
32h	50

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	50	0	1	0	1	0	0	0	0	CDI	A[7:0] = 97h [POR]
0	1		A_7	A_6	A_5	0	0	0	0	0		A[7:5]~VBD [2:0] Border Output Selection:

	DDX=1
VBD[2:0]	LUT (Default)
000	Gray 0
001	Gray 1
010	Gray 2
011	Gray 3
100	HIZ(Default)

0	0	61	0	1	1	0	0	0	0	1	TRES	Resolution setting Register This command defines alternative resolution
0	1		0	0	0	0	0	0	A_9	A_8		A[7:0] ~ HRES[9:0] Horizontal Display Resolution Remark: Horizontal resolution should be 4-multiple. B[8:0] ~ VRES[9:0] Vertical Display Resolution e.g. HRES= 3C0h, VRES= 2A8h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	B_9	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

UD,SHL	Source and gate sequence
00	S679,G959 to S0,G0
01	S0, G959 to S679,G0
10	S679,G0 to S0, G959
11	S0,G0 to S679, G295

Remark:
1) Both PSR.RES & TRES command can set panel resolution. Priority will be given to the last received PSR or TRES command.
2) VRES[8:0] >= 120

0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		The command is to read the ID A[7:0] = 07h [POR]

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>80</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>AMV</td><td>Auto Measurement VCOM Register
This command implements related VCOM sensing setting.
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>0</td><td>A_0</td><td></td><td>A[7:6] ~ P[1:0]
Number of sensing Points
00: 2 (Default)
01: 4
10: 8
11: 16

A[5:4] ~AMVT[1:0]
Auto Measure Vcom Time:
Sensing Time
00: 5 sec. (Default)
01: 10 sec.
10: 15 sec.
11: 20 sec.

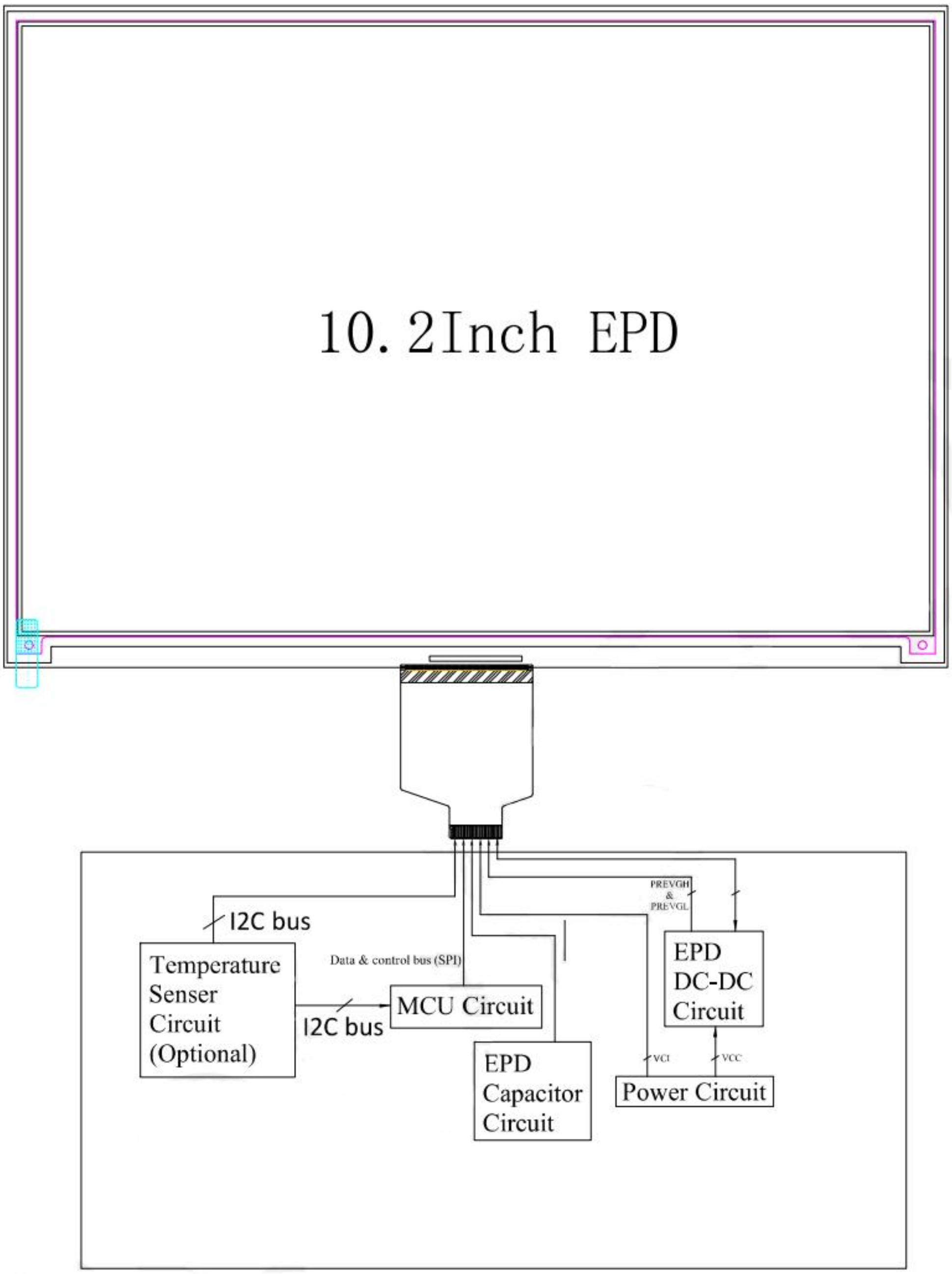
A[0] ~ AMVE
Auto Measure Vcom Enable (/Disable):
0: Disabled (Default)
1: Enabled
Requirement:
1) AMV works at PON only
2) BUSY_N signal will become "0" until Vcom sensing is finished.</td></tr>
<tr><td>0</td><td>0</td><td>81</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>VV</td><td>Auto Measurement VCOM Register
This command gets the Vcom value after AMV.</td></tr>
<tr><td>1</td><td>1</td><td></td><td>1</td><td>0</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[5:0] ~ VV[5:0]:
Vcom read Value , valid range from -0.2V to -4.0V.<table><tr><td>VV[5:0]</td><td>Vcom read value</td></tr><tr><td>00h</td><td>Reserved</td></tr><tr><td>04h</td><td>-0.2V</td></tr><tr><td>08h</td><td>-0.4V</td></tr><tr><td>0Ch</td><td>-0.6V</td></tr><tr><td>10h</td><td>-0.8V</td></tr><tr><td>...</td><td>...</td></tr><tr><td>50h</td><td>-4.0V</td></tr><tr><td>others</td><td>Reserved</td></tr></table></td></tr>
</table>

0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	0	0		A[7] ~ OTP_VCM Vcom follow VDCS after RESET. 0: Disable (Default), auto load from OTP if it is valid. 1: Enable, VCOM value from the VDCS[6:0] A[6:0] ~ VDCS[6:0]: VCOM_DC Setting, 0.2V step from -0.2V to -4.0V.

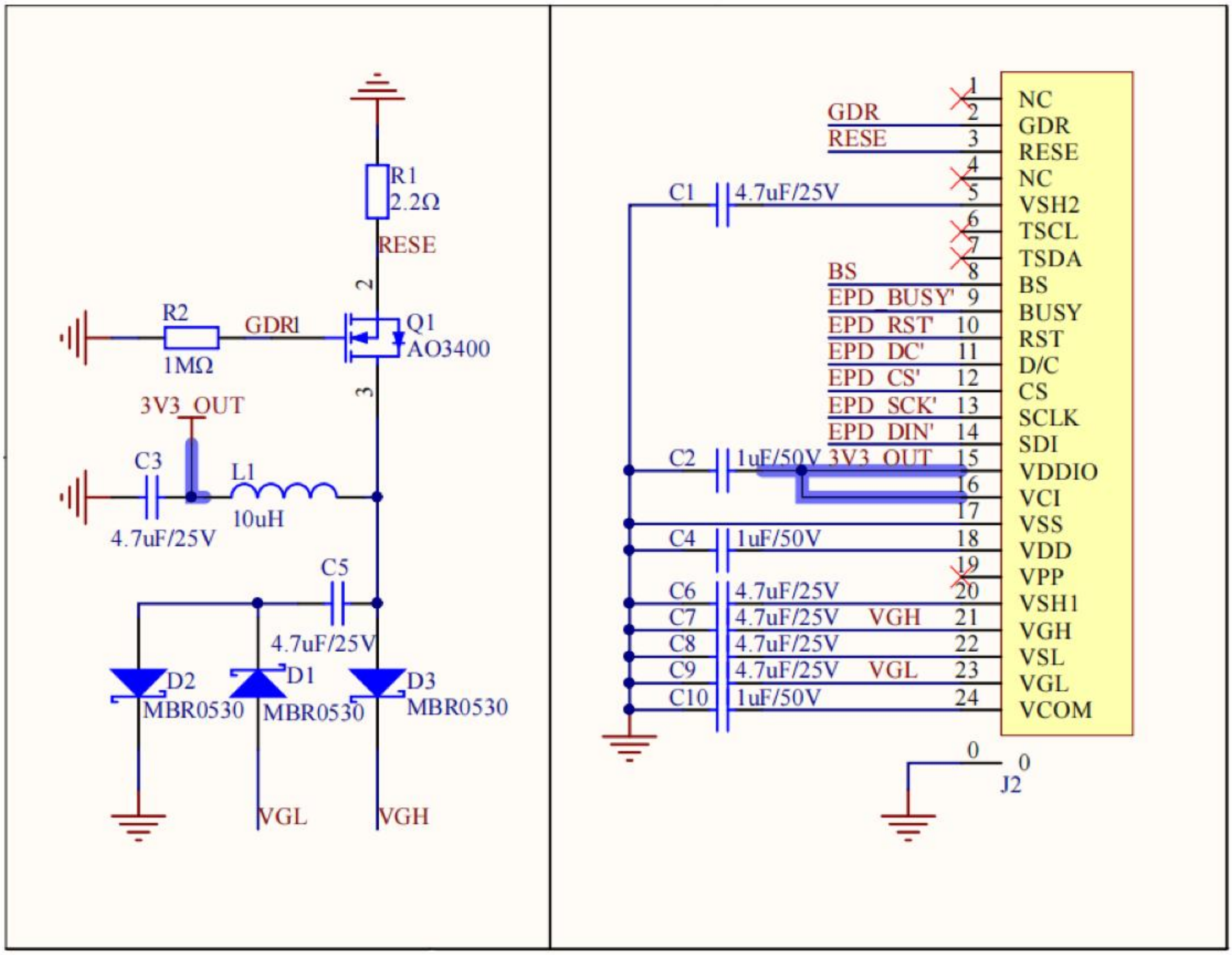
VDCS [6:0]	VCOM_DC Setting
00h	Reserved
04h	-0.2V
08h	-0.4V
0Ch	-0.6V
10h	-0.8V
…	…
50h	-4.0V
others	Reserved

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	90	1	0	0	1	0	0	0	0	PGM	Program Mode This command is to set OTP program mode After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leave the program mode BUSY_N signal will become 0 until PGM mode is ready.
0	0	91	1	0	0	1	0	0	0	1	APG	Active Program This command is to execute OTP program After this command is issued, the chip would program the OTP. BUSY_N signal will become 0 until the programming is completed. Requirement: In PON mode with internal programming power.
0	0	92	1	0	0	1	0	0	1	0	ROTP	Read OTP Data This command is to read the OTP content from SRAM. The 1st byte read is dummy byte. The 2nd byte read is the content of Address 0 in OTP The N+1th byte read is the content of Address n in OTP After issue this command, the host must read at least 1 byte data from the device.
1	1		1st ~ dummy 2nd ~ N+1th Parameter									
0	0	E3	1	1	1	0	0	0	1	1	PWS	Power Saving Register This command is sets for saving power VCOM/Source power saving during display refresh period. A[7:0] = 65h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

8. BLOCK DIAGRAM

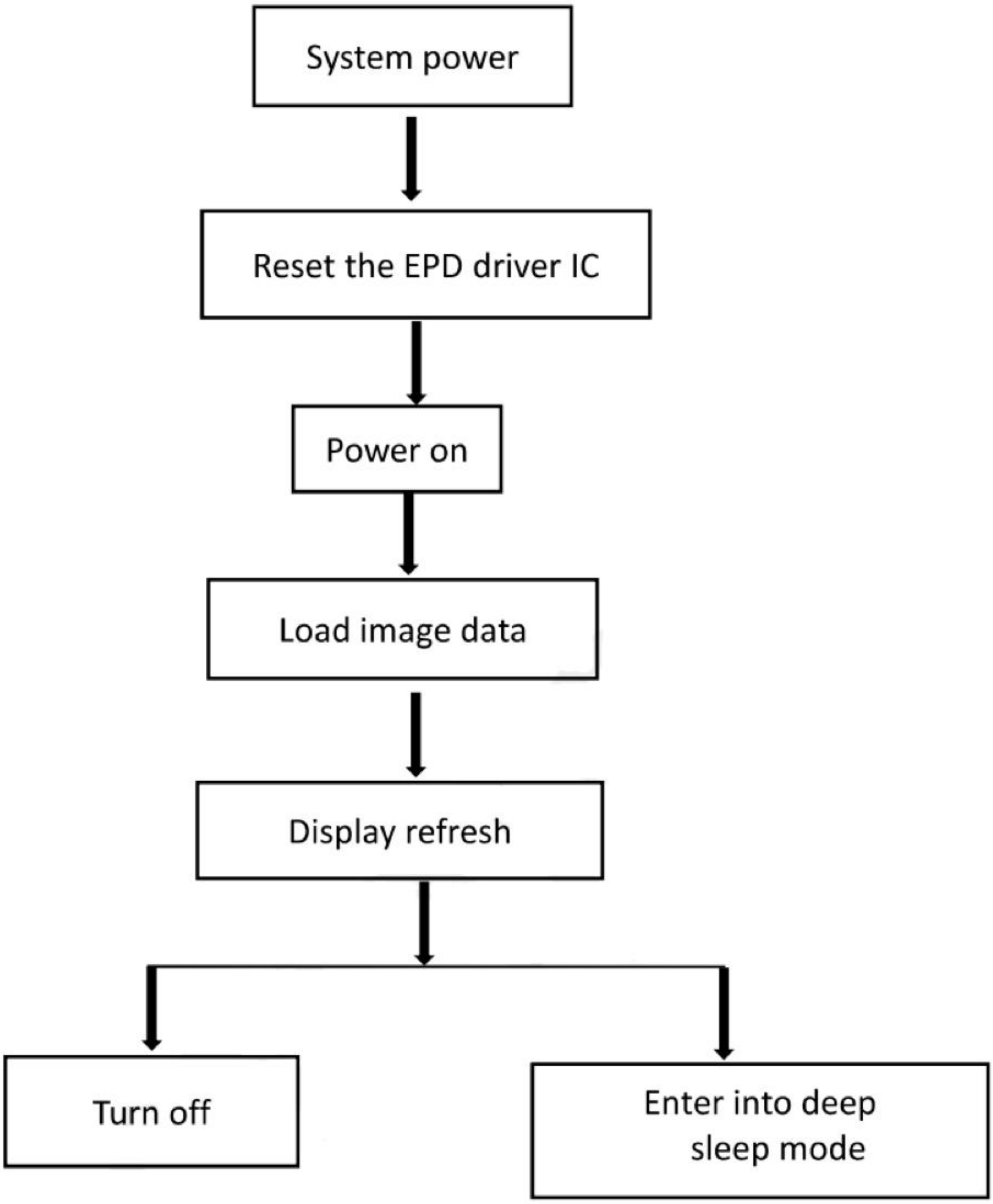


9. TYPICAL APPLICATION CIRCUIT WITH SPI INTERFACE

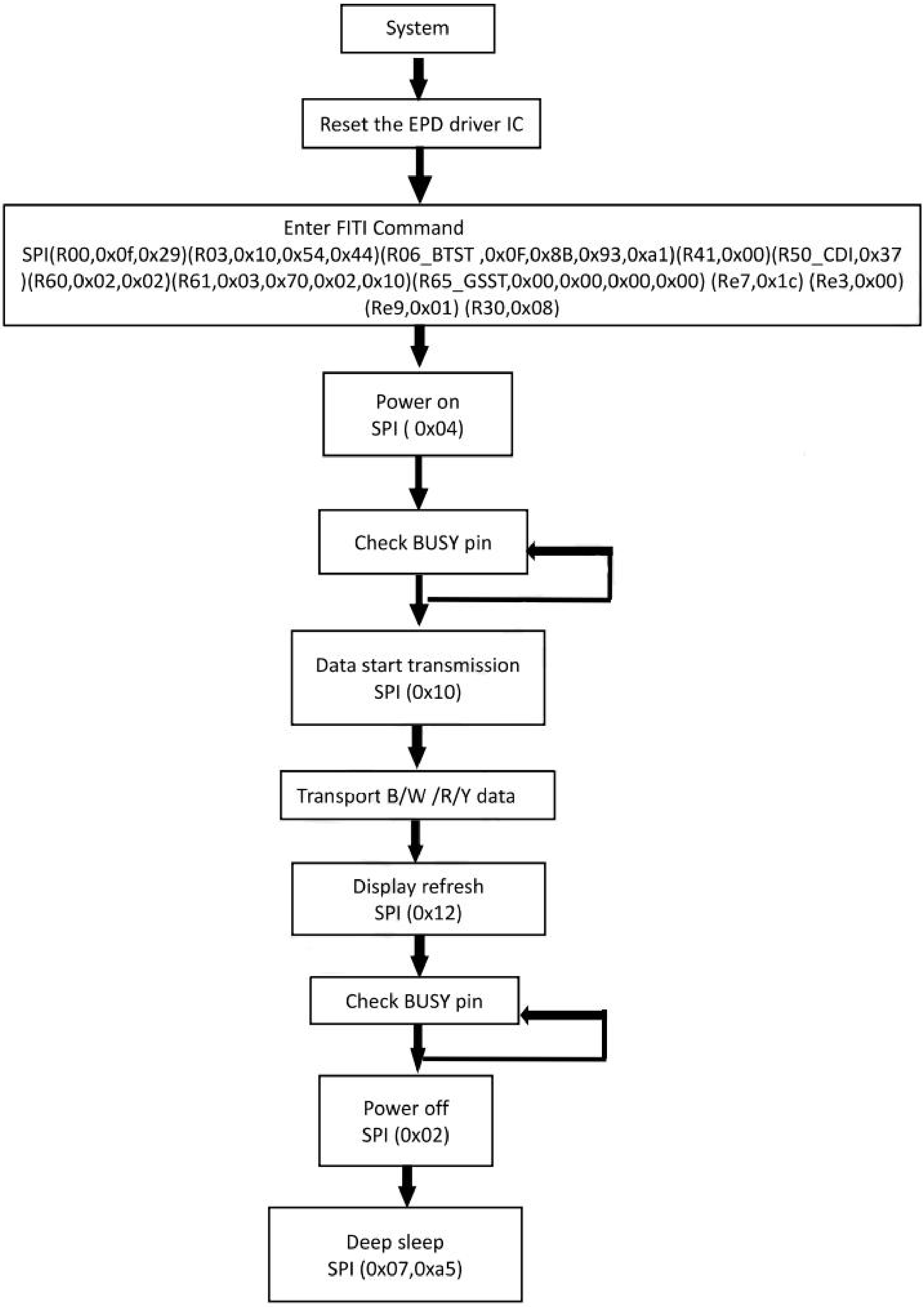


10. TYPICAL OPERATING SEQUENCE

10.1 LUT FROM OTP OPERATION FLOW



10.2 OTP OPERATION REFERENCE PROGRAM CODE



11. RELIABILITY TEST

No.	Test Items	Test Conditions
1	Low-Temperature Storage	T= -25°C, 500h Test in white pattern
2	High-Temperature Storage	T= 60°C, RH=35%, 500h Test in white pattern
3	High-Temperature Operation	T= 50°C, RH=30%, 500h
4	Low-Temperature Operation	0°C, 500h
5	High-Temperature, High-Humidity Operation	T= 40°C, RH=90%, 500h
6	High-Temperature, High-Humidity Storage	T= 60°C, RH=80%, 500h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min] → [+60°C 30min]:100 cycles Test in white pattern

Notes:

11-1: Stay white pattern for storage and non-operation test.

11-2: The operation is black → white → red → yellow pattern, the interval is 150s.

11-3: Put in 20°C--25 °C for 1 hour after test finished. The functionality, appearance, and display performance are OK.

12. QUALITY ASSURANCE

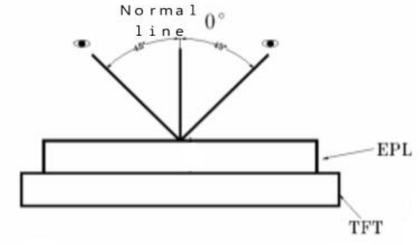
12.1 ENVIRONMENT

Temperature: 18~28℃; Humidity: 40%~70%RH

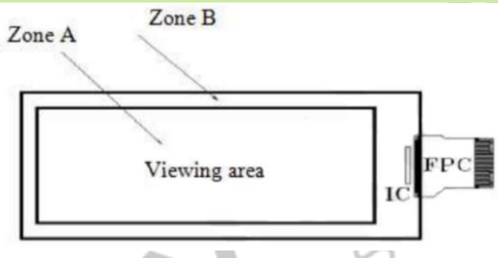
12.2 ILLUMINANCE

Brightness: 800~1500LUX;
Angle: The light source surrounds the module at a 45±5° angle;
Functional tests are performed at a distance of 30CM from the module surface under 150-200 LUX

12.3 INSPECTION METHOD

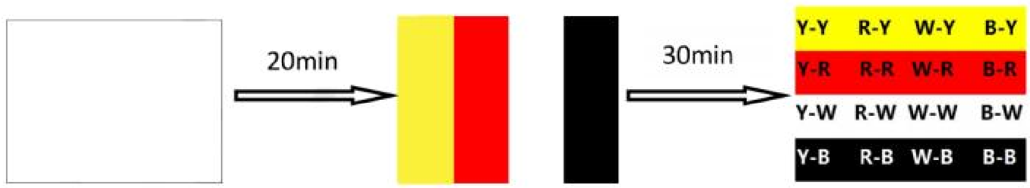


12.4 DISPLAY AREA



12.5 GHOSTING TEST METHOD

Four-color ghosting is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.



1) Measurement Instruments: X-rite i1Pro
2) Ghosting formula:

W ghosting: ΔE=Max(ΔEab(Y-W,R-W), ΔEab(Y-W,W-W), ΔEab(Y-W,B-W), ΔEab(R-W,W-W), ΔEab(R-W,B-W), ΔEab(W-W,B-W))

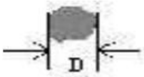
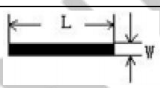
K ghosting: ΔE=Max(ΔEab(Y-B,R-B), ΔEab(Y-B,W-B), ΔEab(Y-B,B-B), ΔEab(R-B,W-B), ΔEab(R-B,B-B), ΔEab(W-B,B-B))

R ghosting: ΔE=Max(ΔEab(Y-R,R-R), ΔEab(Y-R,W-R), ΔEab(Y-R,B-R), ΔEab(R-R,W-R), ΔEab(R-R,B-R), ΔEab(W-R,B-R))

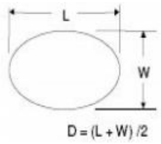
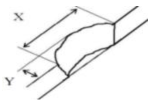
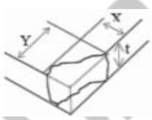
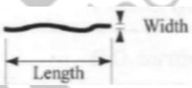
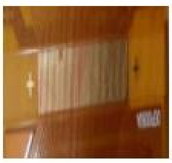
Y ghosting: ΔE=Max(ΔEab(Y-Y,R-Y), ΔEab(Y-Y,W-Y), ΔEab(Y-Y,B-Y), ΔEab(R-Y,W-Y), ΔEab(R-Y,B-Y), ΔEab(W-Y,B-Y))

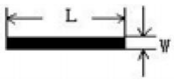
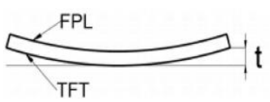
12.6 INSPECTION STANDARDS

12.6.1 Electric Inspection Standards

No.	Item	Standard	Defect Level	Method	Scope
1	Display	Clear display; Display complete; Display uniform	MA		
2	Black/Write spots	 D≤0.3mm, negligible; 0.3mm<D≤0.5mm, N≤5 allowed; D>0.5mm, not allowed	MI	Visual inspection	Zone A
3	Black/White lines (No switch)	 L≤1.0mm, W≤0.15mm, negligible; 1.0mm<L≤4.0mm,0.15mm<W≤0.5mm, N≤4 allowable; L>4.0mm,W>0.5mm, not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot/ Multilateral	Flash points are allowed when switching screens; Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not allowed			

12.6.2 Appearance Inspection Standards

No.	Item	Standard	Defect Level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.3mm, negligible; 0.3mm<D≤0.5mm, N≤5 allowable; D>0.5mm, not allowed	MI	Visual inspection	Zone A
2	Glass crack	Not allowed	MA	Visual /Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm, t=not counted, and without affecting the electrode, permissible  X≤2mm or Y≤2mm t=not counted and without affecting the electrode, permissible  W≤0.1mm, L≤5mm, without affecting the electrode, n≤2	MI	Visual /Microscope	Zone A Zone B
5	TFT cracks	 Not allowed	MA	Visual /Microscope	Zone A Zone B
6	Dirty/Foreign bodies	Allowed if can be removed/Allowed	MI	Visual /Microscope	Zone A Zone B
7	FPC broken/FPC oxidation/scratch	  Not allowed	MA	Visual /Microscope	Zone B

8	B/W line	 L≤1.0mm, W≤0.15mm, negligible; 1.0mm<L≤4.0mm, 0.15mm<W≤0.5mm, N≤4 allowable; L>4.0mm, W>0.5mm, not allowed	MI	Visual /Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: X≤3mm,Y≤0.3mm, allowed TFT chromatic aberration: allowed	MI	Visual /Microscope	Zone A Zone B
10	Electrostatic point	D≤0.25mm, allowed; 0.25mm<D≤0.4mm, N≤4 allowed; D>0.4mm is not allowed (n≤8 items are allowed within 5mm in diameter)	MI	Visual /Microscope	Zone A
11	PCB damaged /Poor welding /Curl	PCB(Circuit area) damaged, not allowed PCB Poor welding, not allowed PCB Curl≤1%	MI	Visual /Ruler	
12	Edge glue height /Edge glue bubble	Edge adhesives H≤PS surface (including protective film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesive bubble: bubble width≤1/2 Margin width; Length≤5.0mm. n≤5	MI		Zone B
13	Protective film	Surface scratch but not effect protection function, allowed	MI	Visual inspection	
14	Silicon glue	Thickness≤PS surface(with protective film): Full cover the IC; Shape: The width on the FPC≤0.5mm(Front) The width on the FPC≤1.0mm(Back) Smooth surface, no obvious protrusions	MI	Visual inspection	
15	Wrap degree (TFT substrate)	 t ≤1.5mm	MI	Ruler	
16	Color difference in COM area(Silver point area)	Allowed		Visual inspection	

13. HANDLING, SAFETY, AND ENVIRONMENT REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

14. PRECAUTIONS

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.
(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue.
(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.