13.3inch e-Paper (E)

User Manual

Revision History

Version	Content	Date	Page
1.0	New creation	2024/11/15	All

Contents

1. OVERVIEW

13.3inch e-Paper (E) is a reflective Electrophoretic E Ink technology display module based on active matrix TFT substance. It has 13.3inch active area with 1200×1600 pixels and 3:4 aspect ratios. The display is capable to display images at red/green/blue/yellow/black/white depending on the display controller and the associated waveform file it used.

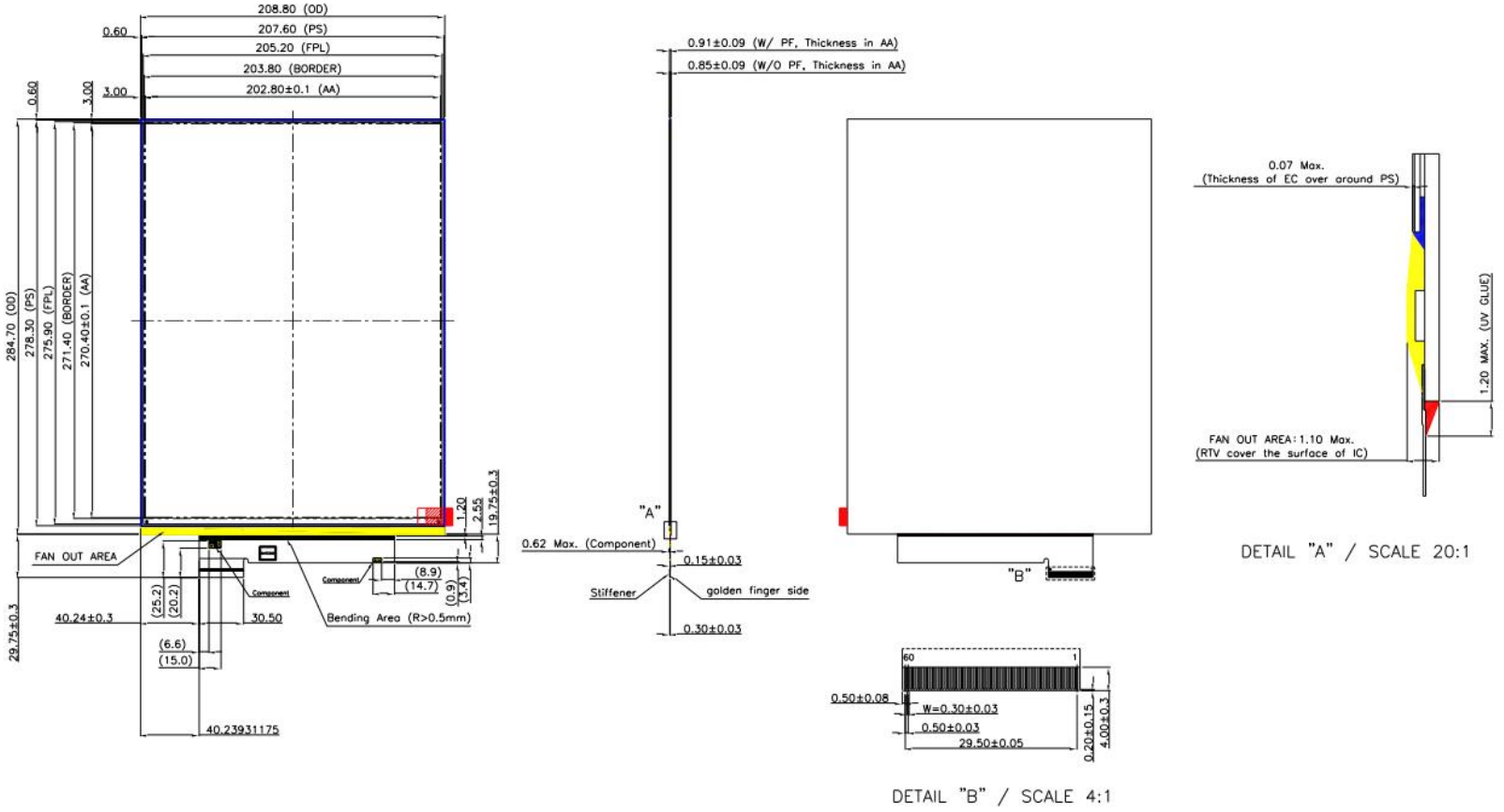
2. FEATURES

- ✧ 1200×1600 pixels display
- ✧ High contrast Electrophoretic imaging film
- ✧ Ultra wide viewing angle
- ✧ Ultra low power consumption
- ✧ Pure reflective mode
- ✧ Bi-stable display
- ✧ Commercial temperature range: 0℃～50℃
- ✧ Landscape and portrait modes

3. MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit	Remark
Screen Size	13.3	Inch	150ppi
Display Resolution	1200 (H) x 1600 (V)	Pixel	3:4
Active Area	202.8 (H) x 270.4 (V)	mm	
Pixel Pitch	0.169 x 0.169	mm	
Pixel Configuration	Square		
Outline Dimension	208.8 (H) × 284.7 (V) × 0.85 (D)	mm	Without masking film
Module Weight	50 ± 10	g	
Display operating mode	Reflective mode		
Surface treatment	Anti-glare treatment for protective sheet		

4. MECHANICAL DRAWING OF EPD MODULE



Note: 1. General tolerance is ±0.3; 2. ( ) is reference dimension.

5. PIN ASSIGNMENT

NO.	Type	Name	Description
1	P	VCOMBD_M	VCOMBD driving voltage (Master)
2	I	RESEC	Current sense input pin for the control loop (VCOM)
3	O	GDRC	N-Channel MOSFET gate drive control (VCOM)
4	I	RESEN	Current sense input pin for the control loop (VDDN)
5	O	GDRN	P-Channel MOSFET gate drive control pin (VDDN)
6	I	RESEP	Current sense input pin for the control loop (VDDP)
7	O	GDRP	N-Channel MOSFET gate drive control pin (VDDP)
8	P	GND	Ground
9	P	AVDD	2.3~6V for analog voltage supply (DC/DC)
10	P	VDD	2.3~3.6V for analog /digital voltage supply
11		NC	No connection and do not connect with other NC pins
12	P	VCC	LDO output pin
13	P	VDDP	Positive power supply for analog circuit
14	P	VDDP	Positive power supply for analog circuit
15		NC	No connection and do not connect with other NC pins
16	P	VDDN	Negative power supply for analog circuit
17	P	VDDN	Negative power supply for analog circuit
18	P	VCCI	Positive power supply only for Oscilltor
19	P	VDDIO	Power input for IO
20	I/O	TSCL	I2C Interface to digital temperature sensor Clock pin
21	I/O	TSDA	I2C Interface to digital temperature sensor Data pin
22	I	BS0	Input interface setting. Select 3 wire/ 4 wire/ **Quad** SPI interface **(Default :H)**
23	I	BS1	Input interface setting. Select 3 wire/ 4 wire/ **Quad** SPI interface **(Default :H)**
24	I	RES#	Reset
25	O	BUSY_N	This pin indicates the driver status. Connect with a pull up resistor to VDDIO
26	I	D/C#	Command/Data input. L: command H: data. (4-wire SPI) Connect to GND in 3-wire mode or standard 4-wire mode
27	I	CSB_M	Serial communication chip select (Master)
28	I	SCL	Serial communication clock input
29	I/O	SI0	Serial communication data input/output (3-wire/4-wire SPI) Serial communication data input (Standard 4-wire SPI)
30	I/O	SI1	Serial communication data input. Serial communication data output (Standard 4-wire SPI)
31	I	SI2	Serial communication data input (Standard 4-wire SPI Quad mode)

32	I	SI3	Serial communication data input (Standard 4-wire SPI Quad mode)
33	O	DRVP_Gate	Driving external N-MOSFET(VGP)
34	I	FBP	Positive charge pump(VGP) feedback pin
35	P	GND	Ground
36	O	VCOMBD_S	VCOMBD driving voltage (Slave)
37	O	DRVN	Driving external BTJ (VGN)
38	I	FBN	Negative charge pump feedback pin (VGN)
39	O	REG_VGN	VGN internal reference voltage output
40	O	DRVN2	Driving external BTJ. (VNCP_3P5V)
41	P	VNCP_3P5V	Negative power supply for analog bias1 circuit. (for TFT_Vcom)
42	P	VSPH	Positive Source driving voltage
43	P	VSPL	Positive Source driving voltage
44	P	VSPL2	Positive Source driving voltage
45	P	VSPHI	Positive source voltage
46	P	VSPLI	Positive source voltage
47	P	VSPL2I	Positive source voltage
48	P	VSNH	Negative source buffer output
49	P	VSNL	Negative source buffer output
50	P	VSPL2	Negative source buffer output
51	P	VSPL2I	Negative source voltage
52	P	VSNLI	Negative source voltage
53	P	VSNHI	Negative source voltage
54	O	FPL_VCOM	FPL_VCOM driving voltage
55	O	TFT_VCOM	TFT_VCOM driving voltage
56	P	VBB_3P5V	Negative power supply for analog bias2 circuit (for TFT_Vcom)
57	-	NC	No connection and do not connect with other NC pins
58	I	CSB_S	Serial communication chip select (Slave)
59	P	VGH	Positive Gate driving voltage
60	P	VGL	Negative Gate driving voltage

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin

Note 5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin (BUSY_N) is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting display waveform; or

- Programming with OTP

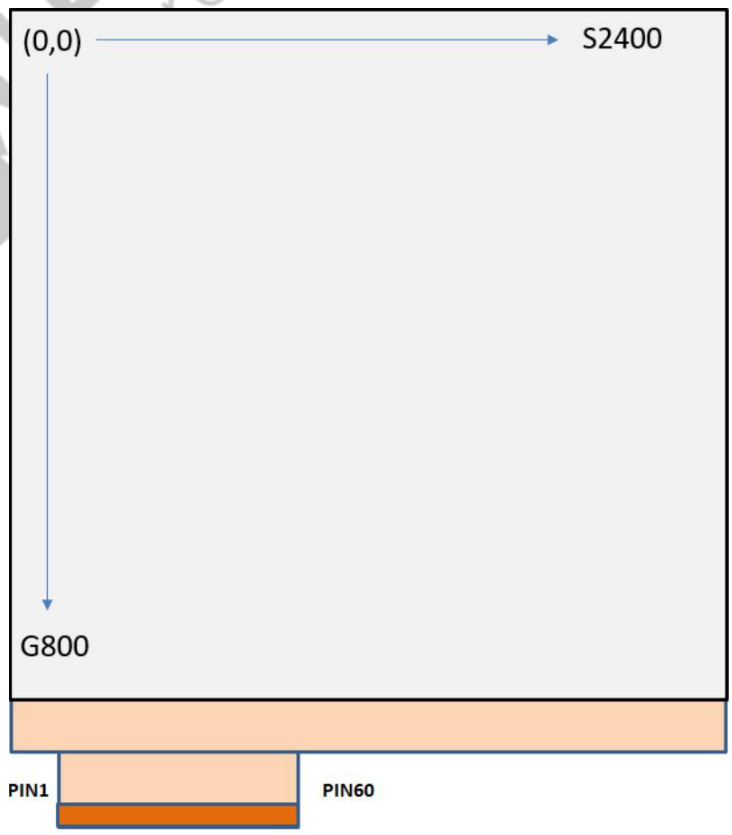
- Communicating with digital temperature sensor

Note 5-5: This pin (BS0/BS1) is for 3-line SPI /4-line SPI/QSPI selection. Please refer to below Table.

Table: Bus interface selection

BS1	BS0	MPU Interface
L	L	4-line serial peripheral interface(SPI)
L	H	3- line serial peripheral interface(SPI) - 9 bits SPI
H	L	Standard 4-wire SPI
H	H	Standard 4-wire SPI (Default)

Note 6: Panel Scan Directions



Golden finger down

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Analog power	V_{DD}	-0.5 to +3.6	V
Operating temp range	T_{OPR}	0 to +40	ºC
Storage temp range	T_{STG}	-25 to +60	ºC

Note:

Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

6.2 DISPLAY MODULE DC CHARACTERISTICS

The following specifications apply for: VDD=3.0V, TA =25ºC.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Logic supply voltage		2.4	3.0	3.6	V
V_{GH}	Positive gate driving voltage		26	27	28	V
V_{GL}	Negative gate driving voltage		-21	-20	-19	V
V_{SPH}	Positive source driving voltage 1		-	Adjusted	-	V
V_{SPH2}	Positive source driving voltage 2		-	Adjusted	-	V
V_{SNH}	Negative source driving voltage 1		-	Adjusted	-	V
V_{SNH2}	Negative source driving voltage 2		-	Adjusted	-	V
V_{COM_DC}	VCOM_DC output voltage		-4.0	Adjusted	0.3	V
V_{COM_AC}	VCOM_AC output voltage		V_{SL}+ V_{COM_DC}	-	V_{SH}+ V_{COM_DC}	V
V_{IL}	Low level input voltage	Digital input pins	GND	-	0.2xV_{DD}	V

V_{IH}	High level input voltage	Digital input pins	0.8xV_{DD}	-	V_{DD}	V
V_{OH}	High level output voltage	Digital output pins, I_{OUT} = 1mA,V_{DD} = 2.4V	0.8xV_{DD}	-	-	V
V_{OL}	Low level output voltage	Digital output pins, I_{OUT} = 1mA,V_{DD} = 2.4V	GND	-	0.2xV_{DD}	V
I_{MSTB}	Module stand-by current	Stand-by mode	-	TBD	-	uA
I_{MDS}	Module deep sleep current	Deep sleep mode	-	TBD	-	uA
I_{NC}	Inrush current	Booster on	-	592	879.8	mA
I_{PC}	Driving peak current	TYP loading pattern	-	195.2	310.1	mA
		High loading pattern	-	887.6	1400.5	mA
I_{MOPR}	Module operating current	TYP loading pattern	-	50.8	80.4	mA
		High loading pattern	-	460.2	750.0	mA
P	Operation power dissipation	TYP loading pattern V_{DD}=3.0V with DC-DC	-	150.6	241.2	mW
		High loading pattern V_{DD}=3.0V with DC-DC	-	1218.6	2250	mW
P_{STBY}	Standby power dissipation	V_{DD}=3.0V	-	TBD	-	mW

Note: The Module operating current data is measured by using Oscilloscope, and extract the Mean value.

1. The typical power consumption is measured using associated 25C waveform with following pattern transition: from full white pattern to color stripe pattern. (Note 7-1).

2. The high loading power consumption is measured using associated 25C waveform with following pattern transition: from full white pattern to noise pattern (including random scattering of 4 colors) (Note 7-2).

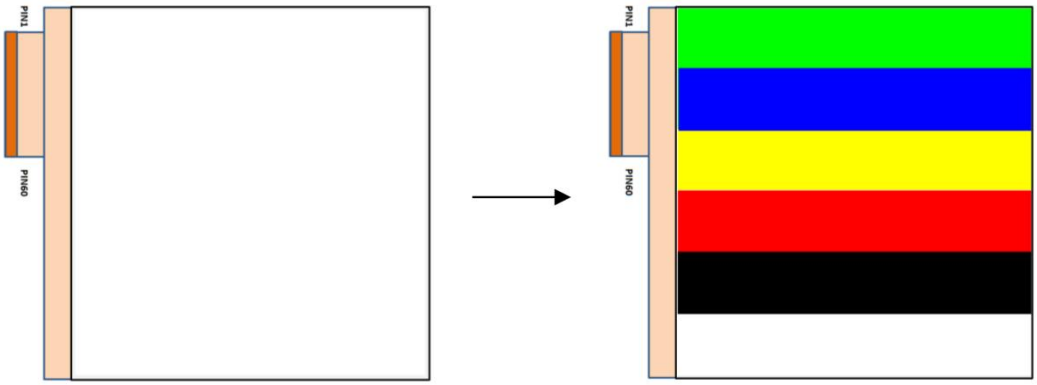
3. The minimum VDD value by 2.4V is based on typical application pattern with stable and continuing power supply. It does not apply on high loading pattern such as Note 7-2.

4. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.

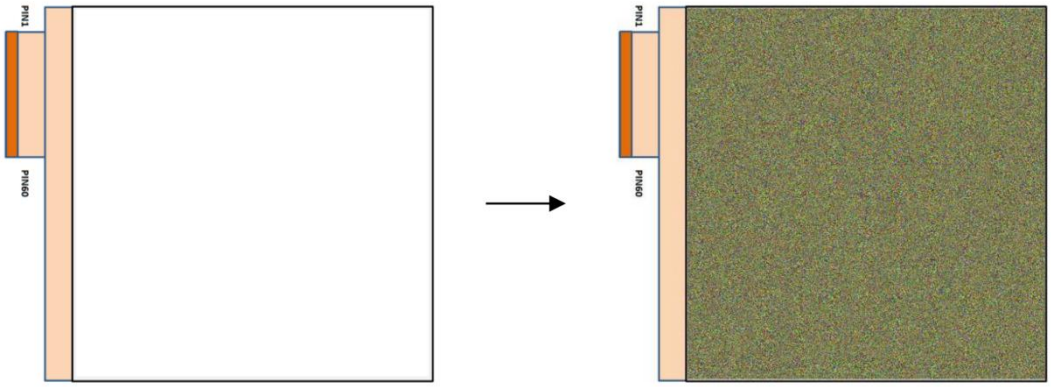
5. Vcom value has been set in the IC chip on the panel.

Note 6-1

The typical power consumption



Note 6-2
The high loading power consumption



6.3 PANEL AC CHARACTERISTICS

6-3-1 MCU Interface

6-3-1-1 MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

Table 6-1: MCU interface assignment under different bus interface mode

Note 6-3: L is connected to GND

Note 6-4: H is connected to VDD

6-3-1-2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDA, D/C#, CS#.

Function	CS#	D/C#	SCLK
Write command	L	L	↑
Write data	L	H	↑

Table 6-2: Control pins of 4-wire Serial Peripheral interface

Note 6-5: ↑stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

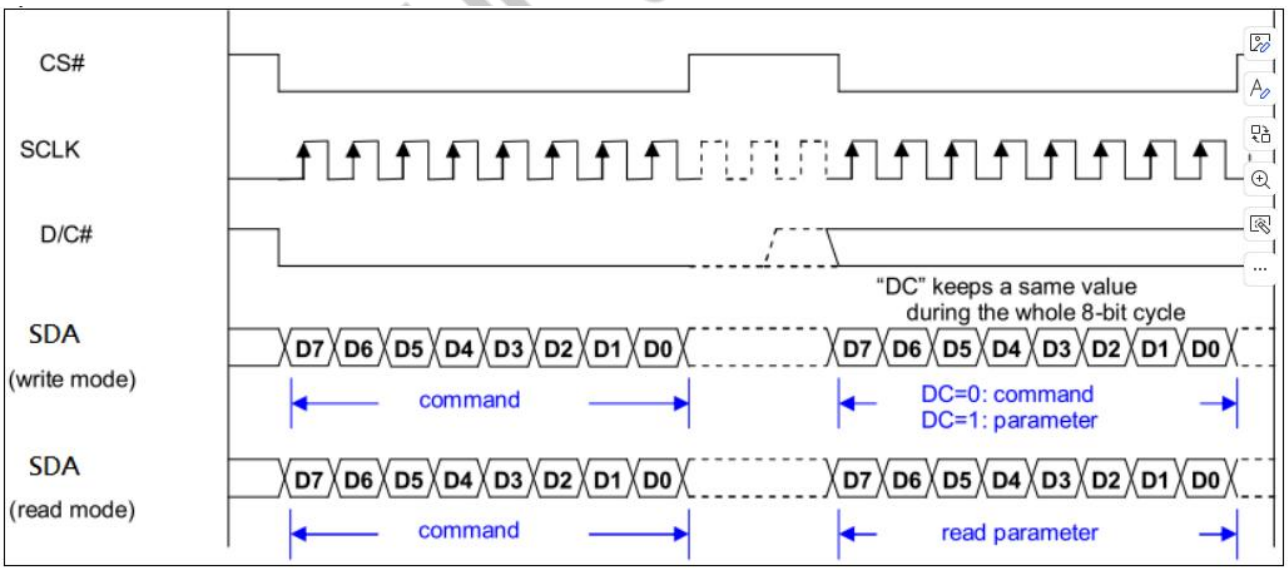


Figure 6-1: Write procedure in 4-wire Serial Peripheral Interface mode

6-3-1-3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDA and CS#.
In 3-wire SPI mode, the pin D/C# can be connected to an external ground.
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 6-3: Control pins of 3-wire Serial Peripheral Interface

Note 6-6: ↑stands for rising edge of signal

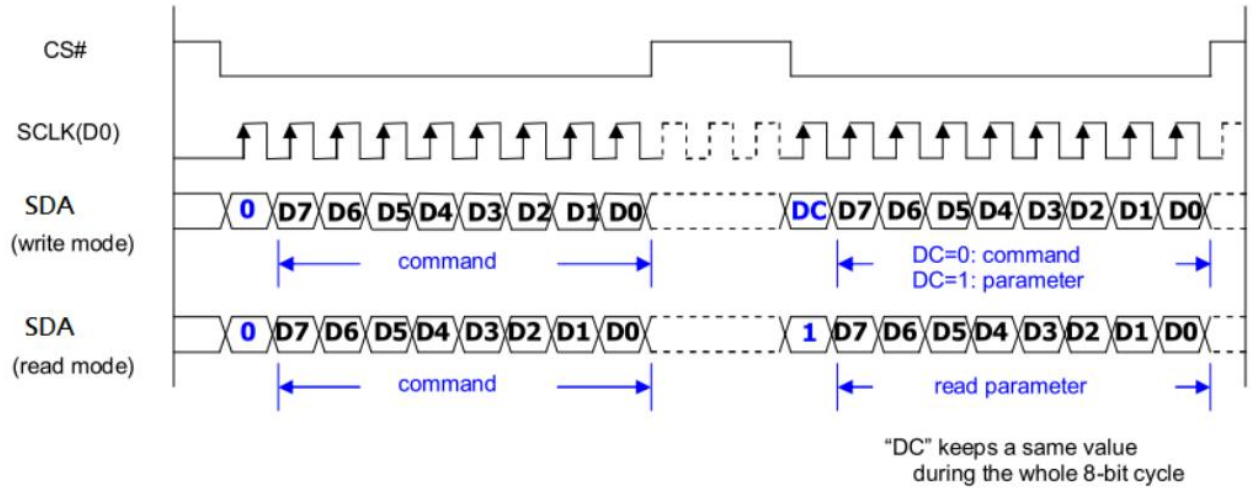
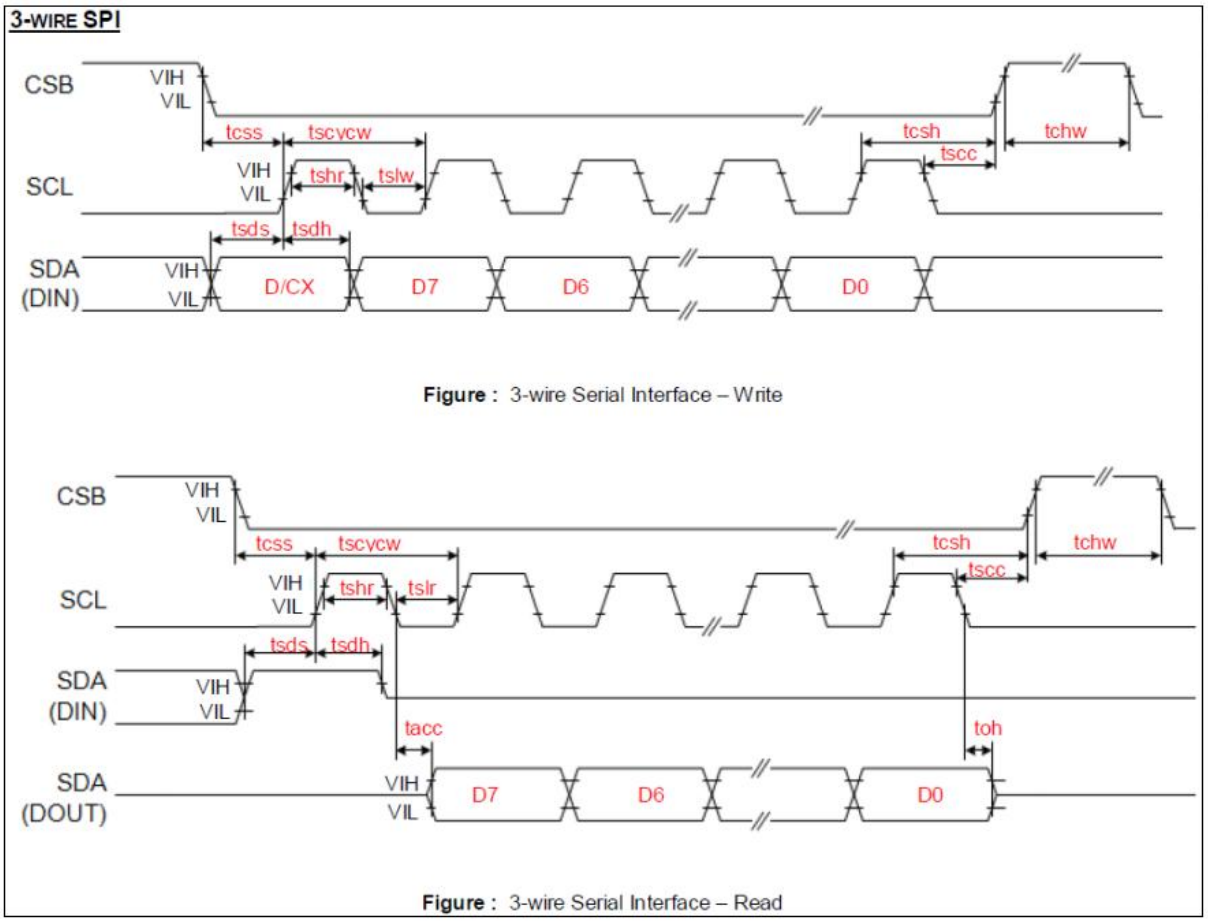


Figure 6-2: Write procedure in 3-wire Serial Peripheral Interface mode

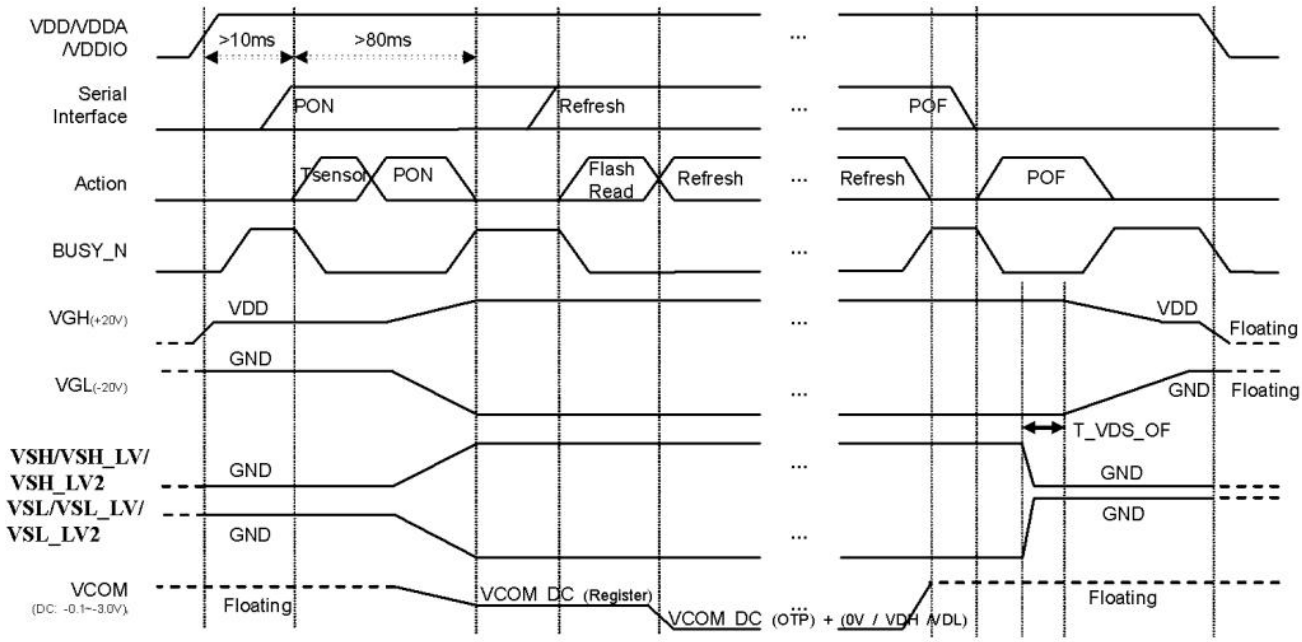
6-3-2 Timing Characteristics of Series Interface



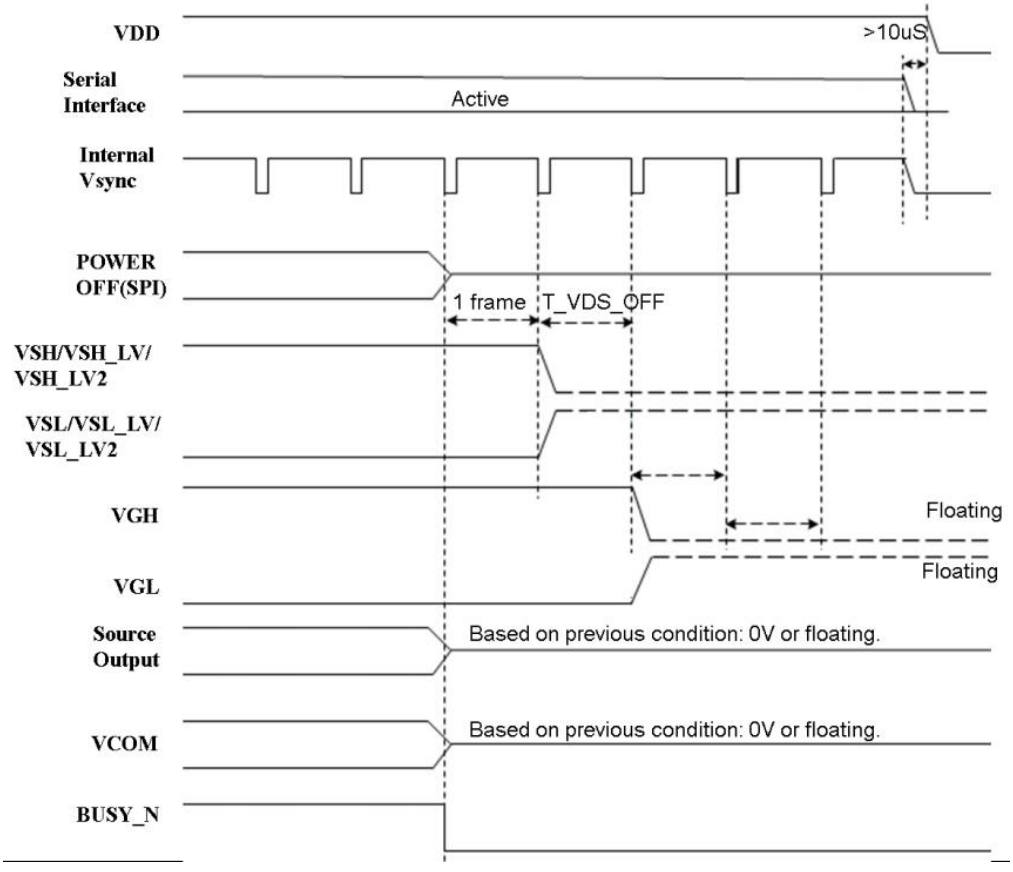
Symbol	Signal		Min.	Typ.	Max.	Unit
SERIAL COMMUNICATION						
tCSS	CSB	Chip select setup time	60			ns
tCSH		Chip select hold time	65			ns
tSCC		Chip deselect setup time	20			ns
tCHW		Chip deselect setup time	40			ns
tSCYCW	SCL	Serial clock cycle (Write)	50			ns
tSHW		SCL “H” pulse width (Write)	25			ns
tSLW		SCL “L” pulse width (Write)	25			ns
tSCYCR		Serial clock cycle (Read)	600			ns
tSHR		SCL “H” pulse width (Read)	150			ns
tSLR		SCL “L” pulse width (Read)	400			ns
tSDS	SDA (DIN) (DOUT)	Data setup time	30			ns
tSDH		Data hold time	30			ns
tACC		Access time			200	ns
tOH		Output disable time	15			ns

7. POWER CHARACTERISTICS

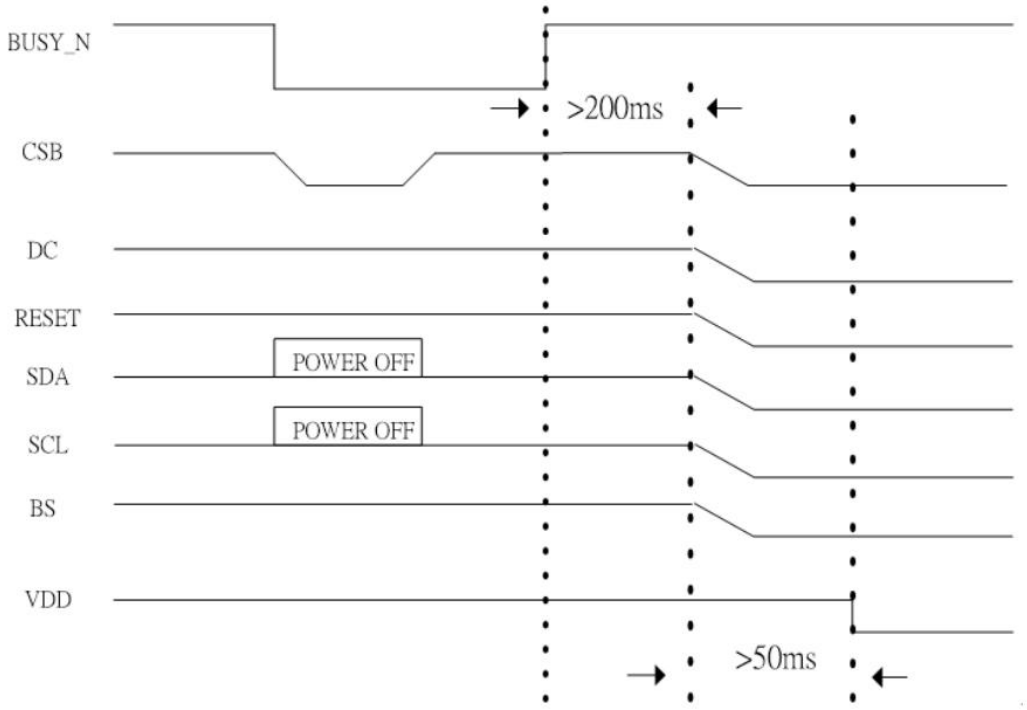
Power ON Sequence



Power OFF Sequence

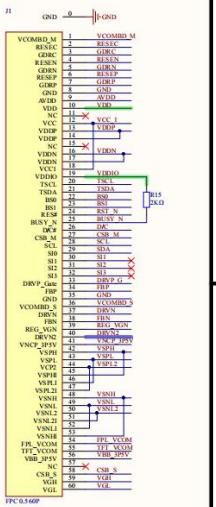


External GPIO Power On/Off Sequence

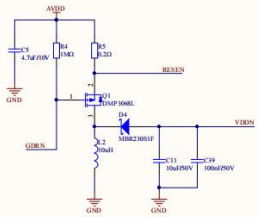


8. REFERENCE CIRCUIT

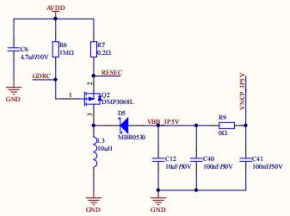
EPD FPC



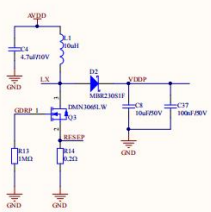
VDDN



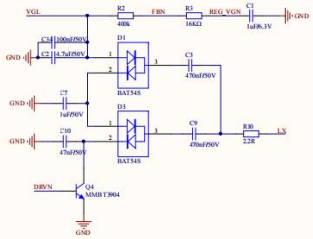
TFT_VCOM Power



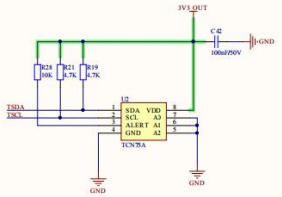
VDDP



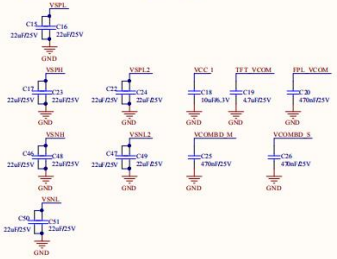
VGL(VGN)



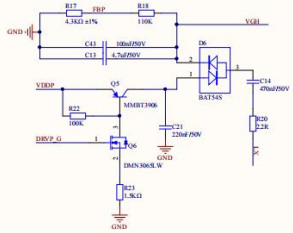
TCN75A



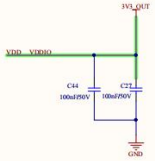
Capacitive Coupling



VGH(VGP)



Power



SPI Mode Selection

Type	BS1	BS0	SPI mode
1	0	0	4-wire SPI
2	0	1	3-wire SPI
3	1	0	Standard 4-wire SPI/Dual SPI/Quad SPI
4	1	1	

9. HANDLING, SAFETY, AND ENVIRONMENT REQUIREMENS AND REMARK

WARNING

The display may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION

(1) The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
(2) Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
(3) IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions

(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because he former generates corrosive gas of attacking the PS at high temperature and the latter cause's circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

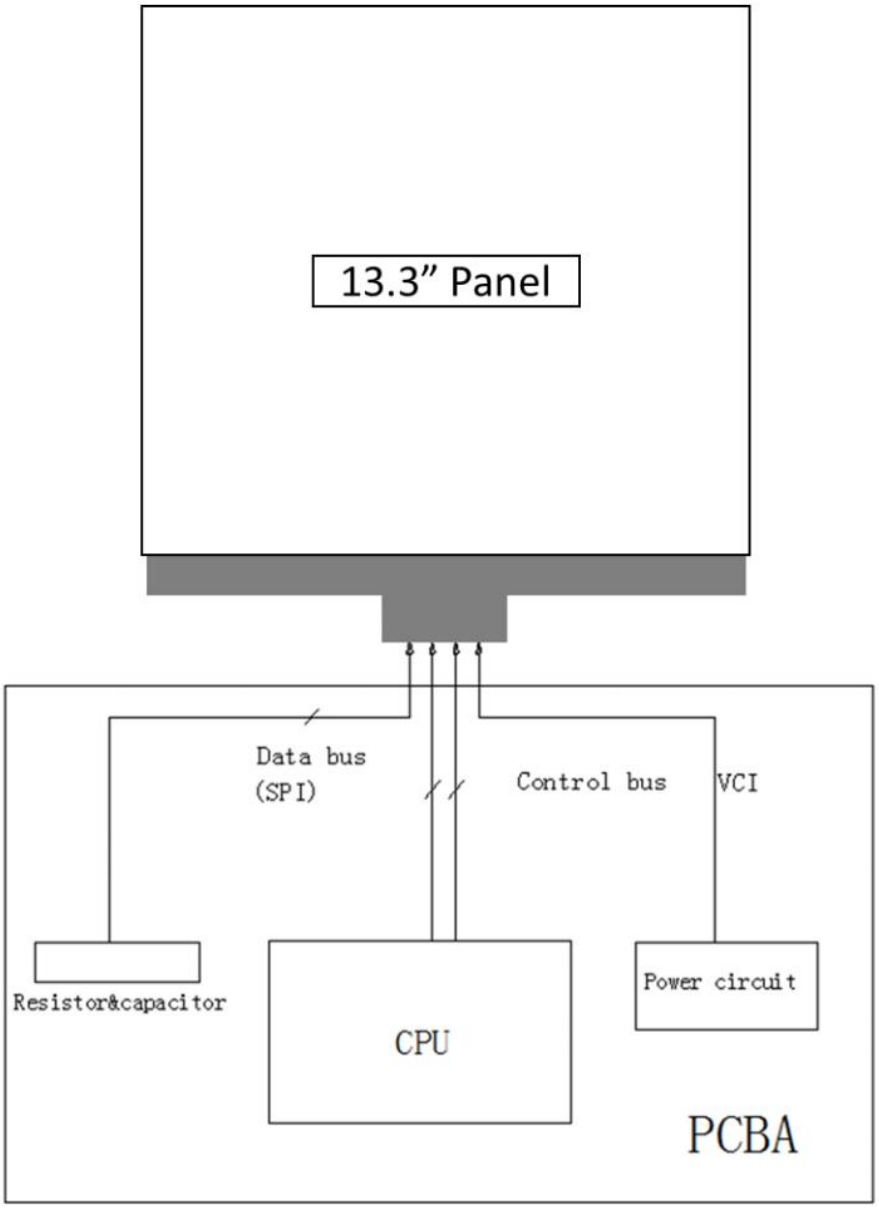
Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other condition these are stress ratings only and operation of the device at these or at any other condition to limiting values for extended periods may affect device reliability.

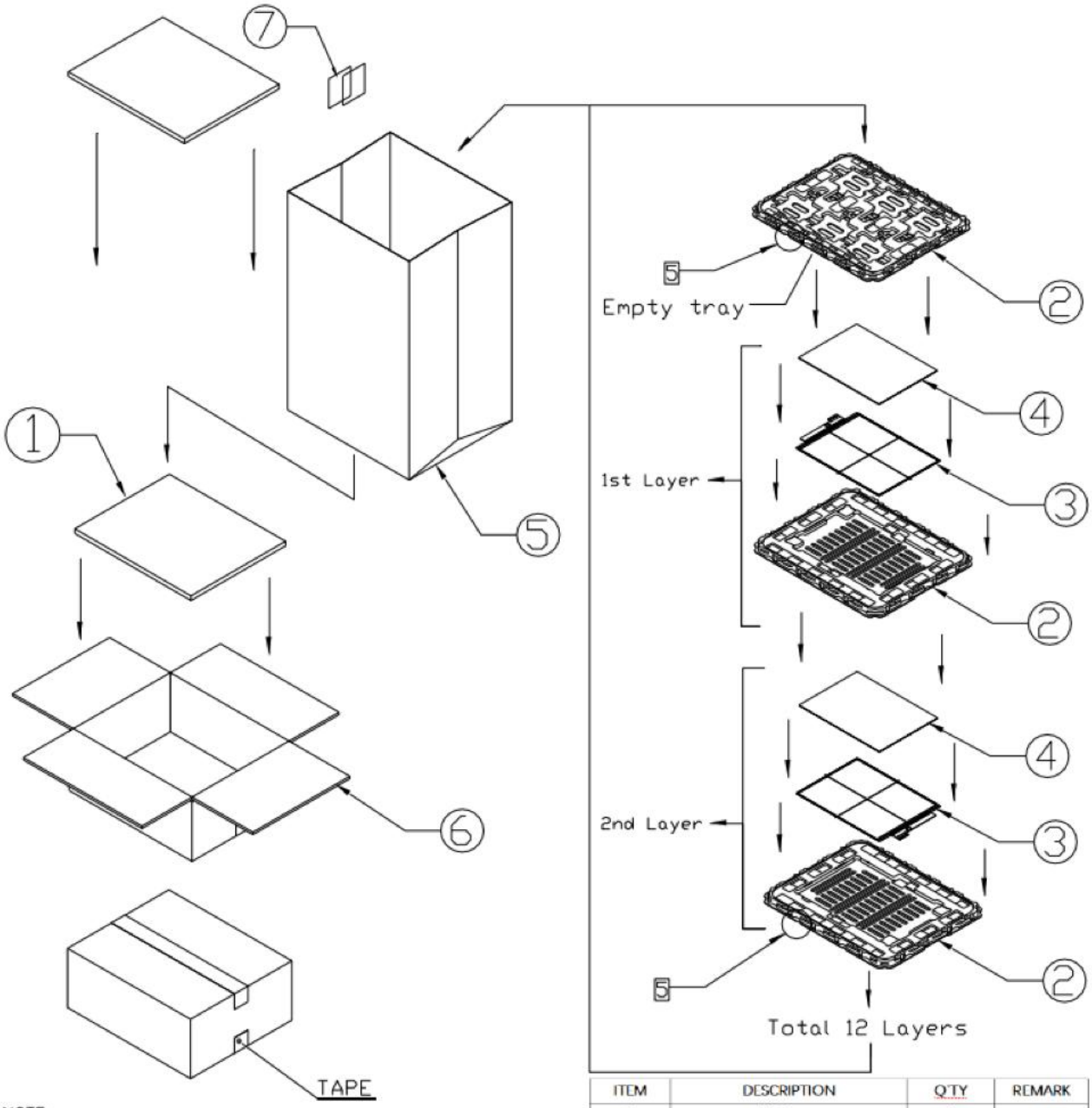
Application information

Where application information is given, it is advisory and does not form part of the specification.

10. BLOCK DIAGRAM



11. PACKING DRAWING



NOTE:
1. ONE LAYER INCLUDE:
   1 PCS MODULE & 1 PIECE OF TRAY.
2. Q'TY: 12 PCS PANEL/CARTON.
3. DIMENSION: 455*375*190mm.
4. N.W.:x.xKG G.W.:x.xKG
5. Make sure tray stacked with 180° rotation,we can check this by tray's half circles from lateral side view.

ITEM	DESCRIPTION	Q'TY	REMARK
1	EPE Foam	2	
2	Tray	13	Antistatic
3	13.3inch e-Paper (E)	12	
4	EPE cushion sheet	12	Antistatic
5	Folded bag 450×380×580mm	1	Antistatic
6	Carton internal	1	
7	30g desiccant	2	