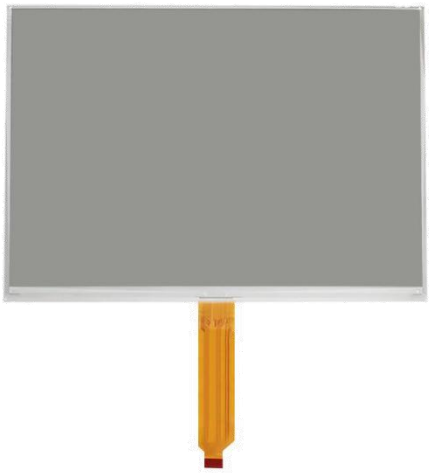
# 13.3inch e-Paper (K)

# User Manual

# Revision History

| Version | Content | Date | Producer |
|---|---|---|---|
| 1.0 | Revision 1.0 | 2023/07/03 | |
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# Contents

# 1. OVERVIEW

13.3 e-Paper (K) is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display image at 1-bit white and black full display capabilities. The 13.3inch active area contains 960x680 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

# 2. FEATURES

- ✧ 960×680 pixels display
- ✧ High contrast High reflectance
- ✧ Ultra wide viewing angle Ultra low power consumption
- ✧ Pure reflective mode
- ✧ Bi-stable display
- ✧ Commercial temperature range
- ✧ Landscape portrait modes
- ✧ Hard-coat antiglare display surface
- ✧ Ultra Low current deep sleep mode
- ✧ On-chip display RAM
- ✧ Waveform can stored in On-chip OTP or written by MCU
- ✧ Serial peripheral interface available
- ✧ On-chip oscillator
- ✧ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ✧ $I^2C$ signal master interface to read external temperature sensor
- ✧ Built-in temperature sensor

# 3. MECHANICAL SPECIFICATION

| Parameter | Specification | Unit | Remark |
|---|---|---|---|
| Screen Size | 13.3 | Inch | |
| Display Resolution | 960(H) x 680(V) | Pixel | DPI:88 |
| Active Area | 275.52 x 195.16 | mm | |
| Pixel Pitch | 0.287 x 0.287 | mm | |
| Pixel Configuration | Rectangle | | |
| Outline Dimension | 286.32(H) x 212.26 (V) x 1.20(D) | mm | |
| Weight | 106.7±0.5 | g | |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| KS | Back State L*value | | - | 18 | 20 | | 3-1 |
| | Back Ghosting ΔL | | - | 1 | - | | 3-1 |
| WS | White state L*value | | 66 | 67 | - | | 3-1 |
| | White Ghosting ΔL | | - | 1 | - | | 3-1 |
| R | White Reflectivity | White | 30 | 34 | - | % | 3-1 |
| CR | Contrast Ratio | Indoor | 15:1 | 20:1 | - | | 3-1<br>3-2 |
| GN | 2 Grey Level | - | - | - | - | | |
| Life | | Temp:23±3℃<br>Humidity: 55±10%RH | | 5 years | - | | 3-3 |

**Notes:**

**3-1. Luminance meter: Eye-One Pro Spectrophotometer.**

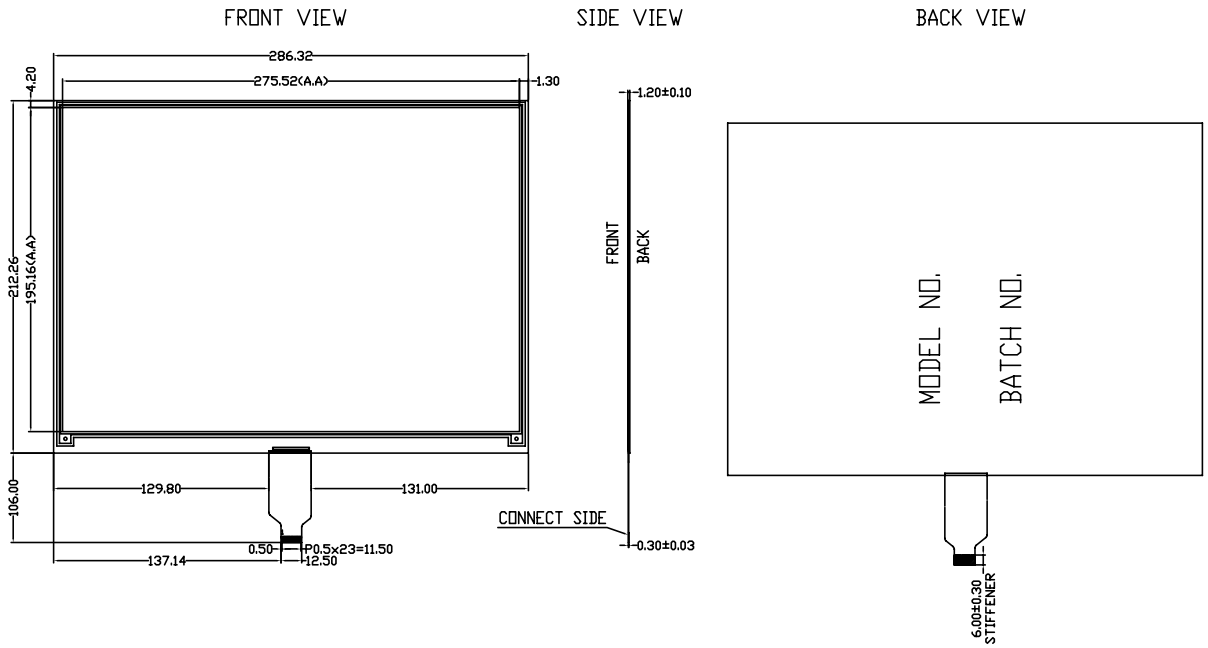
**3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.**

**3-3. When the product is stored. The display screen should be kept white and face up.**

# 4. MECHANICAL DRAWING OF EPD MODULE

Confirmation:

| | | |
|---|---|---|
| 2020-03-04 | A | FIRST ISSUE |




NOTE

1 DISPLAY MODULE 13.3″ ARRAY FOR EPD 2

DRIVER IC:SSD1677

3 RESOLUTION: 680gateX960source

4 PIXEL SIZE:0.287mmX0.287mm

RoHS

WAVESHARE ELECTRONICS

| | | | |
|---|---|---|---|
| TOLERANCE UNMARKED | TITLE<br>EPD | PROJECT<br>13.3" e-Paper (K) | UNIT:<br>mm |
| ANGLES±5°<br>.X=±0.4mm<br>.XX=±0.20mm<br>.XXX=±0.20mm | REV:<br>A | 3RD ANGLE | DATE:<br>22.03.04 |

# 5. INPUT/OUTPUT PIN ASSIGNMENT

**I = Input Pin, O = Output Pin, I/O = Bidirectional Pin (Input/output), P = Power Pin, C = Capacitor Pin.**

| NO. | Name | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | NC | | Do not connect with other NPC pins | Keep Open |
| 2 | GDR | O | N-Channel MOSFET Gate Drive Control | |
| 3 | RESE | I | Current Sense Input for the Control Loop | |
| 4 | NC | NC | Do not connect with other NC pins | Keep Open |
| 5 | VSH | C | Positive Source driving voltage | |
| 6 | TSCL | O | I2C Interface to digital temperature sensor Clock pin | Note 5-6 |
| 7 | TSDA | I/O | I2C Interface to digital temperature sensor Data pin | Note 5-6 |
| 8 | BS1 | I | Bus Interface selection pin | Note 5-5 |
| 9 | BUSY | O | Busy state output pin | Note 5-4 |
| 10 | RES# | I | Reset signal input, Active Low | Note 5-3 |
| 11 | D/C# | I | Data/Command control pin | Note 5-2 |
| 12 | CS# | I | Chip select output pin | Note 5-1 |
| 13 | SCL | I | Serial Clock pin (SPI) | |
| 14 | SDA | I/O | Serial Data pin (SPI) | |
| 15 | VDDIO | P | Power supply for interface logic pins.<br>It should be connected with VCI. | |
| 16 | VCI | P | Power supply for the chip | |
| 17 | VSS | P | Ground | |
| 18 | VDD | C | Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS. | |
| 19 | VPP | P | FOR TEST | Keep Open |
| 20 | VSH1 | C | Positive Source driving voltage | |
| 21 | VGH | C | Power Supply pin for Positive Gate driving voltage and VSH1 | |
| 22 | VSL | C | Negative Source driving voltage | |
| 23 | VGL | C | Power Supply pin for Negative Gate driving voltage VCOM and VSL | |
| 24 | VCOM | C | VCOM driving voltage | |

**Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.**

**Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.**

**Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.**

**Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform-Communicating with digital temperature sensor.**

**Note 5-5: Bus interface selection pin.**

**Note 5-6: The pin connects to the VSS if there is no external temperature sensor.**

| BS1 State | MCU Interface |
|---|---|
| L | 4-lines serial peripheral interface(SPI) - 8 bits SPI |
| H | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

# 6. COMMAND TABLE

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output Control</td><td>Gate setting<br>Set A[9:0]=2A7h[POR] 680MUX<br>Set B[2:0]=000[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving voltage control</td><td rowspan="2">Set Gate Driving voltage A[4:0] = 17h[POR], VGH at 20V[POR]<br>VGH setting from 12V to 20V</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Source Driving voltage control</td><td rowspan="4">Set Source Driving voltage<br>A[7:0] = 41h[POR], VSH1 at 15V<br>B[7:0]=A8h[POR], VSH2 at 5.0V<br>C[7:0]=32h[POR], VSL1 at -15V</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep mode</td><td rowspan="2">Deep Sleep mode Control<br><table><tr><td>A[1:0]:</td><td>Description</td></tr><tr><td>00</td><td>Normal Mode [POR]</td></tr><tr><td>11</td><td>Enter Deep Sleep Mode</td></tr></table>After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>11</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Data Entry mode setting</td><td rowspan="2">Define data entry sequence<br>A[1:0]=ID[1:0] Address automatic increment / decrement setting<br>The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | 00 –Y decrement, X decrement,<br>01 –Y decrement, X increment,<br>10 –Y increment, X decrement,<br>11 –Y increment, X increment [POR] A[2] = AM<br>Set the direction in which the address<br>counter is updated automatically after data are written to the RAM.<br>AM=0, the address counter is updated in the X direction. [POR]<br>AM=1, the address counter is updated in the Y direction. |
| 0 | 0 | 12 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | SWRESET | It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode.<br>During operation, BUSY pad will output high.<br>Note: RAM are affected by this command. |
| 0 | 0 | 18 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | Temperature Sensor Control | Temperature Sensor Selection<br>A[7:0]=48h [POR], external temperature sensor<br>A[7:0]=80h [POR], internal temperature sensor |
| 0 | 1 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 0 | 1A | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | Temperature Sensor Control (Write to temperature | Write to temperature register.<br>A[11:0]=7FFh[POR] |
| 0 | 1 | | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | | |
| 0 | 1 | | A3 | A2 | A1 | A0 | 0 | 0 | 0 | 0 | | |

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>register)</td><td></td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Active Display Update Sequence<br>The Display Update Sequence Option is located at R22h.<br>User should not interrupt this operation to avoid corruption of panel images</td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Display Update Control 1</td><td rowspan="2">RAM content option for Display Update<br>A[7:0]=00H[POR]<br>A[7:4] Red RAM option<br><table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table><br>A[3:0] BW RAM option<br><table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:<br>Enable the stage or Master Activation<br><table><tr><td>Setting for LUT from MCU</td><td></td></tr><tr><td>Enable Clock Signal,<br>Then Enable Analog<br>Then PATTERN DISPLAY<br>Then Disable Analog<br>Then Disable OSC</td><td>C7</td></tr></table><br>Setting for LUT from</td></tr>
<tr><td></td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

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<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>OTP according to external Temperature Sensor operation<table><tr><td>Then Enable Analog Then Load LUT</td><td>90</td></tr><tr><td>Enable Analog Then PATTERN DISPLAY Then Disable Analog Then Disable OSC</td><td>47</td></tr></table></td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM (BW)</td><td>After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0</td></tr>
<tr><td>0</td><td>0</td><td>26</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Write RAM (RED)</td><td>After this command, data entries will be written into the 2 RAM until another command is written. Address pointers will advance accordingly. For RED pixel: Content of write RAM(RED)=1 For White/Black pixel: Content of write RAM(RED)=0</td></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Write VCOM register</td><td rowspan="2">Set A[7:0]=50h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>2D</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="3">OTP Register Read</td><td rowspan="3">Read Register stored in OTP:<br>1. A[7:0]~B[7:0]: VCOM</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
</table>

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | | Information |
| 1 | 1 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | 2. C[7:0]~G[7:0]: Display mode |
| 1 | 1 | | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 | | 3. H[7:0]~K[7:0]: Waveform Version [4bytes] |
| 1 | 1 | | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | | |
| 1 | 1 | | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | | |
| 1 | 1 | | H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 | | |
| 1 | 1 | | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 | | |
| 1 | 1 | | J7 | J6 | J5 | J4 | J3 | J2 | J1 | J0 | | |
| 1 | 1 | | K7 | K6 | K5 | K4 | K3 | K2 | K1 | K0 | | |
| 0 | 0 | 2F | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | Status Bit Read | Read IC status Bit [POR 0x21]<br>A[5]: HV relay detection flag [POR=1]<br>0: Ready<br>1: Not ready<br>A[4]: VCI detection flag [POR=0]<br>0: Normal<br>1: VCI lower than the Detect level<br>A[3]: [POR=0]<br>0: Normal<br>1: BUSY<br>A[1:0]: Chip ID [POR=0]<br>Remark:<br>A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively. |
| 1 | 1 | | 0 | 0 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 0 | 32 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Write LUT register | Write LUT register from MCU interface [105 bytes] |
| 0 | 1 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 1 | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| 0 | 1 | | : | : | : | : | : | : | : | : | | |
| 0 | 1 | | : | : | : | : | : | : | : | : | | |
| 0 | 1 | | : | : | : | : | : | : | : | : | | |
| 0 | 0 | 3A | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | Reserved | Reserved |
| 0 | 0 | 3B | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | Reserved | Reserved |
| 0 | 0 | 3C | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | Border Waveform Control | Select boarder waveform for VBD<br>A[7:0]=C0h [POR], set |
| 0 | 1 | | A7 | A6 | A5 | A4 | 0 | 0 | A1 | A0 | | |

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>VBD as HIZ<br>A[7:6] Select VBD option<table><tr><td>A[7:6]</td><td>Select VBD as</td></tr><tr><td>00</td><td>GS Transition Define A[1:0]</td></tr><tr><td>01</td><td>Fix Level Define A[5:4]</td></tr><tr><td>10</td><td>VCOM</td></tr><tr><td>11[POR]</td><td>HIZ</td></tr></table>A[5:4] Fix Level Setting for VBD<table><tr><td>A[5:4]</td><td>VBD level</td></tr><tr><td>00[POR]</td><td>VSS</td></tr><tr><td>01</td><td>VSH1</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11</td><td>VSH2</td></tr></table>A[1:0] BW Transition setting for VBD<table><tr><td>A[1:0]</td><td>VBD Transition</td></tr><tr><td>00[POR]</td><td>LUT0</td></tr><tr><td>01</td><td>LUT1</td></tr><tr><td>10</td><td>LUT2</td></tr><tr><td>11</td><td>LUT3</td></tr></table></td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="5">Set RAM X-address Start/End position</td><td rowspan="5">Specify the start/end positions of the window address in the X direction by an address unit<br>A[9:0]: XSA[9:0], X Start, POR=000h<br>B[9:0]: XEA[9:0], X End, POR=3BFh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A9</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B9</td><td>B8</td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="5">Set RAM Y-address Start/End position</td><td rowspan="5">Specify the start/end positions of the window address in the Y direction by an address unit<br>A[9:0]: YSA[9:0], Y Start,</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A9</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B8</td></tr>
</table>

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | POR=000h<br>B[9:0]: YEA[9:0], Y End, POR=2A7h |
| 0 | 0 | 4E | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | Set RAM X-address counter | Make initial settings for the RAM X address in the address counter (AC)<br>A[9:0]: 000h[POR] |
| 0 | 1 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 1 | | - | - | - | - | - | - | A9 | A8 | | |
| 0 | 0 | 4F | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Set RAM Y-address counter | Make initial settings for the RAM Y address in the address counter (AC)<br>A[9:0]: 000h[POR] |
| 0 | 1 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 1 | | - | - | - | - | - | - | A9 | A8 | | |
| 0 | 1 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |

# 7. ELECTRICAL CHARACTERISTICS

## 7.1 ABSOLUTE MAXIMUM RATING

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Logic supply voltage | VCI | -0.3 to +6.0 | V |
| Logic Input voltage | VIN | -0.3 to VCI +0.3 | V |
| Operating Temp range | TOPR | 0 to +50 | ºC |
| Storage Temp range | TSTG | -25 to+70 | ºC |
| Optimal Storage Temp | TSTGo | 23±3 | ºC |
| Optimal Storage Humidity | HSTGo | 55±10 | %RH |

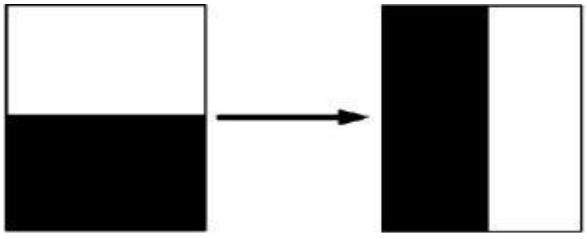
**Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.**

## 7.2 PANEL DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Single ground | $V_{SS}$ | - | | - | 0 | - | V |
| Logic supply voltage | $V_{CI}$ | - | VCI | 2.2 | 3.0 | 3.3 | V |
| Core logic voltage | $V_{DD}$ | | VDD | 1.7 | 1.8 | 1.9 | V |
| High level input voltage | $V_{IH}$ | - | - | $0.8V_{CI}$ | - | - | V |
| Low level input voltage | $V_{IL}$ | - | - | - | - | $0.2V_{CI}$ | V |
| High level output voltage | $V_{OH}$ | IOH = - 100uA | - | $0.9V_{CI}$ | - | - | V |
| Low level output voltage | $V_{OL}$ | IOL = 100uA | - | - | - | $0.1V_{CI}$ | V |
| Typical power | $P_{TYP}$ | $V_{CI}$ =3.0V | - | - | 66 | - | mW |
| Deep sleep mode | $P_{STPY}$ | $V_{CI}$ =3.0V | - | - | 0.009 | - | mW |
| Typical operating current | $Iopr\_V_{CI}$ | $V_{CI}$ =3.0V | - | - | 22 | - | mA |
| Image update time | - | 23 ºC | - | - | 4 | - | sec |
| Typical peak current | $Iopr\_V_{CI}$ | 2.2~3.7v | | | 100 | 160 | mA |
| Sleep mode current | $Islp\_V_{CI}$ | DC/DC off, No clock No input load Ram data retain | - | - | 20 | - | uA |
| Deep sleep mode current | $Idslp\_V_{CI}$ | DC/DC off, No clock No input load Ram data not retain | - | - | 3 | 5 | uA |

**Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical.**



**2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.**

**3. The listed electrical characteristics are only guaranteed under the controller & waveform provided by Waveshare.**

**4. Electrical measurement: Tektronix oscilloscope - MDO3024, Tektronix current probe –TCP0030A.**

## 7.3 PANEL DC CHARACTERISTICS (DRIVER IC INTERNAL REGULATORS)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR=23°C.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VCOM output voltage | VCOM | - | VCOM | - | TBD | - | V |
| Positive Source output voltage | $V_{SH}$ | - | $S_0$~$S_{959}$ | +14.8 | +15 | +15.2 | V |
| Negative Source output voltage | $V_{SL}$ | - | $S_0$~$S_{959}$ | -15.2 | -15 | -14.8 | V |
| Positive gate output voltage | $V_{gh}$ | - | $G_0$~$G_{679}$ | +19.5 | +20 | +20.5 | V |
| Negative gate output voltage | $V_{gl}$ | - | $G_0$~$G_{679}$ | -20.5 | -20 | -19.5 | V |

## 7.4 MCU INTERFACE

### 7.4.1 MCU INTERFACE SELECTION

The pin assignment at different interface mode is summarized in Table 7-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

| Pin Name | Data/Command Interface | | Control Signal | | |
|---|---|---|---|---|---|
| Bus interface | SDA | SCL | CS# | D/C# | RES# |
| BS1=L 4-wire SPI | SDA | SCL | CS# | D/C# | RES# |
| BS1=H 3-wire SPI | SDA | SCL | CS# | D/C# | RES# |

### 7.4.2 MCU SERIAL INTERFACE (4-WIRE SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

| Function | CS# | D/C# | SCL |
|---|---|---|---|
| Write command | L | L | ↑ |
| Write data | L | H | ↑ |

**Note: ↑ stands for rising edge of signal.**

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM/Data Byte register or command Byte register according to D/C# pin.

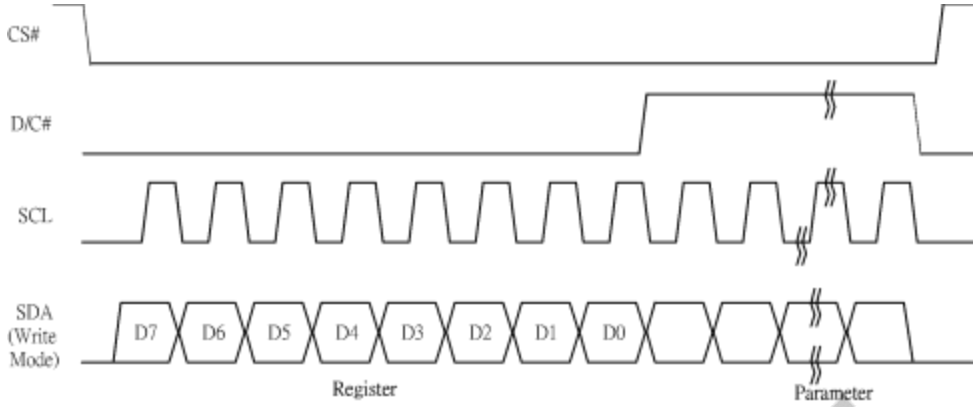



**Figure 7-1: Write procedure in 4-wire SPI mode**

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.

2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.

3. After SCL change to low for the last bit of register, D/C# need to drive to high.

4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.

5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

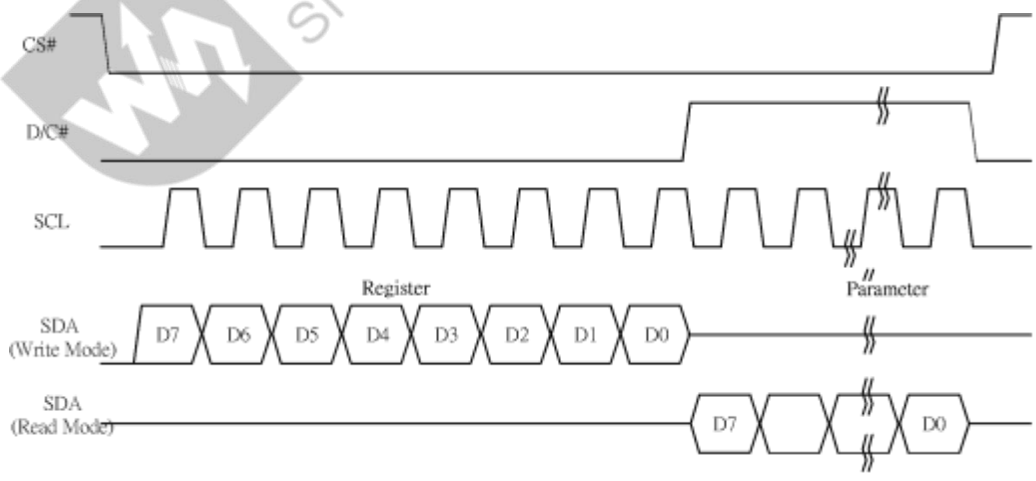



**Figure 7-2: Read procedure in 4-wire SPI mode**

### 7.4.3 MCU SERIAL INTERFACE (3-WIRE SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit=1) or the command register (D/C# bit=0).

| Function | CS# | D/C# | SCL |
|---|---|---|---|
| Write command | L | Tie | ↑ |
| Write data | L | Tie | ↑ |

**Note: ↑ stands for rising edge of signal**

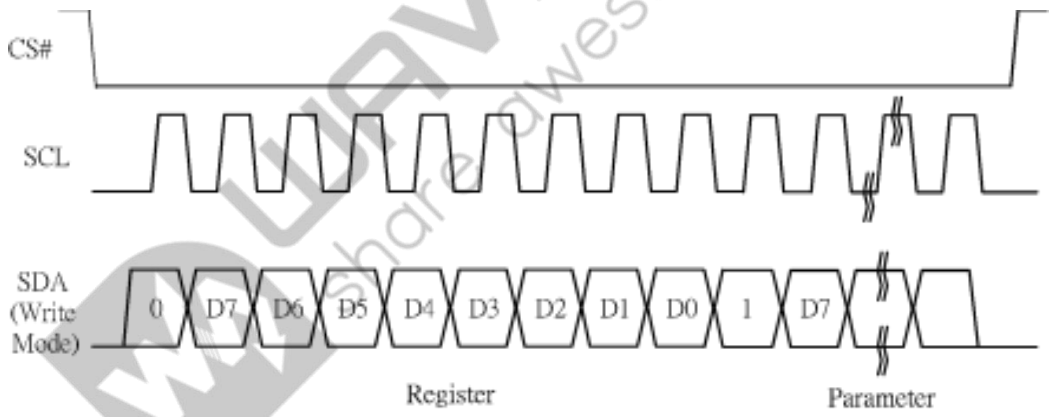



**Figure 7-3: Write procedure in 3-wire SPI mode**

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.

2. D/C=0 is shifted thru SDA with one rising edge of SCL.

3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.

4. D/C=1 is shifted thru SDA with one rising edge of SCL.

5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.

6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

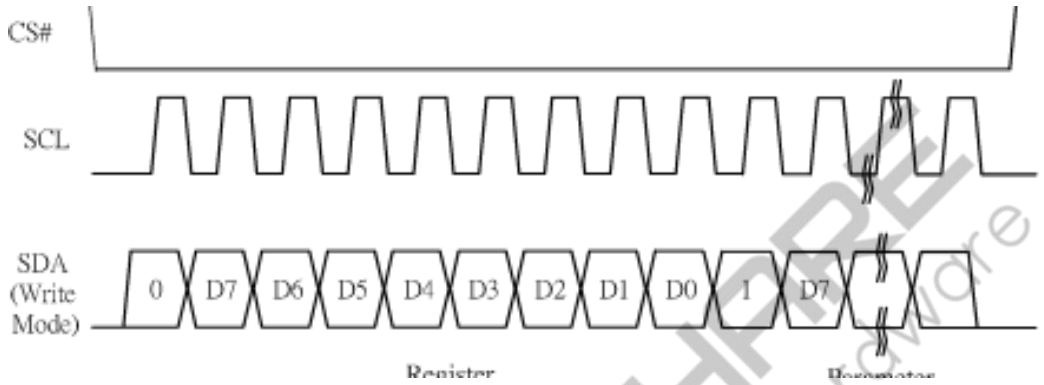
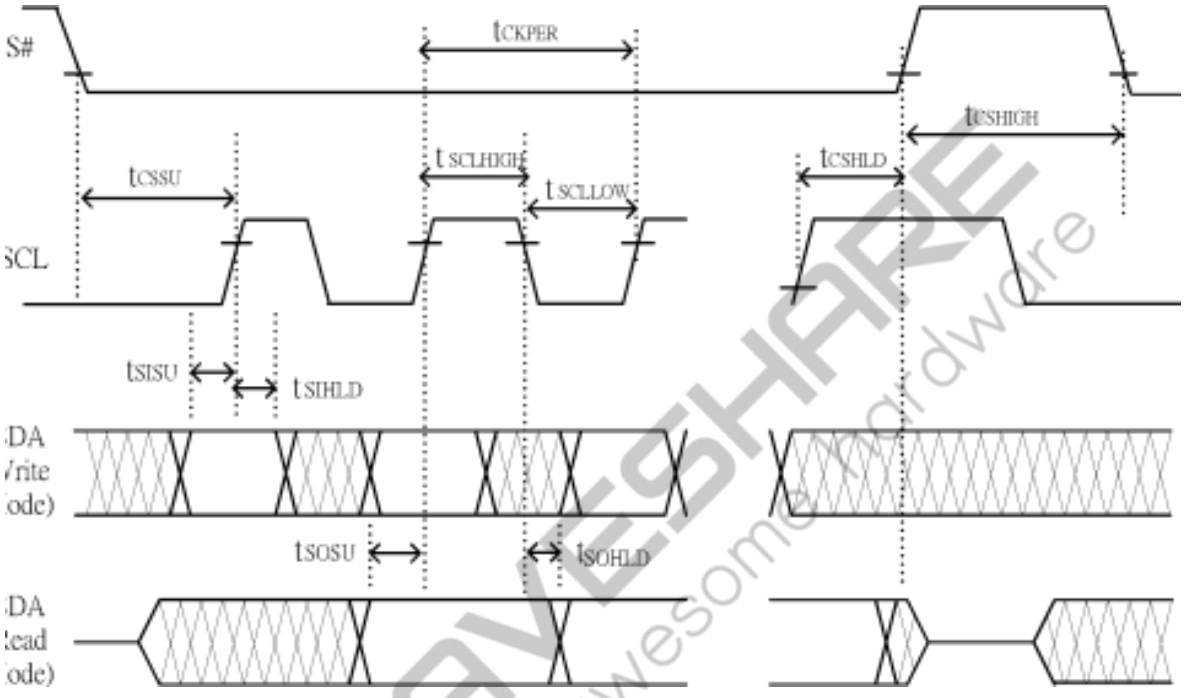



**Figure 7-4: Read procedure in 3-wire SPI mode**

### 7.4.4 INTERFACE TIMING

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.




**Changed diagram**

**Serial Interface Timing Characteristics**

(VCI - VSS = 2.2V to 3.7V, TOPR = 23°C, CL=20pF)

**Write mode**

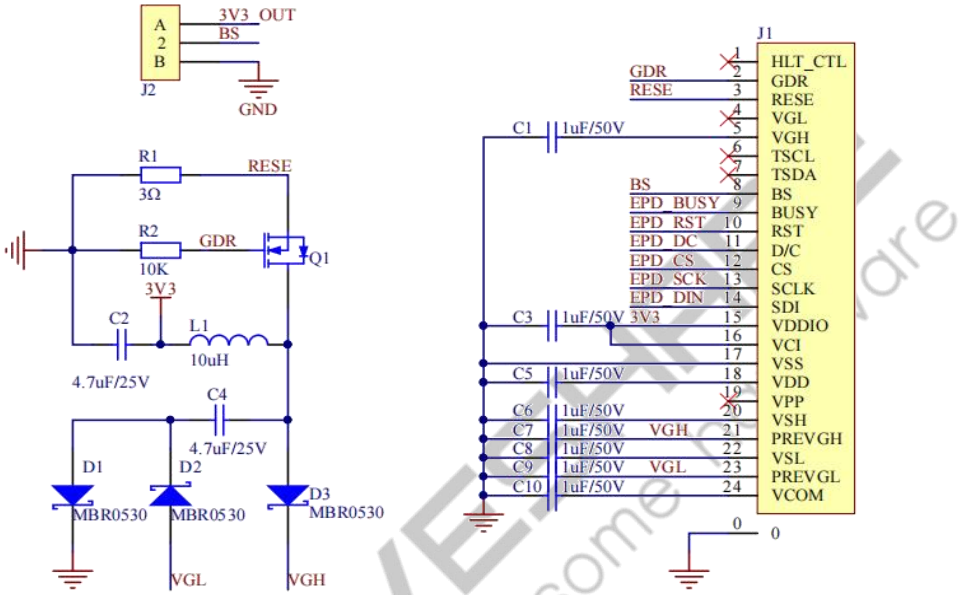
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| fSCL | SCL frequency (Write Mode) | | | 20 | MHZ |
| tCSSU | Time CS# has to be low before the first rising edge of SCLK | 60 | | | ns |
| tCSHLD | Time CS# has to remain low after the last falling edge of SCLK | 65 | | | ns |
| tCSHIGH | Time CS# has to remain high between two transfers | 100 | | | ns |
| tSCLHIGH | Part of the clock period where SCL has to remain high | 25 | | | ns |
| tSCLLOW | Part of the clock period where SCL has to remain low | 25 | | | ns |
| tSISU | Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL | 10 | | | ns |
| tSIHLD | Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL | 40 | | | ns |

**Read mode**

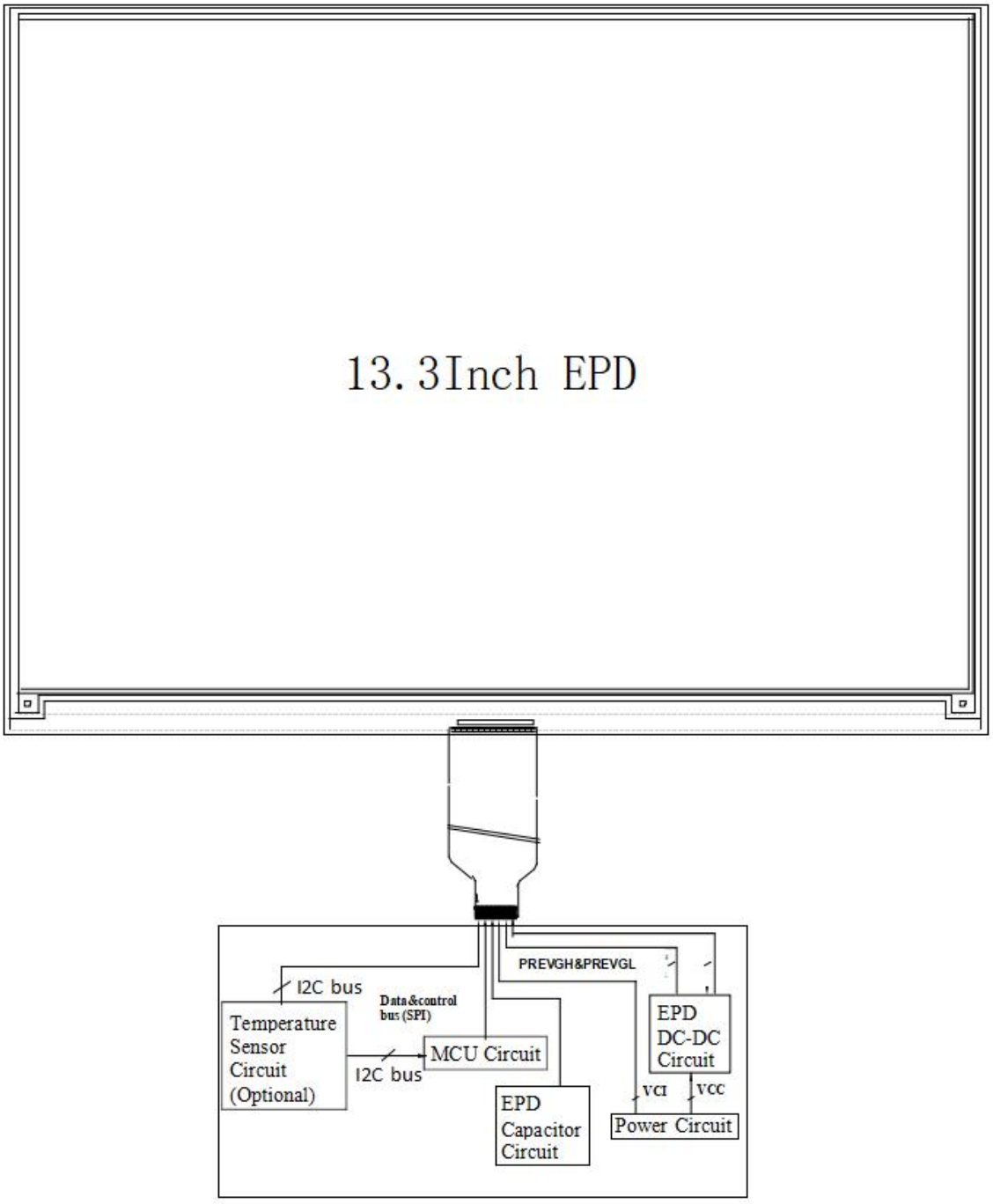
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| fSCL | SCL frequency (Read Mode) | | | 2.5 | MHZ |
| tCSSU | Time CS# has to be low before the first rising edge of SCLK | 100 | | | ns |
| tCSHLD | Time CS# has to remain low after the last falling edge of SCLK | 50 | | | ns |
| tCSHIGH | Time CS# has to remain high between two transfers | 250 | | | ns |
| tSCLHIGH | Part of the clock period where SCL has to remain high | 180 | | | ns |
| tSCLLOW | Part of the clock period where SCL has to remain low | 180 | | | ns |
| tSOSU | Time SI (SDA Read Mode) has to be stable before the next rising edge of SCL | | 50 | | ns |
| tSOHLD | Time SO (SDA Read Mode) has to be stable before the next rising edge of SCL | | 0 | | ns |

## 7.5 REFERENCE CIRCUIT

| BS | VCC | GND |
|---|---|---|
| Interface | 3-line SPI | 4-line SPI |



# 8. BLOCK DIAGRAM



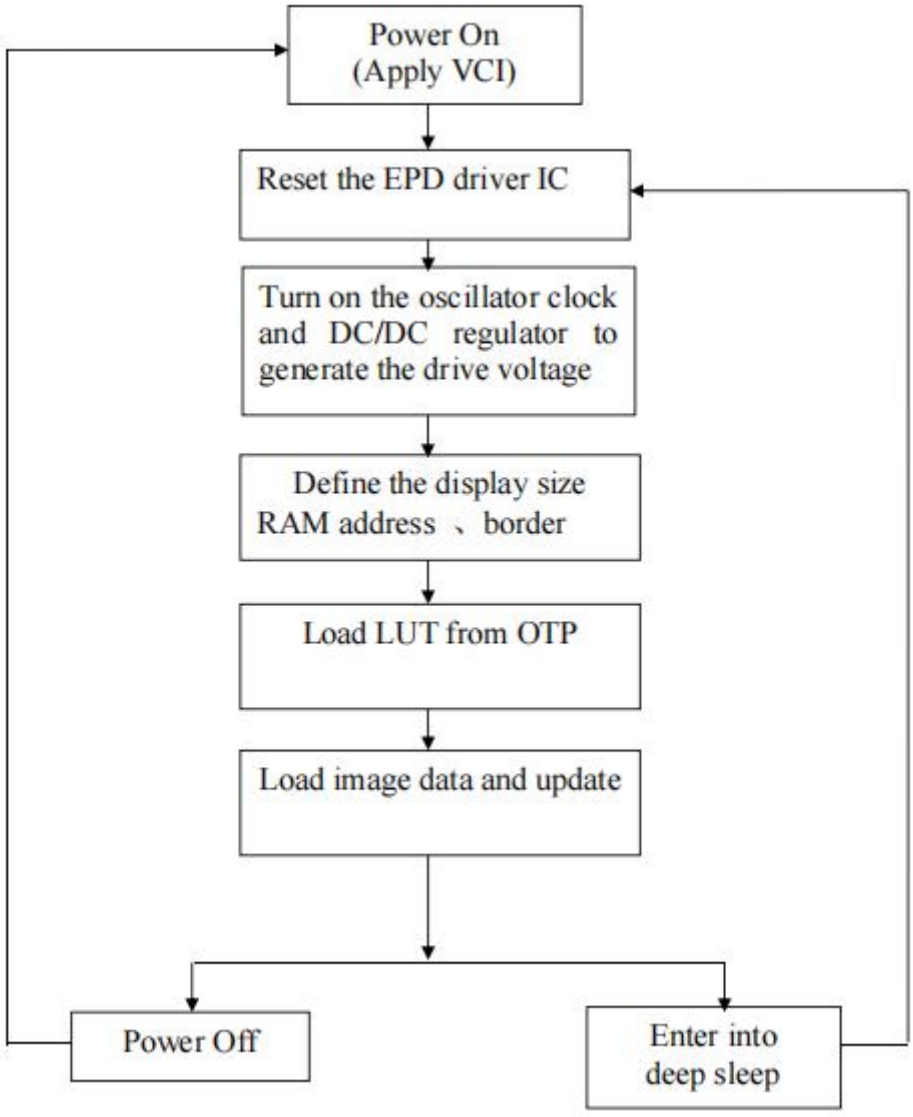
# 9. MATCHED DEVELOPMENT KIT

Our Development Kit designed for SPI e-Paper Display aims to help users to learn how to use e-Paper Display more easily. It can refresh black-white Display, three-color (black, white and red/yellow) e-Paper Display, four-color (black, white, red and yellow) Waveshare's e-Paper Display.

Development Kit consists of the development board and the pinboard. Supported development platforms include Raspberry Pi, STM32, Arduino UNO, etc. For more details, please click to the following link: **https://www.waveshare.com/product/displays.htm**

# 10. TYPICAL OPERATING STATUS

## 10.1 LUT FROM OTP OPERATION FLOW



## 10.2 OTP OPERATION REFERENCE PROGRAM CODE

| ACTION | VALUE/DATA | COMMENT |
|---|---|---|
| POWER ON | | |
| delay | 10ms | |
| PIN CONFIG | | |
| RESE# | low | Hardware reset |
| delay | 200us | |
| RESE# | high | |
| delay | 200us | |
| Read busy pin | | Wait for busy low |
| Command 0x12 | | Software reset |
| Read busy pin | | Wait for busy low |
| LOAD LUT | | |
| Command 0x18 | Data 0x80 | Set built-in temperature sensor |
| Command 0x22 | Data 0xB1 | Load LUT |
| Command 0x20 | | |
| Read busy pin | | Wait for busy low |
| LOAD IMAGE AND UPDATE | | |
| Command 0x24 | 81600bytes | Load BW image (960/8*680) |
| Command 0x22 | Data 0xC7 | Image update |
| Command 0x20 | | |
| Read busy pin | | Wait for busy low |
| Command 0x10 | Data 0x01 | Enter deep sleep mode |
| POWER OFF | | |

# 11. RELIABILITY TEST

| NO | Test items | Test condition |
|---|---|---|
| 1 | Low-Temperature Storage | T = -25°C, 240 h<br>Test in white pattern |
| 2 | High-Temperature Storage | T=+70ºC, RH=40%, 240h<br>Test in white pattern |
| 3 | High-Temperature Operation | T=+50ºC, RH=30%, 240h |
| 4 | Low-Temperature Operation | 0ºC, 240h |
| 5 | High Temperature<br>High Humidity Operation | T=40ºC , RH=90%, 240h |
| 6 | High Temperature<br>High Humidity Storage | T=60ºC , RH=80%, 240h<br>Test in white pattern |
| 6 | Temperature Cycle | 1 cycle: [-25°C 30min]→ [+70 °C 30 min] : 100 cycles Test in white pattern |
| 7 | ESD Gun | Air+/-4KV; Contact +/-2KV<br>Contact +/-2KV (HBM C:100pF; R:1.5k ohm)<br>Contact +/-200V (MM C:2000pF; R:0 ohm)<br>(Naked EPD display, including IC and FPC area) |

**Note：1. Stay white pattern for storage and non-operation test.**

**2. Operation is black →white pattern, the interval is 150s.**

# 12. QUALITY ASSURANCE

## 12.1 ENVIRONMENT

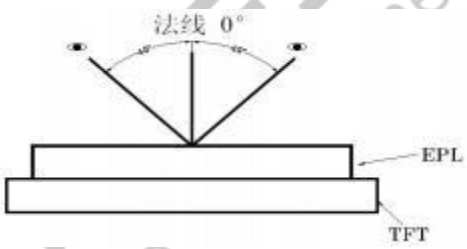
Temperature: 23±3℃

Humidity: 55±10%RH

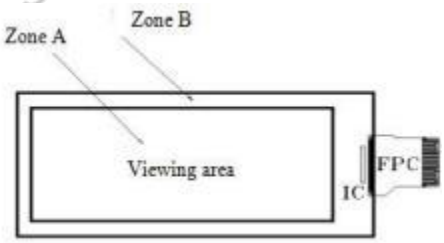
## 12.2 ILLUMINANCE

Brightness:1200～1500LUX; distance:20-30CM; Angle: Relate 45° surround.

## 12.3 INSPECT METHOD



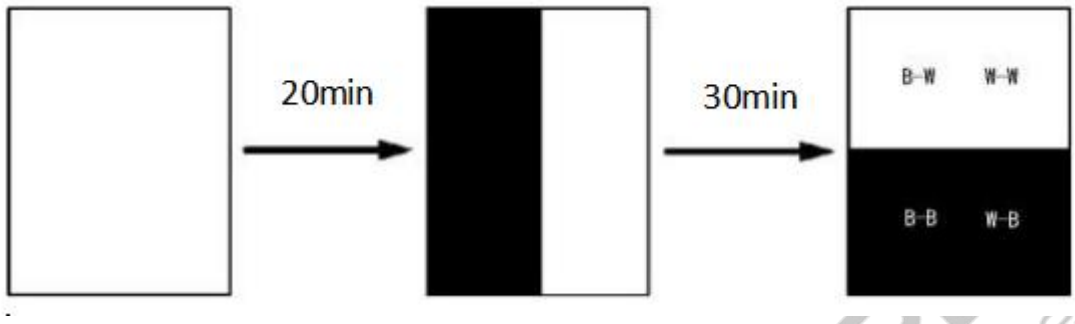

## 12.4 DISPLAY AREA




## 12.5 GHOSTING TEST METHOD

Two-color ghosting is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.

The listed optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.




1) Measurement Instruments: X-rite i1Pro

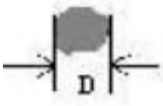
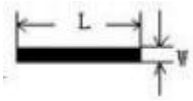
2) Ghosting formula:

W ghosting: ΔL=Max (ΔL(W-W, B-W)) - Min (ΔL(W-W B-W))

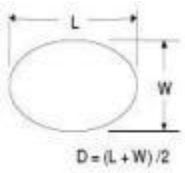
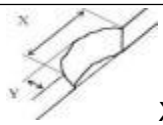
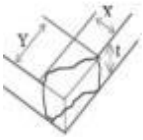
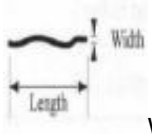
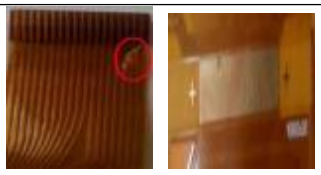
K ghosting: ΔL=Max (ΔL(W-B, B-B)) - Min (ΔL(W-B, B-B))

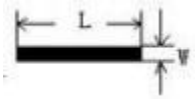
## 12.6 INSPECTION STANDARD

### 12.6.1 ELECTRIC INSPECTION STANDARD

| NO. | Item | Standard | Defect level | Method | Scope |
|---|---|---|---|---|---|
| 1 | Display | Clear display Display complete<br>Display uniform | MA | Visual inspection<br><br>Visual/ Inspection card | Zone A |
| 2 | Black/White spots |  <br>D≤0.3mm, negligible<br>0.3mm<D≤0.5mm, N≤7, Allowed<br>0.5mm<D≤0.6mm, N≤1, Allowed<br>0.6mm<D, Not allow | MI | | |
| 3 | Black/White spots<br>(No switch) |  <br>L ≤1mm, W≤0.15mm negligible<br>1.0mm<L ≤4.0mm<br>0.15mm<W≤0.5mm<br>N≤4 Allow<br>L>4.0mm, W>0.5mm, Not allow | | | |
| 4 | Ghost image | Allowed in switching process | MI | Visual inspection | |
| 5 | Flash dot/Multilateral | Flash points are allowed when switching screens<br>Multilateral colors outside the frame are allowed for fixed screen time | MI | Visual/ Inspection card | Zone A<br>Zone B |
| 6 | Segment display | Selection segment are all displayed, and other segments are not displayed after the selection segment | MA | Visual inspection | Zone A |
| 7 | Short circuit/Circuit break/Abnormal display | Not Allowed | | | |

### 12.6.2 APPEARANCE INSPECTION STANDARD

| NO. | Item | Standard | Defect level | Method | Scope |
|---|---|---|---|---|---|
| 1 | B/W spots/Bubble/Foreign bodies/Dents |  <br>D≤0.3mm, negligible<br>0.3mm<D≤0.5mm, N≤7, Allowed<br>0.5mm<D≤0.6mm, N≤1, Allowed<br>D>0.6mm, Not allow | MI | Visual Inspection | Zone A |
| 2 | Glass crack | Not Allowed | MA | Visual/ Microscope | Zone A<br>Zone B |
| 3 | Dirty | Allowed if can be removed | MI | | Zone A<br>Zone B |
| 4 | Chips/Scratch/Edge crown |  <br>X≤3mm,Y≤0.5mm<br>  <br>2mm≤X or 2mm≤Y Allow<br>  <br>W≤0.1mm, L≤5mm, n≤2 | MI | Visual/ Microscope | Zone A<br>Zone B |
| 5 | TFT Cracks |  <br>Not allow | MA | Visual/ Microscope | Zone A<br>Zone B |
| 6 | Dirty/Foreign body | Allowed if can be removed/allow | MI | Visual/ Microscope | Zone A /Zone B |
| 7 | FPC broken/FPC Oxidation/scratch |  <br>Not allow | MA | Visual/ Microscope | Zone B |

| | | | | | |
|---|---|---|---|---|---|
| 8 | B/W Line |  <br>L ≤1.0mm, W≤0.15mm negligible<br>1mm<L≤4.0mm<br>0.15mm<W≤0.5mm, N≤4 Allow<br>L>4.0mm, W>0.5mm, Not allow | MI | Visual/Ruler | Zone B |
| 9 | TFT edge bulge/TFT chromatic aberration | TFT edge bulge:<br>X≤3mm, Y≤0.3mm; Allowed<br>TFT chromatic aberration; Allowed | MI | Visual/ Microscope | Zone A<br>Zone B |
| 10 | Electrostatic point | D≤0.3mm, negligible<br>0.5mm<D≤0.5mm n≤4 Allow<br>D>0.5mm Not allow (n ≤10 items are allowed within 5mm in diameter) | MI | Visual/ Microscope | Zone A |
| 11 | PCB damaged/Poor welding/Curl | PCB (Circuit area) damaged Not Allow, PCB Poor welding Not Allow<br>PCB Curl≤1% | MI | Visual/Ruler | Zone B |
| 12 | Edge glue height/Edge glue bubble | Edge Adhesives H≤PS surface (Including protect film)<br>Edge adhesives seep in ≤1/2 Margin width, Length excluding Edge adhesives bubble; bubble width≤1/2 Margin width; Length≤0.5mm, n≤5 | MI | | |
| 13 | Protect film | Surface scratch but not effect protect function, Allowed | MI | Visual Inspection | |
| 14 | Silicon glue | Thickness≤PS surface (with protect film); Full cover the IC;<br>Shape: The width on FPC≤0.5mm (Front); The width on the FPC≤1.0mm (Back) Smooth surface. No obvious raised. | MI | Visual Inspection | |
| 15 | Warp degree (TFT substrate) |  <br>t ≤2.5mm | MI | Ruler | |
| 16 | Color difference in COM area (Silver point area) | Allowed | | Visual Inspection | |

# 13. HANDLING, SAFETY, AND ENVIRONMENT REQUIREMENTS

**WARNING**

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

**CAUTION**

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

| **Data sheet status** | |
|---|---|
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).<br>Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

# 14. PRECAUTIONS

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL/EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL/EPD Tag with a completely white image to avoid this issue.

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.