3.52inch e-Paper (B)

User Manual

Revision History

Version	Content	Date	Page
1.0	New creation	2024/09/05	All

Contents

1. OVERVIEW

3.52inch e-Paper (B) is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 3.52” active area contains 240×360 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. FEATURES

- ✧ 240x360 pixels display
- ✧ High contrast
- ✧ High reflectance
- ✧ Ultra wide viewing angle
- ✧ Ultra low power consumption
- ✧ Pure reflective mode
- ✧ Bi-stable display
- ✧ Commercial temperature range
- ✧ Landscape portrait modes
- ✧ Hard-coat antiglare display surface
- ✧ Ultra low current deep sleep mode
- ✧ On chip display RAM
- ✧ Low voltage detect for supply voltage
- ✧ High voltage ready detect for driving voltage
- ✧ Internal temperature sensor
- ✧ 10-byte OTP space for module identification
- ✧ Waveform stored in On-chip OTP
- ✧ Serial peripheral interface available
- ✧ On-chip oscillator
- ✧ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ✧ I2C signal master interface to read external temperature sensor

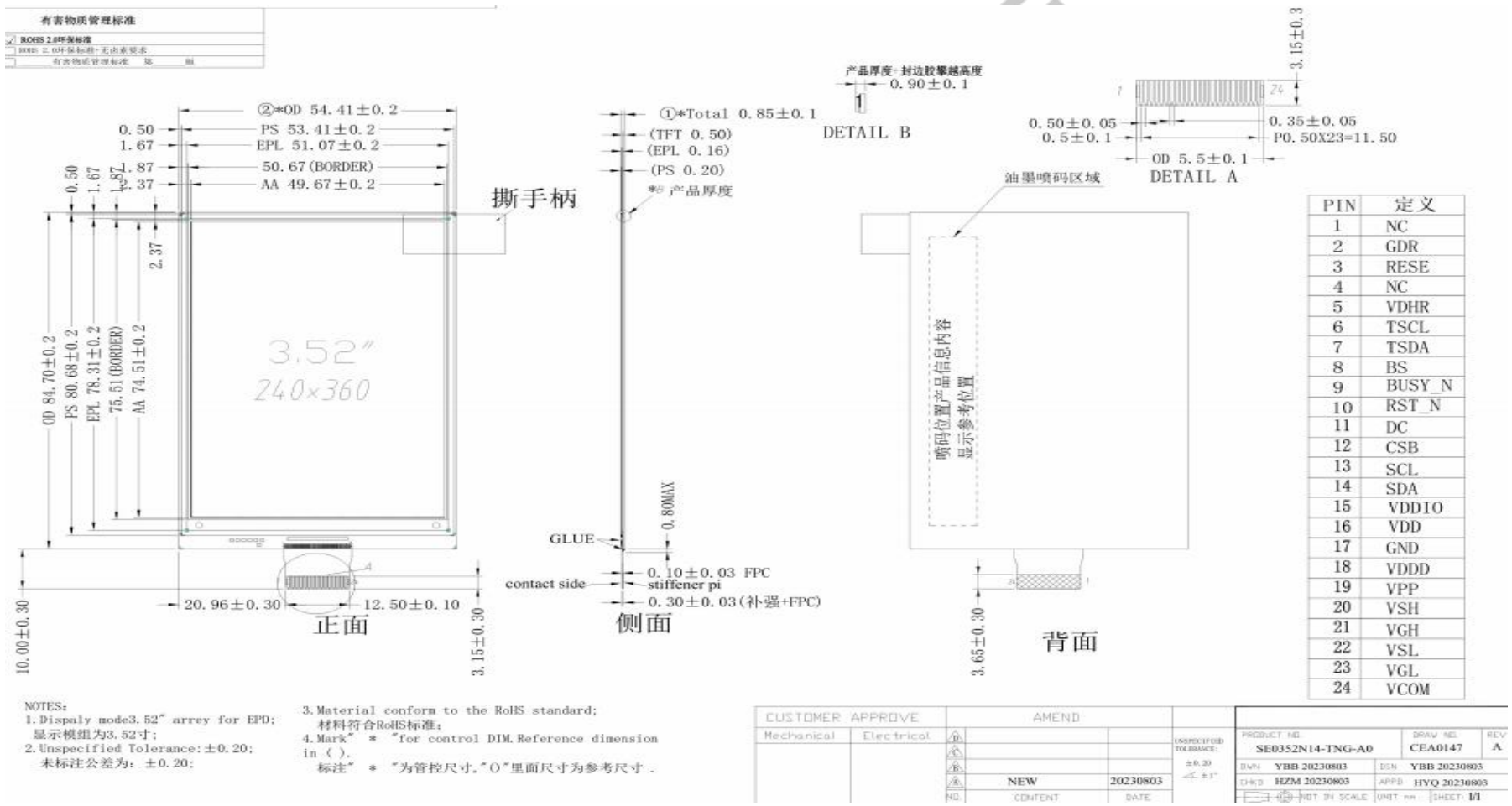
3. APPLICATION

Electronic Shelf Label System

4. MECHANICAL SPECIFICATION

Parameter	Specification	Unit	Remark
Screen Size	3.52	Inch	
Display Resolution	240(H) x 360(V)	Pixel	
Active Area	48.67(H) x 74.51(V)	mm	
Pixel Pitch	0.207 x 0.207	mm	
Pixel Configuration	Rectangle		
Outline Dimension	54.41(H)×84.70(V)×0.85(D)	mm	
Weight	TBD	g	

5. MECHANICAL DRAWING OF EPD MODULE



PIN	定义
1	NC
2	GDR
3	RESE
4	NC
5	VDHR
6	TSCL
7	TSDA
8	BS
9	BUSY_N
10	RST_N
11	DC
12	CSB
13	SCL
14	SDA
15	VDDIO
16	VDD
17	GND
18	VDDD
19	VPP
20	VSH
21	VGH
22	VSL
23	VGL
24	VCOM

6. INPUT/OUTPUT PIN ASSIGNMENT

NO.	Name	I/O	Description	Remark
1	NC		No connection and do not connect with other NC pins	Keep open
2	GDR	0	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		No connection and do not connect with other NC pins	Keep open
5	VDHR	C	Positive Source driving voltage	
6	TSCL	0	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/0	I2C Interface to digital temperature sensor Date pin	
8	BS	I	Bus selection pin	Note 6-5
9	BUSY_N	0	Busy state output pin	Note 6-4
10	RST_N	I	Reset	Note 6-3
11	DC	I	Data /Command control pin	Note 6-2
12	CSB	I	Chip Select input pin	Note 6-1
13	SCL	I	serial clock pin (SPI)	
14	SDA	I/0	serial data pin (SPI)	
15	VDDIO	P	Power for interface logic pins	
16	VDD	P	Power Supply pin for the chip	
17	GND	P	Ground	
18	VDDD	C	Core logic power pin	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive source driver Voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate voltage.	
24	VCOM	C	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY_N) is Driver busy flag.L: Driver is Busy.

H: Host side can send command/data to driver. Note 6-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI is selected.

7. HOST INTERFACE

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high.

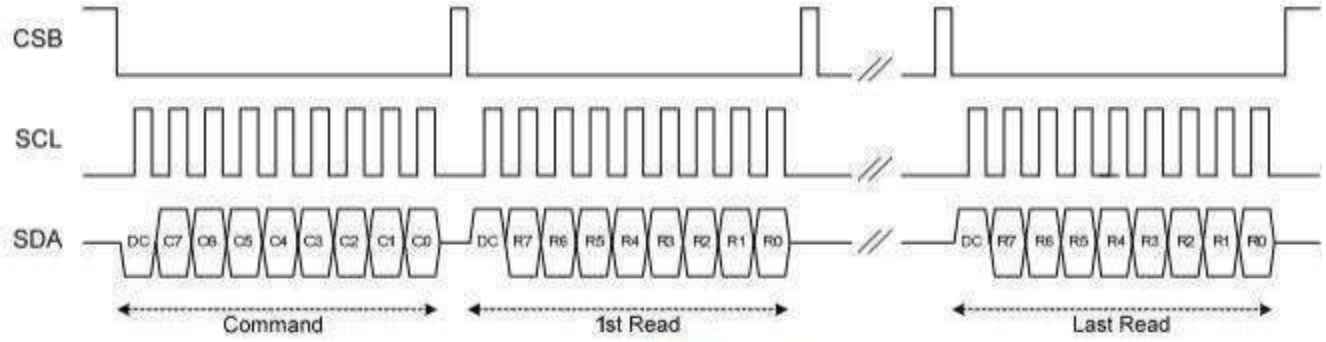


Figure: 3-wire SPI read operation

HT0001 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

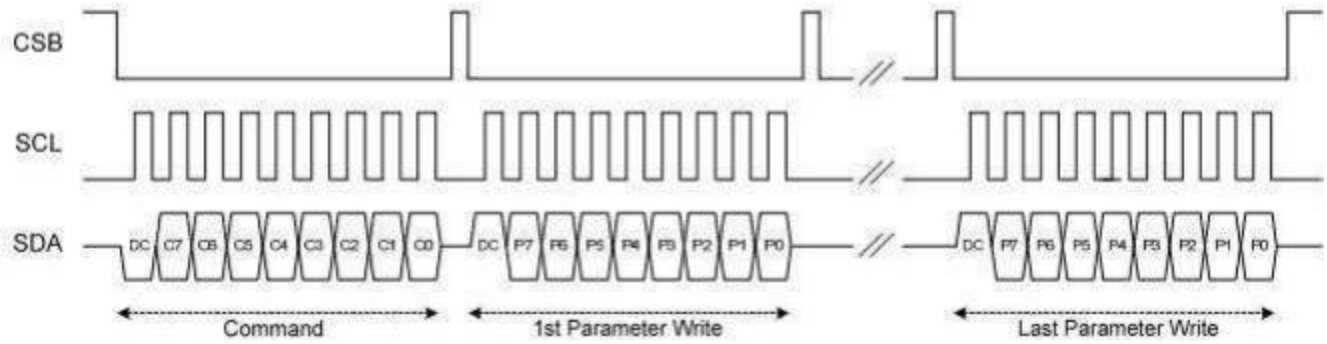


Figure: 3-wire SPI write operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

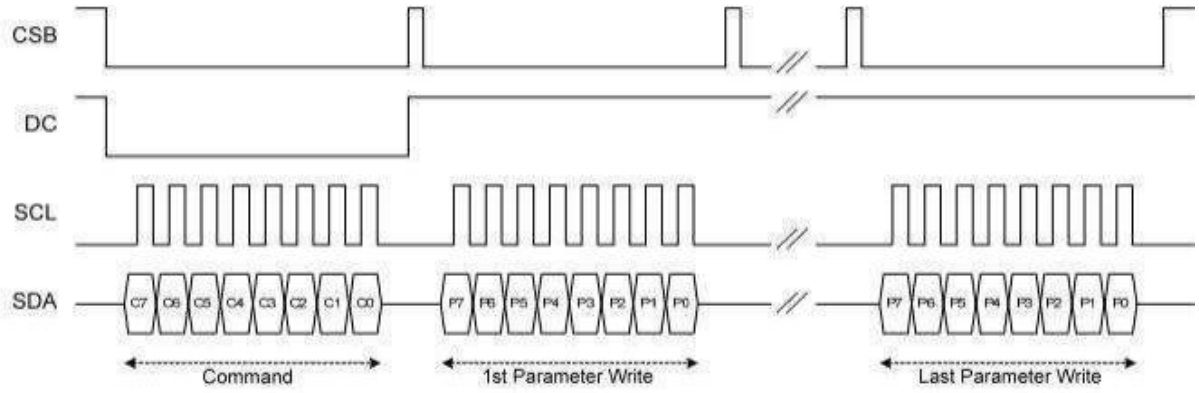


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

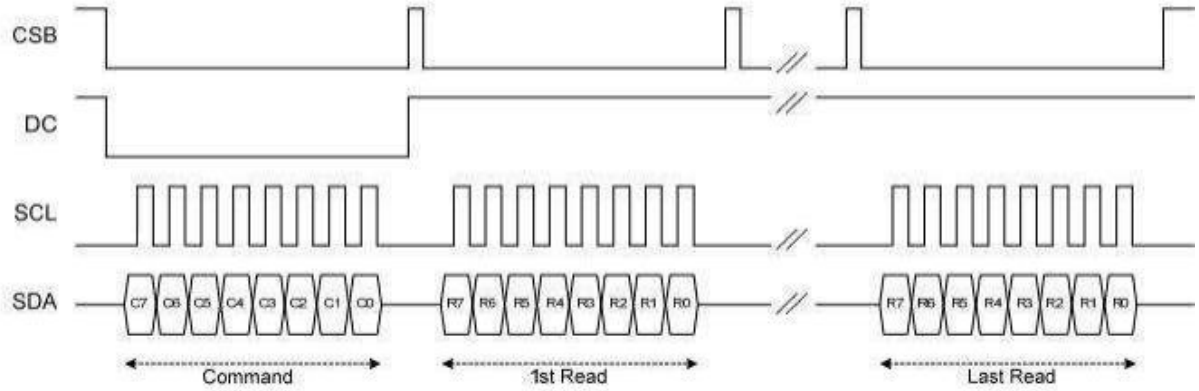


Figure: 4-wire SPI read operation

8. TEMPERATURE SENSOR OPERATION

Following is the way of how to sense the ambient temperature of the module. First, use an external temperature sensor to get the temperature value and converted it into HEX format with below mapping table, then send command 0x1A with the HEX temperature value to the module thru the SPI interface.

The temperature value to HEX conversion is as follow:

1. If the Temperature value MSByte bit D11 = 0, then

The temperature is positive and value (DegC) = + (Temperature value) / 16

2. If the Temperature value MSByte bit D11 = 1, then~

The temperature is negative and value (DegC) = (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

9. COMMAND TABLE

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD,SHL, SHD_N,RST_N	0FH
		0	1	--	--	--	#	#	#	#	#	VCMZ ,TS_AUTO,TIEG,NORG,VCM_LUTZ	8DH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	#	--	--	#	#	BD_EN ,VDS_EN, VDG_EN	03H
		0	1	--	--	--	#	#	#	#	#	VCOM_SLEW,VGHL_LV[3:0]	10H
		0	1	--	--	#	#	#	#	#	#	VDH[5:0]	3FH
		0	1	--	--	#	#	#	#	#	#	VDL[5:0]	3FH
		0	1	#	#	#	#	#	#	#	#	OPEN,VDHR[6:0]	0DH
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W or OLD Pixel Data (400x300):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00H
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--	Data_flag	00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (240x480):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	00H
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		1	1	1	0	1	0	0	1	0	1	Check code	A5H
14	VCOM LUT (LUTC) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0		20H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~8 repeated 6 times)	0	0	0	0	1	0	0	0	0	1		21H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H
16	K2W LUT (LUTKW / LUTR) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	1	0		22H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H
17	W2K LUT (LUTWK / LUTW) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	1	1		23H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H
18	K2K LUT (LUTKK / LUTK) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	1	0	0		24H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	00H
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	00H
19	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	#	--	--	--	--	--	--	--	EOPT	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[15:8]	00H
		0	1	#	#	#	#	#	#	#	#	GROUP_KWE[7:0]	FFH
		0	1	--	--	--	--	--	--	#	#	ATRED , NORED	00H
20	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	--	--	#	#	#	#	#	#	FRS[4:0]	06H
21	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
22	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00H
23	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42H
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
24	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43H
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
25	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44H
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
26	VCOM and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50H
		0	1	#	#	#	#	#	#	#	#	VBD[1:0], DDX[1:0], CDI[3:0]	D7H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
27	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51H
		1	1	--	--	--	--	--	--	--	#	LPD	01H
28	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
29	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
30	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
31	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H
		0	0	#	#	#	#	#	#	#	#	Reserved	00H
		1	1	#	#	#	#	#	#	#	#	CHIP_REV[7:0]	09H
		1	1	#	#	#	#	#	#	#	#	LUT_REV[23:0]	FFH
		1	1	:	:	:	:	:	:	:	:		FFH
		1	1	#	#	#	#	#	#	#	#		FFH
32	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I²C_ERR, I²C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
33	Cyclic Redundancy Check (CRC)	0	0	0	1	1	0	0	0	1	0		72H
		1	1	#	#	#	#	#	#	#	#	CRC_MSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	CRC_LSB[7:0]	00H
34	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
35	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00H
36	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	00H
37	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	07H
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
38	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H
39	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H
40	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H
41	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H
42	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
43	OTP Programming Address (PGAR)	0	0	1	0	1	0	0	0	1	1		A3 H
		0	1	--	--	--	#	#	#	#	#	ST_ADDR[12:8]	00
		0	1	#	#	#	#	#	#	#	#	ST_ADDR[7:0]	00

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
46	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4H
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
47	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5H
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

10. COMMAND DESCRIPTION

COMMAND DESCRIPTION

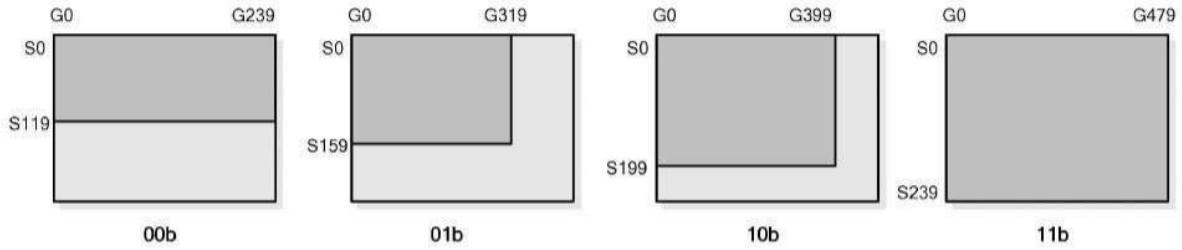
W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH
	0	1	0	0	0	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	0DH

RES[1:0]: Display Resolution setting (source x gate)

00b: 240x120 (Default)	Active gate channels: G0 ~ G239. Active source channels: S0 ~ S119.
01b: 320x160	Active gate channels: G0 ~ G319. Active source channels: S0 ~ S159.
10b: 400x200	Active gate channels: G0 ~ G399. Active source channels: S0 ~ S199.
11b: 480x240	Active gate channels: G0 ~ G479. Active source channels: S0 ~ S239.



REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50uS to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.

1: No effect (Default).

VCMZ: VCOM Hi-Z state function

0: No effect (Default)

1 : VCOM is always floating

TS_AUTO: Temperature sensor will be activated automatically one time.

0: No effect

1: Before enabling booster, Temperature Sensor will be activated automatically one time (Default).

TIEG: VGL state function

0: No effect

1 : After power off booster, VGL will be tied to GND (Default).

NORG: VCOM state during refreshing display

0: No effect (Default)

1: Expect refreshing display, VCOM is tied to GND.

VC_LUTZ: VCOM state during refreshing display

0: No effect

1: After refreshing display, the output of VCOM is set to floating automatically (Default).

Note: Priority of Vcom setting: VCMZ > EOPT > NORG > VC_LUTZ

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01H
	0	1	-	-	-	BD_EN	-	-	VDS_EN	VDG_EN	03H
	0	1	-	-	-	VCOM_SLEW	VGHL_LV[3:0]				10H
	0	1	-	-	VSH[5:0]						3FH
	0	1	-	-	VSL[5:0]						3FH
	0	1	OPTEN	VDHR[6:0]							0DH

BD_EN: Border LDO enable
0 : Border LDO disable (Default)
Border level selection: 00b: VCOM 01b: VDH 10b: VDL 11b: VDHR
1 : Border LDO enable
Border level selection: 00b: VCOM 01b: VBH(VCOM-VDL) 10b:VBL(VCOM-VDH) 11b: VDHR

VDS_EN: Source power selection
0 : External source power from VSH/VSL/VDHR pins
1 : Internal DC/DC function for generating VSH/VSL/VDHR. (Default)

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_SLEW: VCOM slew rate selection for voltage transition. The value is fixed at **1**.

VGHL_LV[3:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
0000 (Default)	VGH=20V, VGL= -20V
0001	VGH=19V, VGL= -19V
0010	VGH=18V, VGL= -18V
0011	VGH=17V, VGL= -17V
0100	VGH=16V, VGL= -16V
0101	VGH=15V, VGL= -15V
0110	VGH=14V, VGL= -14V
0111	VGH=13V, VGL= -13V
1000	VGH=12V, VGL= -12V
1001	VGH=11V, VGL= -11V
1010	VGH=10V, VGL= -10V

VSH[5:0]: Internal VSH power selection for B/W pixel.(**Default value: 11 1111b**)

VSH	Voltage	VSH	Voltage	VSH	Voltage	VSH	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	5.0 V	01 1101	8.2V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	**11 1111**	**15.0 V**

VSL[5:0]: Internal VSL power selection for B/W pixel. (**Default value: 11 1111b**)

VSL	Voltage	VSL	Voltage	VSL	Voltage	VSL	Voltage
00 0000	-2.4 V	01 0000	-5.6 V	10 0000	-8.8 V	11 0000	-12.0 V
00 0001	-2.6 V	01 0001	-5.8 V	10 0001	-9.0 V	11 0001	-12.2 V
00 0010	-2.8 V	01 0010	-6.0 V	10 0010	-9.2 V	11 0010	-12.4 V
00 0011	-3.0 V	01 0011	-6.2 V	10 0011	-9.4 V	11 0011	-12.6 V
00 0100	-3.2 V	01 0100	-6.4 V	10 0100	-9.6 V	11 0100	-12.8 V
00 0101	-3.4 V	01 0101	-6.6 V	10 0101	-9.8 V	11 0101	-13.0 V
00 0110	-3.6 V	01 0110	-6.8 V	10 0110	-10.0V	11 0110	-13.2 V
00 0111	-3.8 V	01 0111	-7.0 V	10 0111	-10.2 V	11 0111	-13.4 V
00 1000	-4.0 V	01 1000	-7.2 V	10 1000	-10.4 V	11 1000	-13.6 V
00 1001	-4.2 V	01 1001	-7.4 V	10 1001	-10.6 V	11 1001	-13.8 V
00 1010	-4.4 V	01 1010	-7.6 V	10 1010	-10.8 V	11 1010	-14.0 V
00 1011	-4.6 V	01 1011	-7.8 V	10 1011	-11.0 V	11 1011	-14.2 V
00 1100	-4.8 V	01 1100	-8.0 V	10 1100	-11.2 V	11 1100	-14.4 V
00 1101	-5.0 V	01 1101	-8.2 V	10 1101	-11.4 V	11 1101	-14.6 V
00 1110	-5.2 V	01 1110	-8.4 V	10 1110	-11.6 V	11 1110	-14.8 V
00 1111	-5.4 V	01 1111	-8.6 V	10 1111	-11.8 V	**11 1111**	**-15.0 V**

VDHR[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 001101b**)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0 V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	**5.0 V**	01 1101	8.2 V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	11 1111	15.0 V

OPTEN: 1 enable step-0.1V voltage selection.

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
1000 0000	2.4 V	1010 0000	5.6 V	1100 0000	8.8 V	1110 0000	12 V
1000 0001	2.5 V	1010 0001	5.7 V	1100 0001	8.9 V	1110 0001	12.1 V
1000 0010	2.6 V	1010 0010	5.8 V	1100 0010	9.0 V	1110 0010	12.2 V
1000 0011	2.7 V	1010 0011	5.9 V	1100 0011	9.1 V	1110 0011	12.3 V
1000 0100	2.8 V	1010 0100	6.0 V	1100 0100	9.2 V	1110 0100	12.4 V
1000 0101	2.9 V	1010 0101	6.1 V	1100 0101	9.3 V	1110 0101	12.5 V
1000 0110	3.0 V	1010 0110	6.2 V	1100 0110	9.4 V	1110 0110	12.6 V
1000 0111	3.1 V	1010 0111	6.3 V	1100 0111	9.5 V	1110 0111	12.7 V
1000 1000	3.2 V	1010 1000	6.4 V	1100 1000	9.6 V	1110 1000	12.8 V
1000 1001	3.3 V	10101001	6.5 V	1100 1001	9.7 V	1110 1001	12.9 V
1000 1010	3.4 V	1010 1010	6.6 V	1100 1010	9.8 V	1110 1010	13.0 V
1000 1011	3.5 V	1010 1011	6.7 V	1100 1011	9.9 V	1110 1011	13.1 V
1000 1100	3.6 V	1010 1100	6.8 V	1100 1100	10.0 V	1110 1100	13.2 V
1000 1101	3.7 V	1010 1101	6.9 V	1100 1101	10.1 V	1110 1101	13.3 V
1000 1110	3.8 V	1010 1110	7.0 V	1100 1110	10.2 V	1110 1110	13.4 V
1000 1111	3.9 V	1010 1111	7.1 V	1100 1111	10.3 V	1110 1111	13.5 V
1001 0000	4.0 V	1011 0000	7.2 V	1101 0000	10.4 V	1111 0000	13.6 V
1001 0001	4.1 V	1011 0001	7.3 V	1101 0001	10.5 V	1111 0001	13.7 V
1001 0010	4.2 V	1011 0010	7.4 V	1101 0010	10.6 V	1111 0010	13.8 V
1001 0011	4.3 V	1011 0011	7.5 V	1101 0011	10.7 V	1111 0011	13.9 V
1001 0100	4.4 V	1011 0100	7.6 V	1101 0100	10.8 V	1111 0100	14.0 V
1001 0101	4.5 V	1011 0101	7.7 V	1101 0101	10.9 V	1111 0101	14.1 V
1001 0110	4.6 V	1011 0110	7.8 V	1101 0110	11.0 V	1111 0110	14.2 V
1001 0111	4.7 V	1011 0111	7.9 V	1101 0111	11.1 V	1111 0111	14.3 V
1001 1000	4.8 V	1011 1000	8.0 V	1101 1000	11.2 V	1111 1000	14.4 V
1001 1001	4.9 V	1011 1001	8.1 V	1101 1001	11.3 V	1111 1001	14.5 V
1001 1010	5.0 V	1011 1010	8.2 V	1101 1010	11.4 V	1111 1010	14.6 V
1001 1011	5.1 V	1011 1011	8.3 V	1101 1011	11.5 V	1111 1011	14.7 V
1001 1100	5.2 V	1011 1100	8.4 V	11011100	11.6 V	1111 1100	14.8 V
1001 1101	5.3 V	1011 1101	8.5 V	1101 1101	11.7 V	1111 1101	14.9 V
1001 1110	5.4 V	1011 1110	8.6 V	1101 1110	11.8 V	1111 1110	15.0 V
1001 1111	5.5 V	1011 1111	8.7 V	1101 1111	11.9 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03H
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17H
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17H
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17H

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "OLD" data to SRAM.

In KWR mode, this command writes "B/W" data to SRAM.

In Program mode, this command writes "OTP" data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become "0".

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become "0" and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be larger than 200uS.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "NEW" data to SRAM.

In KWR mode, this command writes "RED" data to SRAM.

(13) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	0	0	0	1	0	1	1	1	17H
	0	1	1	0	1	0	0	1	0	1	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for VCOM (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0	20H
	0	1	Group Repeat Time [7:0]								00H
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						0
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						0
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						0
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						0
	0	1	State 1 repeat times [7:0]								0
	0	1	State 2 repeat times [7:0]								0

This command stores VCOM Look-Up Table with 8 groups of data. This LUT includes 8 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,... :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34.....:

[D7:D6] Level selection

00b: VCOM_DC

01b: VSH+VCOM_DC (VCOMH)

10b: VSL-VCOM_DC (VCOML)

11b: Floating

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), all 8 groups are used.

If KW/R=1 (KW mode), only 6 groups are used.

(15) W2W LUT (LUTWW) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build White Look-up Table for W2W (43-byte command, structure of bytes 2~8 repeated 6 times)	0	0	0	0	1	0	0	0	0	1	21H
	0	1	Group Repeat Time [7:0]								
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						00H
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						
	0	1	State 1 repeat times [7:0]								
	0	1	State 2 repeat times [7:0]								

This command stores LUTW2W Look-Up Table with 6 groups of data. This LUT includes 6 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,... :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34.....:

[D7:D6] Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), LUTWW is not used.

If KW/R=1 (KW mode), LUTWW is used.

(16) K2W LUT (LUTKW / LUTR) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for K2W or Red (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0	20H
	0	1	Group Repeat Time [7:0]								00H
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						00H
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						00H
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						00H
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						00H
	0	1	State 1 repeat times [7:0]								00H
	0	1	State 2 repeat times [7:0]								00H

This command stores LUTKW / LUTR Look-Up Table with 8 groups of data. This LUT includes 8 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,... :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34.....:

[D7:D6] Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), all 8 groups are used.

If KW/R=1 (KW mode), only 6 groups are used.

(17) W2K LUT (LUTWK / LUTW) (R23H)

This command builds Look-up Table for White-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used.

(18) K2K LUT (LUTKK / LUTK) (R24H)

This command builds Look-up Table for Black-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.

Note: All LUTs are independent of each other and could be deal with separately.If waveform time is different for each LUT , IC would elect longest LUT as refresh time and fill 0 (GND) to remaining refresh time for other LUT.

(19) LUT OPTION (LUTOPT) (R2AH)

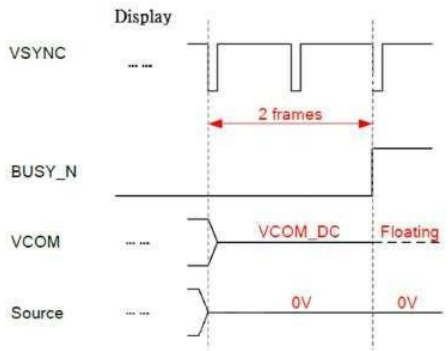
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	2AH
	0	1	EOPT	ESO	-	-	-	-	-	-	00H
	0	1	STATE_XON[7:0]								00H
	0	1	STATE_XON[15:8]								00H
	0	1	GROUP_KWE[7:0]								FFH
	0	1	-	-	-	-	-	ATRED	NORED		00H

This command sets XON and the several options of KWR mode's LUT. .

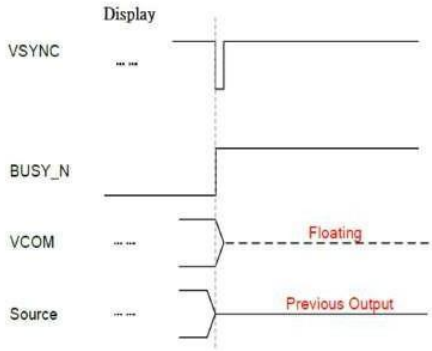
EOPT: LUT sequence option

0: Disable 1: Enable

EOPT=0



EOPT=1



ESO: LUT sequence option 2

STATE_XON[15:0]:

All Gate ON control (Each bit controls one state, STATE_XON [0] for Group-1/State-1, STATE_XON [1] for Group-1/State-2 .....)

0000 0000 0000 0000b: no All-Gate-ON

0000 0000 0000 0001b: Group-1/State-1 All-Gate-ON

0000 0000 0000 0011b: Group-1/State-1 and Group-1/State-2 All-Gate-ON

0000 0000 0000 0111b: Group-1/State-1, Group-1/State-2 and Group-2/State-1 All-Gate-ON

: :

GROUP_KWE[7:0]:

The control bits are only available when KW/R=0 (KWR mode) and (ATRED | NORED)=1

There are only 8 groups in the K/W LUT. Each bit controls one group.

1111 1111b: all groups are executed sequentially.

1111 1110b: only Group-1 is bypassed.

1111 1100b: Group-1 and Group-2 are bypassed.

: :

ATRED: Automatic mode. The option is only available when KW/R=0

NORED: No Red data. The option is only available when KW/R=0

(20) PLL CONTROL (PLL) (R30H)

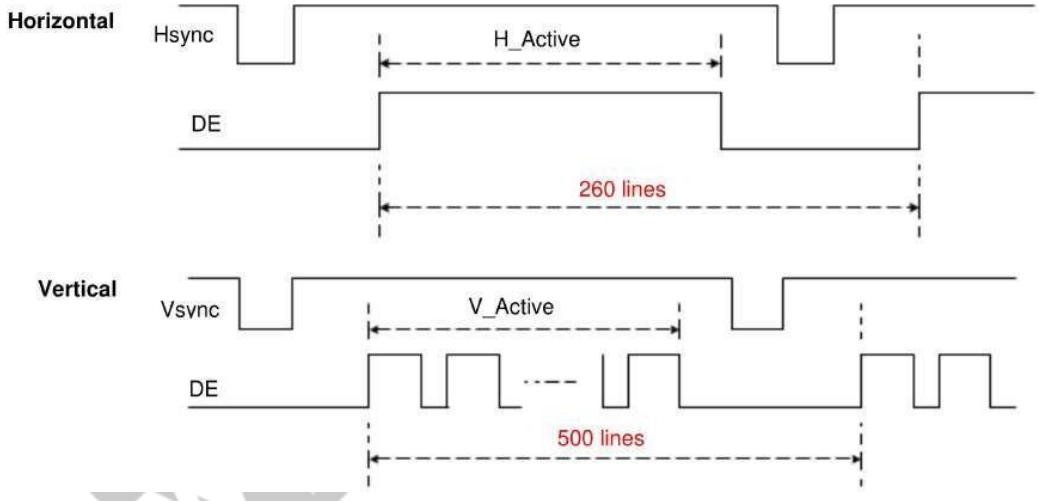
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30H
	0	1	-	-	-	FRS[4:0]					09H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[4:0]: Frame rate setting

FRS	Frame rate
00000	5Hz
00001	10Hz
00010	15Hz
00011	20Hz
00100	25Hz
00101	30Hz
00110	35Hz
00111	40Hz
01000	45Hz
01001	**50Hz**
01010	55Hz
01011	60Hz
01100	65Hz
01101	70Hz
01110	75Hz
01111	80Hz

FRS	Frame rate
10000	85Hz
10001	90Hz
10010	95Hz
10011	100Hz
10100	105Hz
10101	110Hz
10110	115Hz
10111	120Hz
11000	130Hz
11001	140Hz
11010	150Hz
11011	160Hz
11100	170Hz
11101	180Hz
11110	190Hz
11111	200Hz



(21) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature(°C)
0000_0000	**0**
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temperature(°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(22) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(23) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I²C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(24) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(25) PANEL GLASS CHECK (PBC) (R44H)

Action	R/W	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	44H
	R	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(26) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0	50h
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7h

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for B/W data,

DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

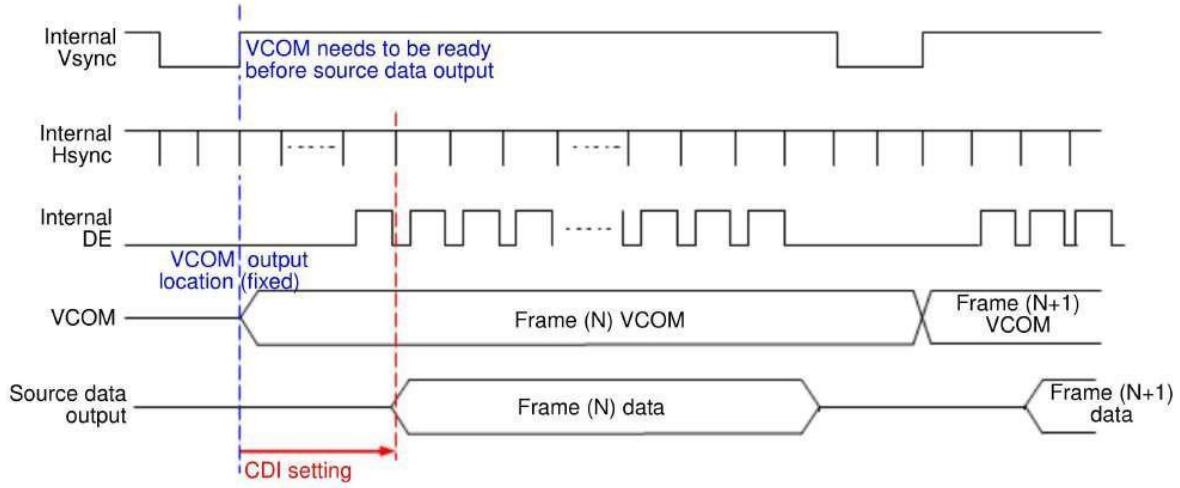
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



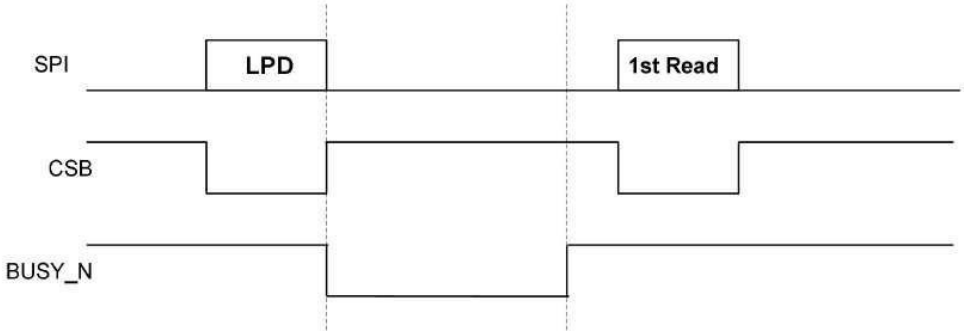
(27) Low Power Detection (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	0	1	0	1	0	0	0	1	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD}<2.5V, selected by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(28) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

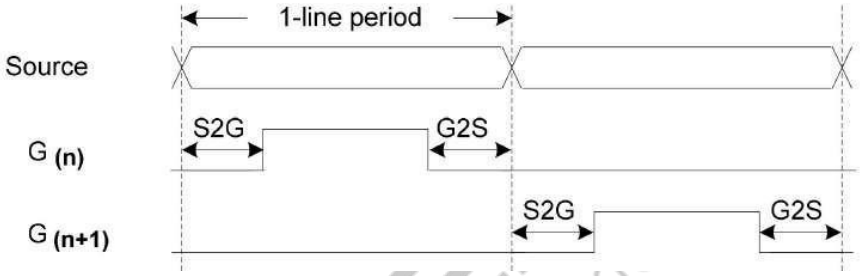
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 650 nS.



(29) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	HRES[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation, assuming HRES[7:3]=0, VRES[8:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[8:0] – 1

Source: First active source = S0;
Last active source = HRES[7:3]*8 - 1

Example: 128 (source) x 272 (gate), assuming HRES[7:3]=0, VRES[8:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[8:0] = 272, 272 - 1= 271)

Source: First active source = S0,
Last active source = S127; (HRES[7:3]=16, 16*8 – 1 = 127)

(30) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)

VST[8:0]: Vertical Display Start Position (Gate)

Example : For 128(Source) x 240(Gate)
HST[7:3] = 4 (HST[8:0] = 4*8 = 32),
VST[8:0] = 32

Gate: First active gate = G32 (VST[8:0] = 32),
Last active gate = G271 (VST[8:0] = 32, VRES[8:0] = 240, 32+240-1=271)

Source: First active source = S32 (HST[7:3] = 32),
Last active source = S159 (HST[7:3] = 32, HRES[8:0] = 128, 32+128-1=159)

(31) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	RESERVED								FFh
	1	1	CHIP_REV[7:0]								09h
	1	1	LUT_REV[7:0]								FFh
	1	1	LUT_REV[15:8]								FFh
	1	1	LUT_REV[23:16]								FFh

The LUT_REV is read from OTP address = 0x0017~0x0019 / 0x1017~0x1019.

CHIP_REV[7:0]: Chip Revision, fixed at 0x09h.

(32) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_ flag	I²C_ERR	I²C_ BUSYN	data_ flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_FLAG Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSYN: I²C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(33) CYCLIC REDUNDANCY CHECK (CRC) (R72H)

Action	R/W	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Cyclic redundancy check	R	0	0	1	1	1	0	0	1	0	72H
	R	1	CRC_MSB[7:0]								FFH
	R	1	CRC_LSB[7:0]								FFH

This command reads Cyclic redundancy check(CRC) result.

The calculation only includes 0x0000~0x1FEF OTP data..

Polynomial = $x^{16} + x^{12} + x^5 + 1$, initial vaulte: 16'hFFFF

The result will be reset after this command.

CRC_MSB[7:0]: Most significant bits of CRC result

CRC_LSB[7:0]: Most significant bits of CRC result

(34) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s
01b: 5s (default)
10b: 8s
11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(35) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	-	VV[6:0]						00h

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(36) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	-	VDCS[6:0]						00h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(37) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~1Dh)

HRED[7:3]: Horizontal end channel bank. (value 00h~1Dh). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~1DFh)

VRED[8:0]: Vertical end line. (value 000h~1DFh). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(38) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(39) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(40) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(41) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

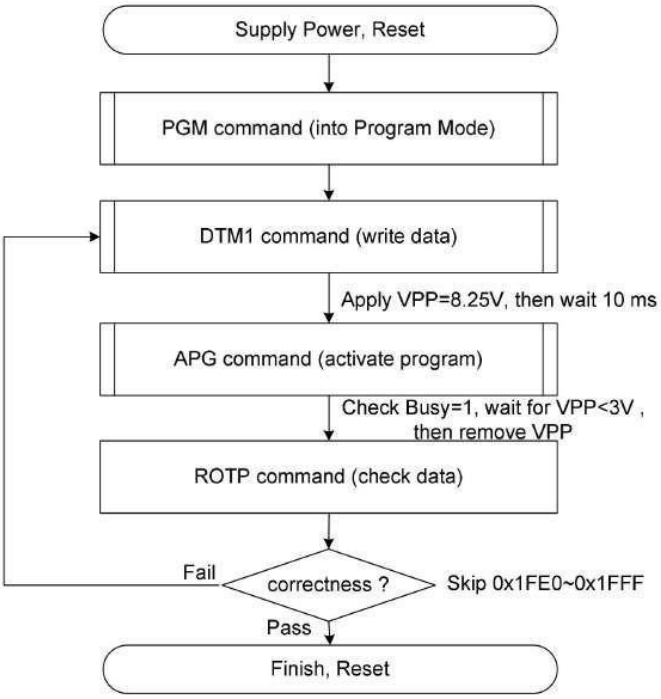
The BUSY_N flag would fall to 0 until the programming is completed.

(42) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.



The sequence of programming OTP.

(43) OTP PROGRAMMING ADDRESS (PGAR) (RA3H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
OTP Programming Address	0	0	1	0	1	0	0	0	1	1	A3H
	0	1	-	-	-	ST_ADDR[12:8]					00
	0	1	ST_ADDR[7:0]								00
	0	1	-	-	-	END_ADDR[12:8]					1F
	0	1	END_ADDR[7:0]								FF

The command is set OTP programming memory start address and end address.

ST_ADDR [12:0]: OTP programming start address.

END_ADDR [12:0]: OTP programming end address.

Example:

For Bank0 0x0000 (start address) ~ 0x0FFF (end address), 4K bytes.

ST_ADDR [12:8] = 0x00

ST_ADDR [7:0] = 0x00

END_ADDR [12:8] = 0x0F

END_ADDR [7:0] = 0xFF

For Bank1 0x1000 (start address) ~ 0x1FFF (end address), 4K bytes.

ST_ADDR [12:8] = 0x10

ST_ADDR [7:0] = 0x00

END_ADDR [12:8] = 0x1F

END_ADDR [7:0] = 0xFF

(44) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

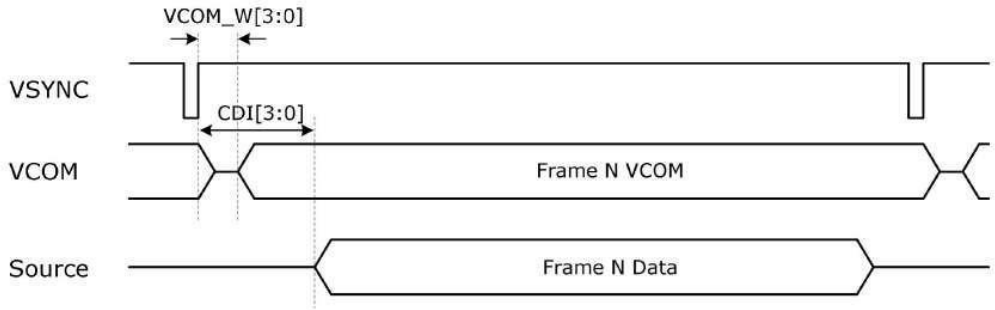
1: Temperature value is defined by TS_SET[7:0] registers.

(45) POWER SAVING (PWS) (RE3H)

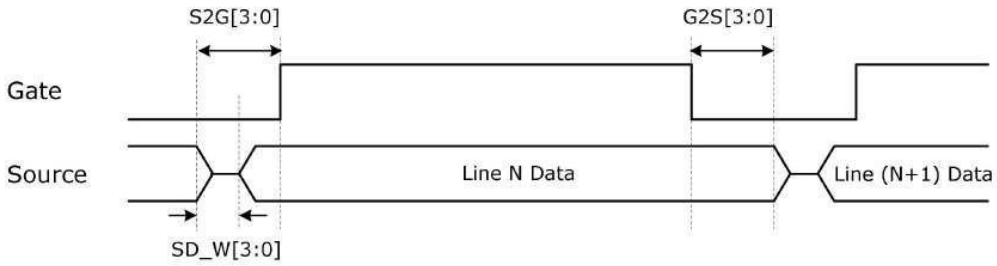
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 650nS)



(46) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

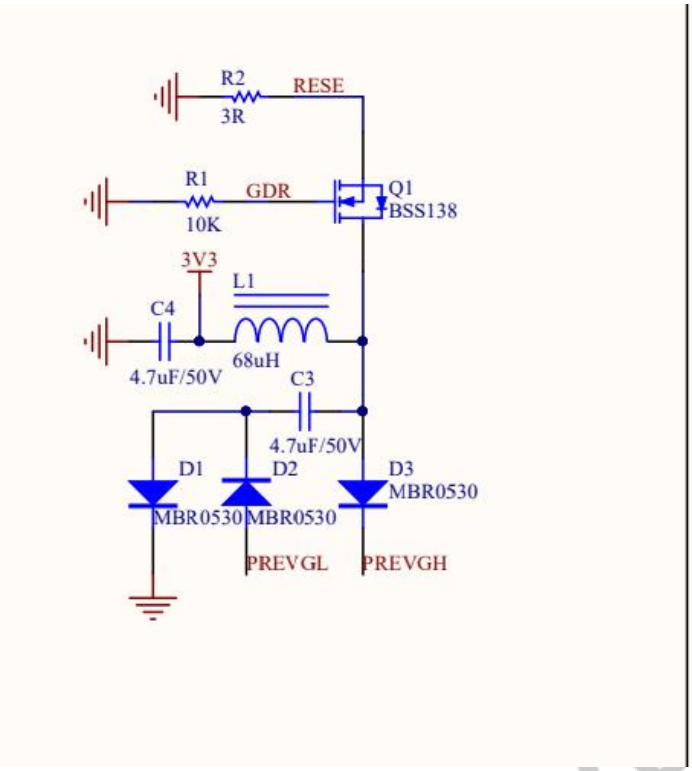
LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

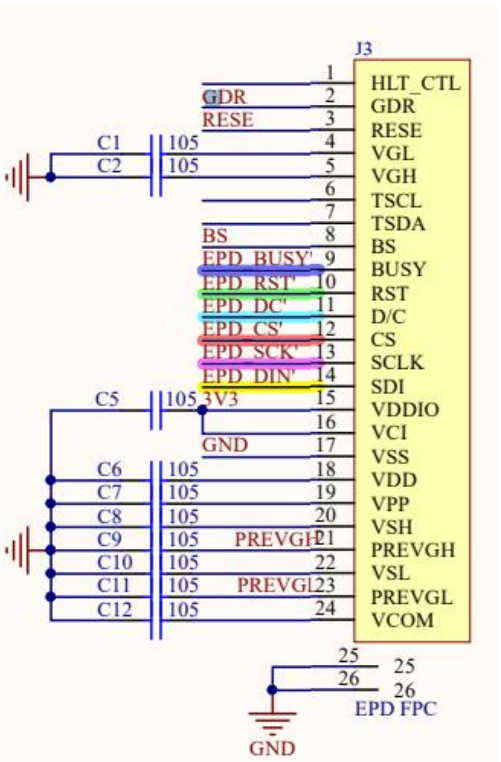
(47) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

11. REFERENCE CIRCUIT





12. ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
VDD	Logic supply voltage	-0.5 to +6.0	V	-	-	
TOPR	Operation temperature range	0 to 40	°C	45 to70	%	Note 12-1
Tttg	Transportation temperature range	-25 to 60	°C	45 to70	%	Note 12-2
Tstg	Storage condition	0 to 40	°C	45 to70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	°C	45 to70	%	

Note 12-1: We guarantee the single pixel display quality for 0-35℃, but we only guarantee the barcode readable for 35-40℃. Normal use is recommended to refresh every 24 hours.

Note 12-2: Tttg is the transportation condition, the transport time is within 10 days for -25℃~0℃ or 40℃~60℃ .

Note 12-3: When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months. We suggest that the full black and full white picture could be added to clear the screen after the module is refreshed for a long time, the display effect would be better.

13. DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, TOPR=25℃ .

Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VDD	VDD operation voltage	-	2.5	3.3	3.6	V
VI H	High level input voltage	-	0.8VDDIO	-	VDDIO	V
VIL	Low level input voltage	-	0	-	0.2VDDIO	V
VOH	High level output voltage	IOH = 400uA	0.8VDDIO	-	-	V
VOL	Low level output voltage	IOL = -400uA	0	-	0.2VDDIO	V
Iupdate	Module operating current	-	-	5	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-	3	uA

The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern.

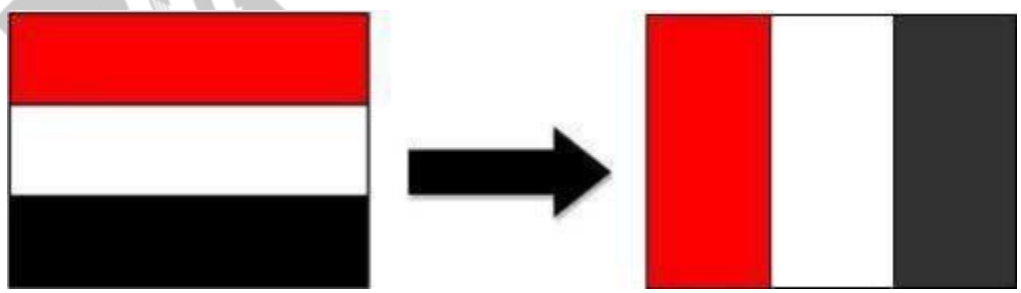
(Note 13-1)

- The listed electrical/optical characteristics are only guaranteed under the controller &waveform provided by SID.

- Vcom value will be OTP before in factory or present on the label sticker.

Note 13-1

The Typical power consumption



14. AC CHARACTERISTICS

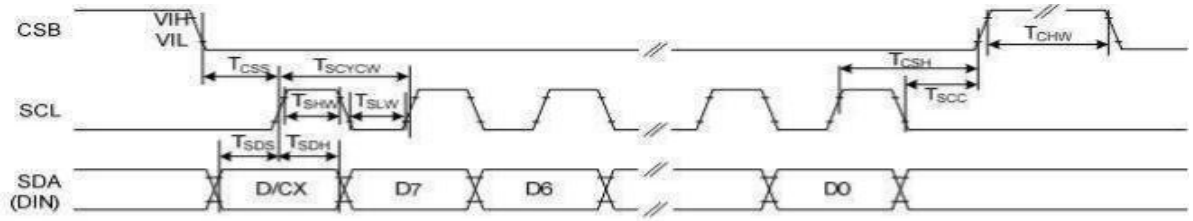


Figure: 3-wire Serial Interface Characteristics (Write mode)

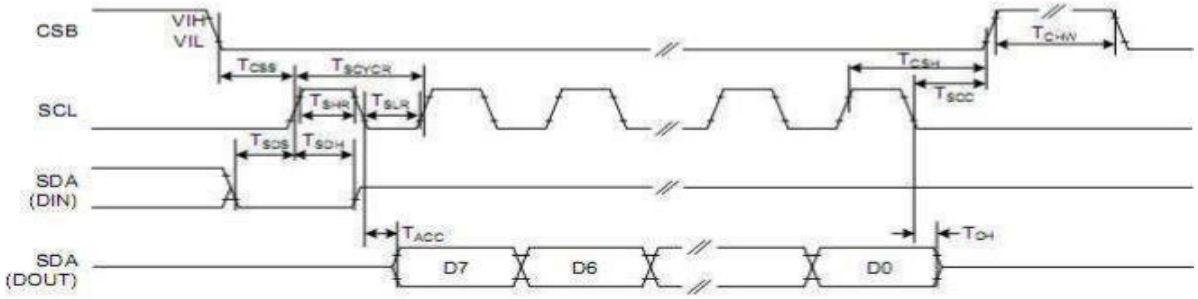


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL "H" pulse width (Read)	175			ns
T_{SLR}		SCL "L" pulse width (Read)	175			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			350	ns
T_{OH}		Output disable time	15			ns

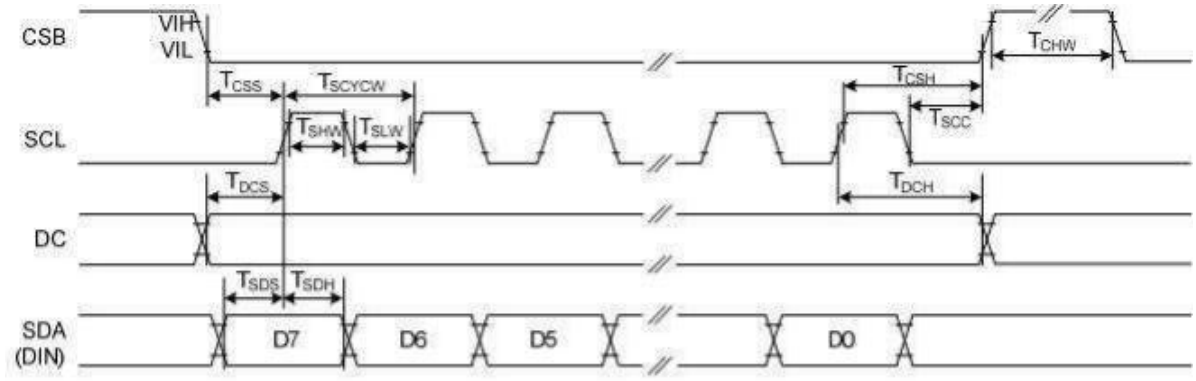


Figure: 4-wire Serial Interface Characteristics (Write mode)

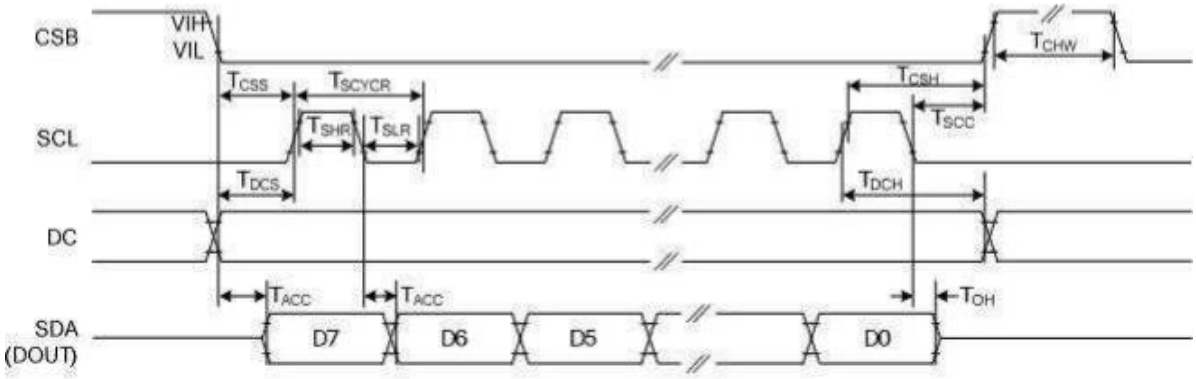


Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL "H" pulse width (Read)	175			ns
T_{SLR}		SCL "L" pulse width (Read)	175			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			350	ns
T_{OH}		Output disable time	15			ns

15. POWER CONSUMPTION

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	150	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

MAS=update average current×update time

16. OPTICAL CHARACTERISTICS

16.1 SPECIFICATION

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃, VDD=3.3V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 16-1
Gn	2Grey Level	-	-	KS+(WS-KS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	10	15	-		-
KS	Black State L* value		-	13	14		Note 16-1
	Black State a* value		-	3	4		Note 16-1
WS	White State L* value		63	65	-		Note 16-1
RS	Red State L* value	Red	25	28	-		Note 16-1
	Red State a* value	Red	36	40	-		Note 16-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-		-
	Update Time	Operation	-	Suggest Updated once a day	-		-

WS : White state, KS : Black state, RS: Red State

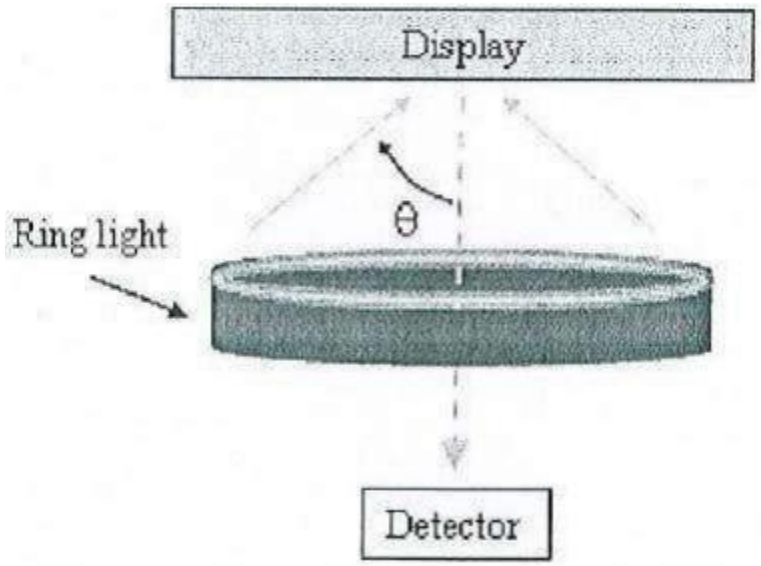
Note 16-1 : Luminance meter : i - One Pro Spectrophotometer

16.2 DEFINITION OF CONTRAST RATIO

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area(Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

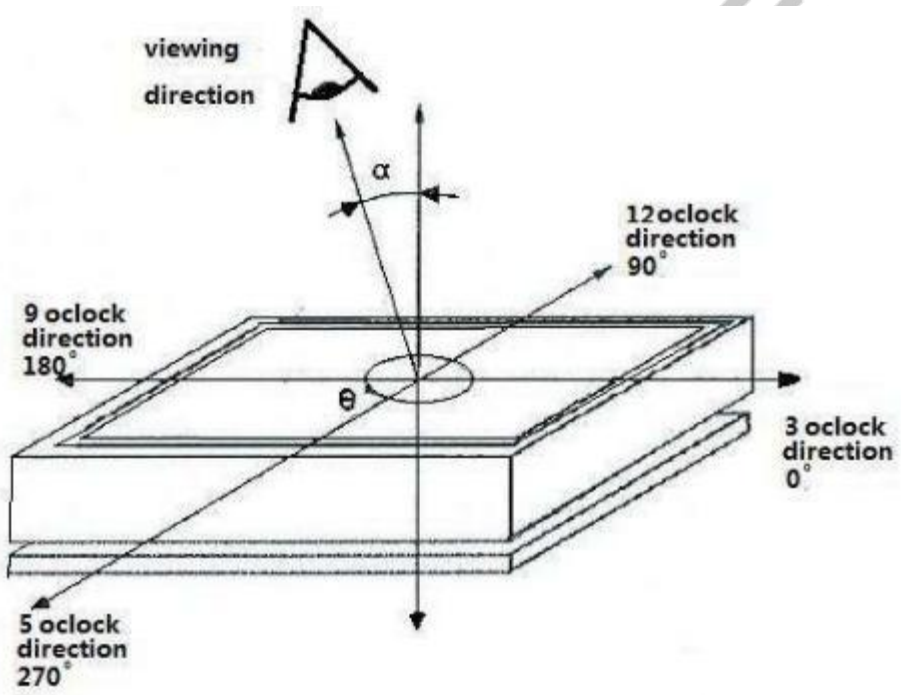


16.3 REFLECTION RATIO

The reflection ratio is expressed as:

R = Reflectance Factor whiteboard x (L center / L white board)

L_{center} is the luminance measured at center in a white area (R=G =B= 1). $L_{white\ board}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angles hall be no more than 2 degrees.



17. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING

The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions

(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied tothe module.

(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.

(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Somecosmetics deteriorate the PS)

(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.

(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Product Environmental Certification	
ROHS	
REMARK	
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.	

18. RELIABILITY TEST

18.1 RELIABILITY TEST ITEM

NO	Test items	Test condition	Remarks
1	High-Temperature Operation	T=40℃,RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0℃for 240 hrs	
3	High-Temperature Storage	T=50℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	Test in white pattern
5	High Temperature High Humidity Operation	T=40℃, RH=90%RH, For 168Hr	
6	High Temperature High Humidity Storage	T=50℃,RH=80%RH For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~60℃(30min)50 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency:20 200Hz Direction: X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3 edges, 6 face One drop for each.	Full packed for shipment
10	UV Exposure Resistance	765W/㎡ for 168hrs, 40℃	
11	Electrostatic Discharge	Machine model: +/-250V,0Ω ,200pF	

Actual EMC level to be measured on customer application.
Note1: Stay white pattern for storage and non-operation test.
Note 2: Operation is black/white/red pattern, hold time is 150S.
Note 3: The function, appearance should meet the requirements of the test before and after the test.
Note4: Keep testing after 2 hours placing at 20℃-25℃ .

18.2 PRODUCT LIFE TIME

The EPD Module is designed for a 5-year life-time with 25℃/60%RH operation assumption.

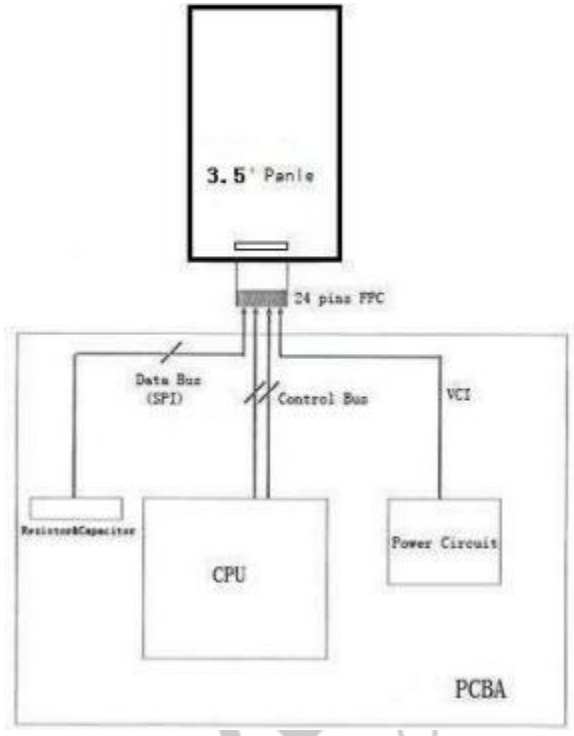
Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

18.3 PRODUCT WARRANTY

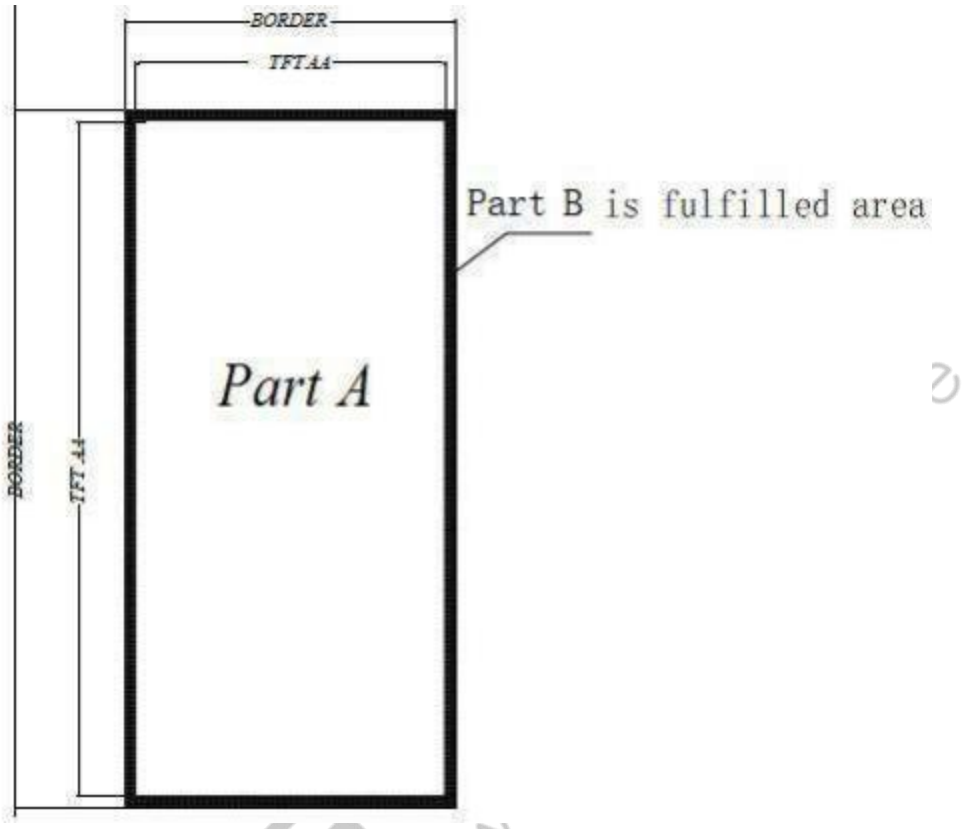
Warranty conditions have to be negotiated between SIDi and individual customers.

SID provides 12+1 (one month delivery time) months warranty for all products which are purchased from SID.

19. BLOCK DIAGRAM



20. PART A/PART B SPECIFICATION



21. POINT AND LINE STANDARD

<table>
<tr><td colspan="8">Shipment Inspection Standard, Equipment：Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline dimension</td><td colspan="2">54.41(H)x84.70(V)x0.91(D)</td><td>Unit: mm</td><td>Part-A</td><td>Active area</td><td>Part-B</td><td>Border area</td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>19℃~25℃</td><td>55%±5%RH</td><td>800~ 1300Lux</td><td>300mm</td><td>35Sec</td><td></td></tr>
<tr><td>Defet type</td><td colspan="2">Inspection method</td><td colspan="3">Standard</td><td>Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="3">Spot</td><td colspan="2" rowspan="3">Electric Display</td><td colspan="3">D≤0.25mm</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td colspan="3">0.25mm＜D≤0.4mm</td><td>N≤4</td><td>Ignore</td></tr>
<tr><td colspan="3">D＞0.4mm</td><td>Not Allow</td><td>Ignore</td></tr>
<tr><td>Display unwork</td><td colspan="2">Electric Display</td><td colspan="3">Not Allow</td><td>Not Allow</td><td>Ignore</td></tr>
<tr><td>Display error</td><td colspan="2">Electric Display</td><td colspan="3">Not Allow</td><td>Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">Scratch or line defect(include dirt)</td><td colspan="2" rowspan="3">Visual/Film card</td><td colspan="3">L≤2mm, W≤0.2mm</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td colspan="3">2.0mm＜L≤5.0mm
0.2＜W≤0.3mm</td><td>N≤2</td><td>Ignore</td></tr>
<tr><td colspan="3">L＞5mm, W＞0.3mm</td><td>Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">PS Bubble</td><td colspan="2" rowspan="3">Visual/Film card</td><td colspan="3">D≤0.2mm</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td colspan="3">0.2mm≤D≤0.35mm&N≤4</td><td>N≤4</td><td>Ignore</td></tr>
<tr><td colspan="3">D＞0.35 mm</td><td>Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">Side Fragment</td><td colspan="2" rowspan="3">Visual/Film card</td><td colspan="5">X≤6mm, Y≤0.4mm, Do not affect the electrode circuit (Edge chipping)</td></tr>
<tr><td colspan="5">X≤1mm, Y≤1mm, Do not affect the electrode circuit ((Corner chipping) Ignore</td></tr>
<tr><td colspan="5">  </td></tr>
<tr><td rowspan="3">Remark</td><td colspan="7">1. Appearance defect should not cause electrical defects;</td></tr>
<tr><td colspan="7">2. Appearance defects should not cause dimensional accuracy problems</td></tr>
<tr><td colspan="7">L=long, W=wide D=point size N=Defects NO</td></tr>
</table>