3.52inch e-Paper V1.1

User Manual

Revision History

Version	Content	Date	Page
1.0	New creation	2024/12/27	All

Contents

1. OVERVIEW

3.52inch e-Paper V1.1 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The 3.52” active area contains 240x360 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. The module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) system.

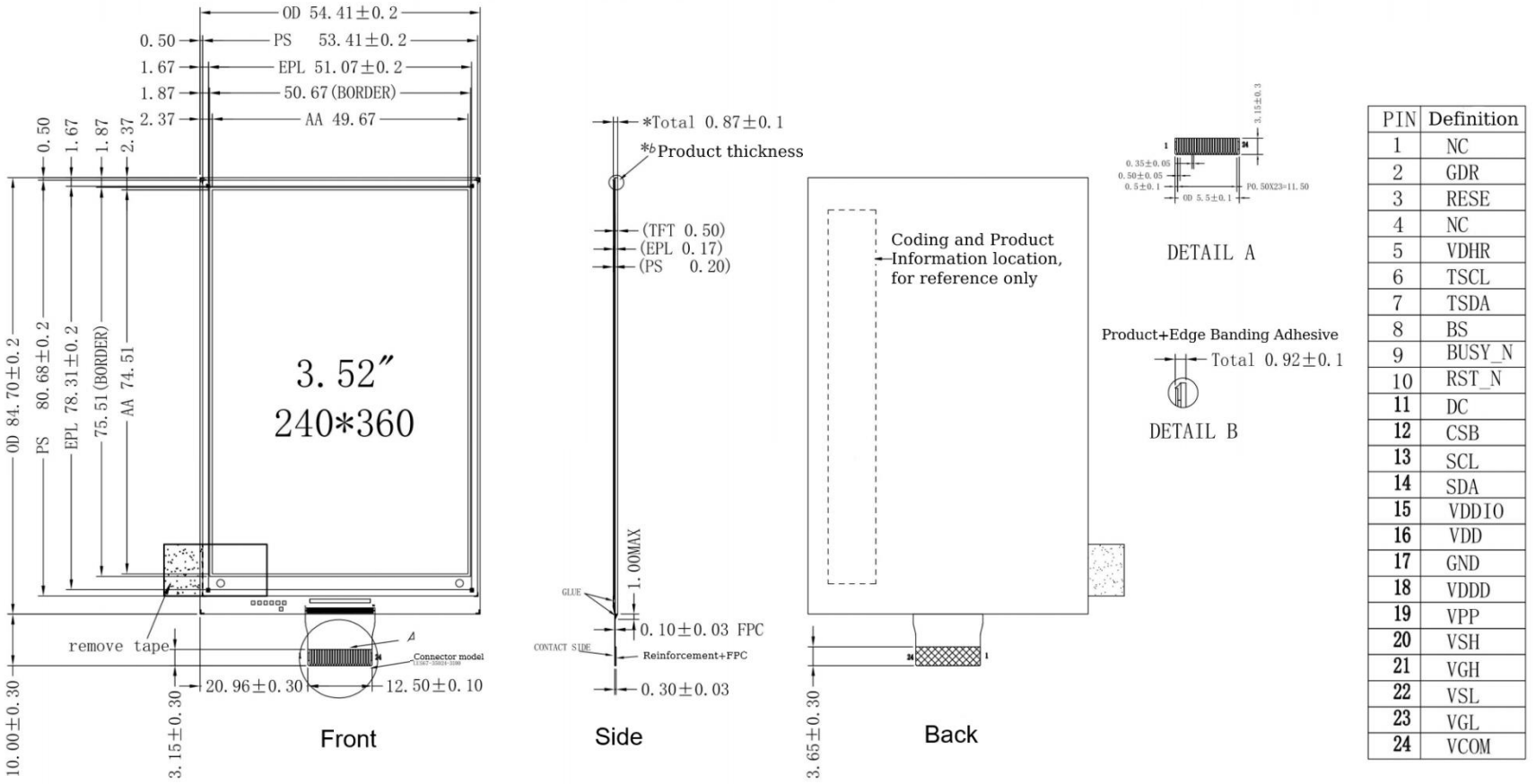
2. FEATURES

- 240×360 pixels display
- White reflectance above 30%
- Contrast ratio above 8:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Landscape and portrait modes
- Ultra low current deep sleep mode
- On-chip display RAM
- Waveform stored in on-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, gate and source driving voltage

3. MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Screen Size	3.52	Inch
Display Resolution	240 (H) x 360 (V)	Pixel
Active Area	49.67 (H) x 74.51 (V)	mm
Pixel Pitch	0.207 (H) x 0.207 (V)	mm
Pixel Configuration	Rectangle	
Outline Dimension	54.41 (H) × 84.70 (V) × 0.87 (D)	mm

4. MECHANICAL DRAWING OF EPD MODULE



PIN	Definition
1	NC
2	GDR
3	RESE
4	NC
5	VDHR
6	TSCL
7	TSDA
8	BS
9	BUSY_N
10	RST_N
11	DC
12	CSB
13	SCL
14	SDA
15	VDDIO
16	VDD
17	GND
18	VDDD
19	VPP
20	VSH
21	VGH
22	VSL
23	VGL
24	VCOM

Note: 1. Display module 3.52″ array for EPD; 2.Unspecified tolerance is ±0.20; 3. Materials confirm to RoHS standards;
4. The mark ✱ for control dimensions, ( ) for reference dimensions; 5. Product thickness includes: Top glass + EPL + PS.

5. PIN ASSIGNMENT

NO.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	VDHR	C	Positive Source driving voltage 1	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSY_N	O	Busy state output pin	Note 5-3
10	RST_N	I	Reset signal input. Active Low	
11	DC	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin. VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage 2	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note:

5-1: This pin is the chip select input pin connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

5-3: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent.The chip would put Busy pin Low when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

5-4: Bus interface selection pin

BS State	MPU Interface
L	4-line serial peripheral interface(SPI)
H	3-line serial peripheral interface(SPI) - 9 bits SPI

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Logic supply voltage	Vdd	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to Vdd +0.5	V
Logic Output voltage	VOUT	-0.5 to Vdd +0.5	V

Note:

Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 PANEL DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD	-	VDD	2.6	3.0	3.6	V
High level input voltage	VIH	-	-	0.8Vdd	-	-	V
Low level input voltage	VIL	-	-	-	-	0.2Vdd	V
High level output voltage	VOH	IOH = -100uA	-	0.9Vdd	-	-	V
Low level output voltage	VOL	IOL = 100uA	-	-	-	0.1Vdd	V
OTP Program voltage	VPP	-	VPP	-	8.25	-	V
Typical power panel	PTYP	-	-	-	9	-	mW
Deep sleep mode	PSTPY	-	-	-	3	-	uW
Typical operating current	Iopr_VDD	Vdd=3.0V	-	-	3	-	mA
Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	27	-	uA

Deep sleep mode current	Idslp_VDD	VDD=3.0V DC/DC OFF No clock No output Load Ram data not retain	VDD	-	1	-	uA
Operation temperature range	TOPR	-	-	0	-	50	°C
Operation illuminance intensity	E	Indoor only	-	-	-	2000	lux
Storage temperature range	TSTG	-	-	-25	-	60	°C
Storage relative humidity	RHst	-	-	30	-	60	%RH

Note:

6-2-1: The typical power is measured with following transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.

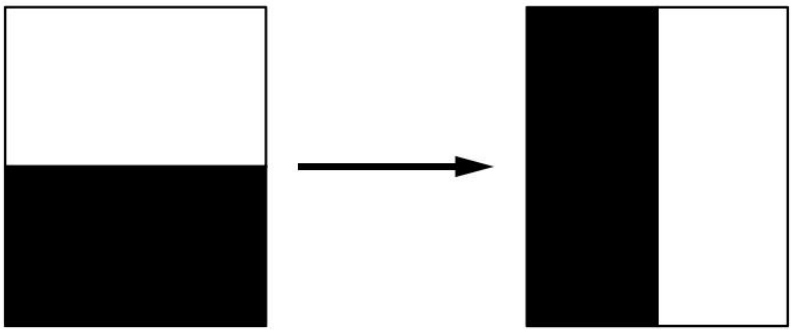


Figure 6-2 Typical power consumption measurement pattern

6-2-2: The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

6-2-3: The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

6.3 PANEL DC CHARACTERISTICS (DRIVER IC INTERNAL REGULATORS)

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR}=25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-3.0	-	-0.2	V

6.4 PANEL AC CHARACTERISTICS

6-4-1 MCU Interface Selection

The MCU interface consists of 2 data/command pins and 3 control pins. The pin assignment at different interface modes is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CSB	D/C	RSTN
4-wire SPI4	SDIN	SCLK	CSB	D/C	RSTN
3-wire SPI3	SDIN	SCLK	CSB	L	RSTN

Table 6-4-1: MCU interface assignment under different bus interface modes

6-4-2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

Function	CSB	D/C	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table 6-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

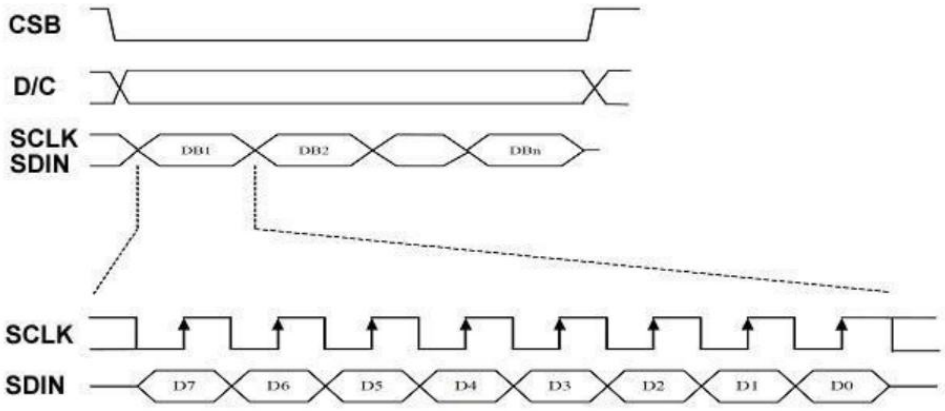


Figure 6-4-2: Write procedure in 4-wire SPI mode

6-4-3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9 bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

Table 6-4-3: Control pins of 3-wire Serial Interface

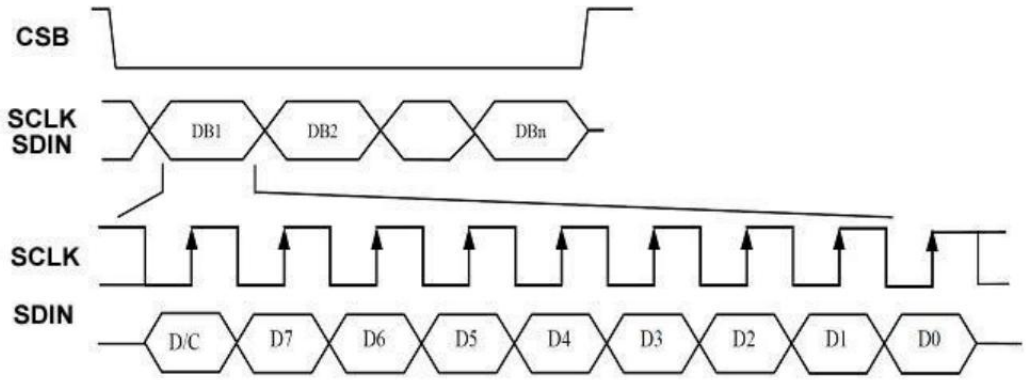


Figure 6-4-3: Write procedure in 3-wire Serial Peripheral Interface mode

6-4-4 Interface Timing

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25ºC

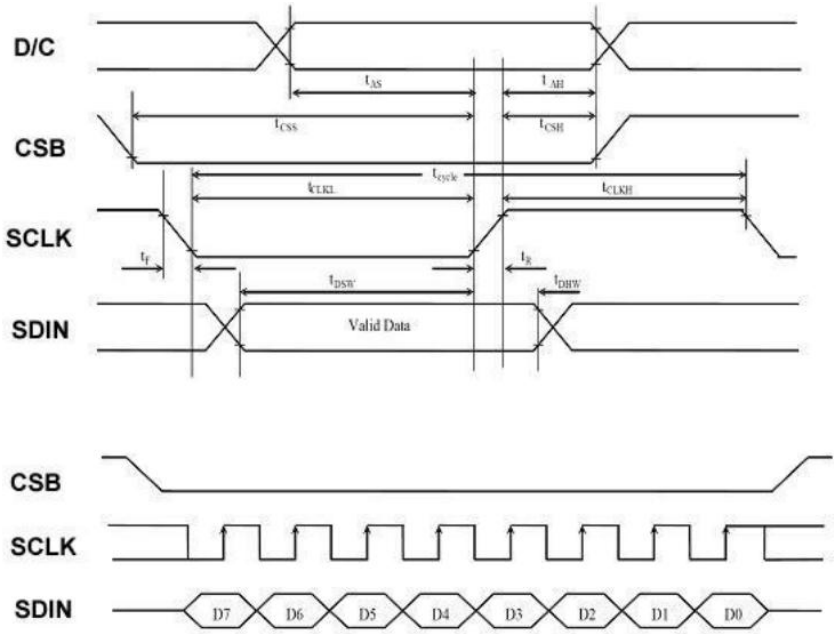


Figure 6-4-4: Serial interface characteristics

Vdd - VSS = 2.4V to 3.3V, TOPR = 25°C, CL=20pF

Symbol	Parameter	Min.	Typ.	Max.	Unit
tcycle	Clock Cycle Time	250	-	-	ns
tAS	Address Setup Time	150	-	-	ns
tAH	Address Hold Time	150	-	-	ns
tCSS	Chip Select Setup Time	120	-	-	ns
tCSH	Chip Select Hold Time	60	-	-	ns
tDSW	Write Data Setup Time	50	-	-	ns
tDHW	Write Data Hold Time	15	-	-	ns
tCLKL	Clock Low Time	100	-	-	ns
tCLKH	Clock High Time	100	-	-	ns
tR	Rise Time [20% ~ 80%]	-	-	15	ns
tF	Fall Time [20% ~80%]	-	-	15	ns

Table 6-4-4: Serial Interface Timing Characteristics

7. OPTICAL SPECIFICATION

Measurements are performed when the illumination is under an angle of 45 degrees, and the detection results are obtained perpendicularly unless otherwise specified.

Symbol	Parameter	Condition	Value			Unit	Note
			Min.	Typ.	Max.		
R	White Reflectivity	White	30	35	-	%	7-1
CR	Contrast Ratio		8:1	10:1	-	-	7-2
White△L 24h	Reduce		-	≤4	-	-	-

Note:

7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixels/Surface Reflectance with all black pixels.

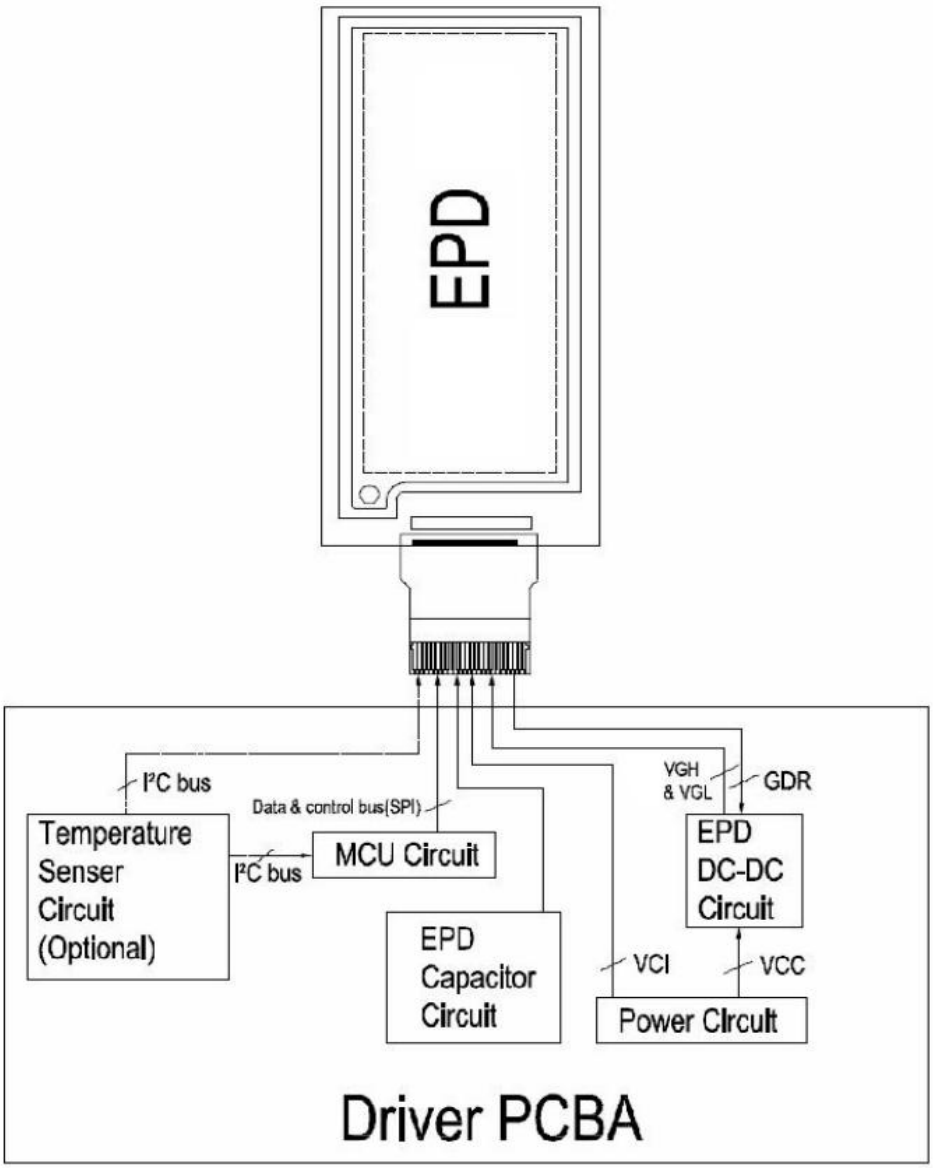
8. HANDLING, SAFETY, AND ENVIRONMENT REQUIREMENTS

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15ºC to 35ºC, and humidity from 30%RH to 60%RH.

9. RELIABILITY TEST

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
4	Low-Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 240hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
7	Thermal Shock	1 cycle:[-25°C 30min] → [+70°C 30min] : 100 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence:1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied

10. BLOCK DIAGRAM



11. TYPICAL APPLICATION CIRCUIT WITH SPI INTERFACE