



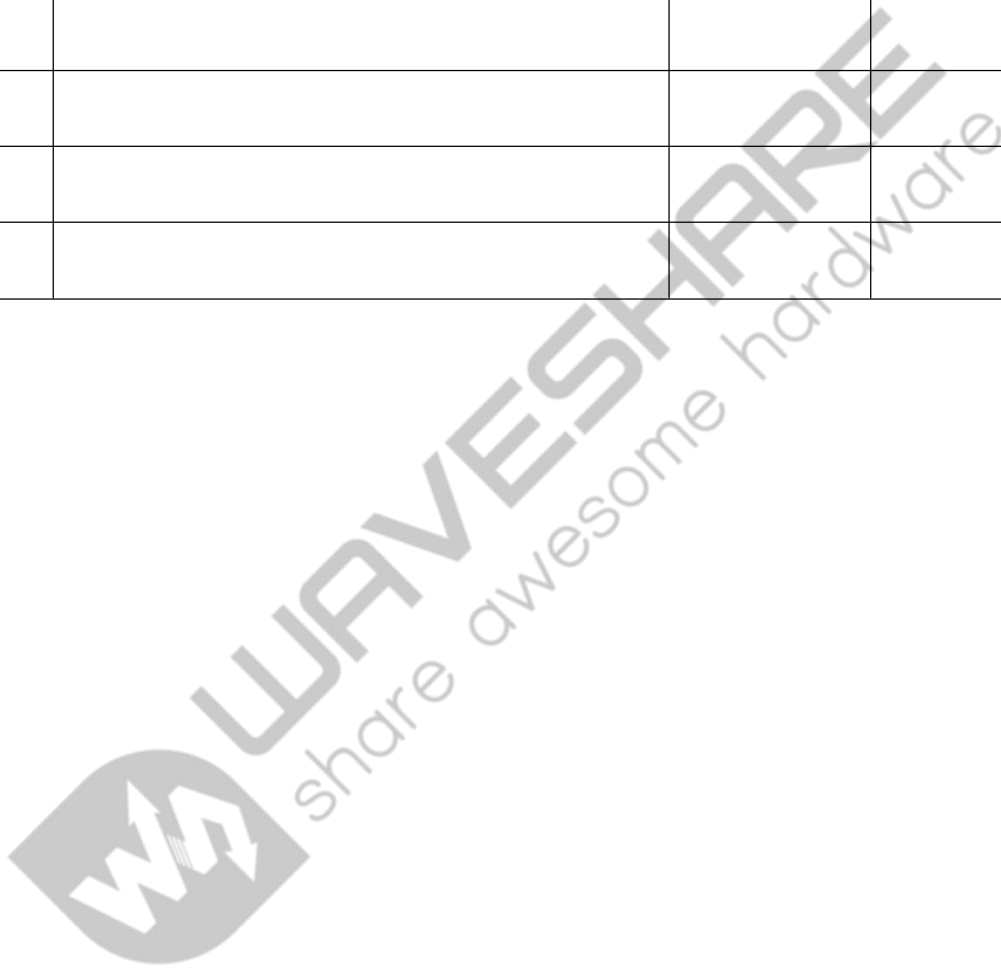
3.6inch e-Paper HAT+

User Manual



Revision History

Version	Content	Date	Page
1.0	New creation	2025/10/20	All



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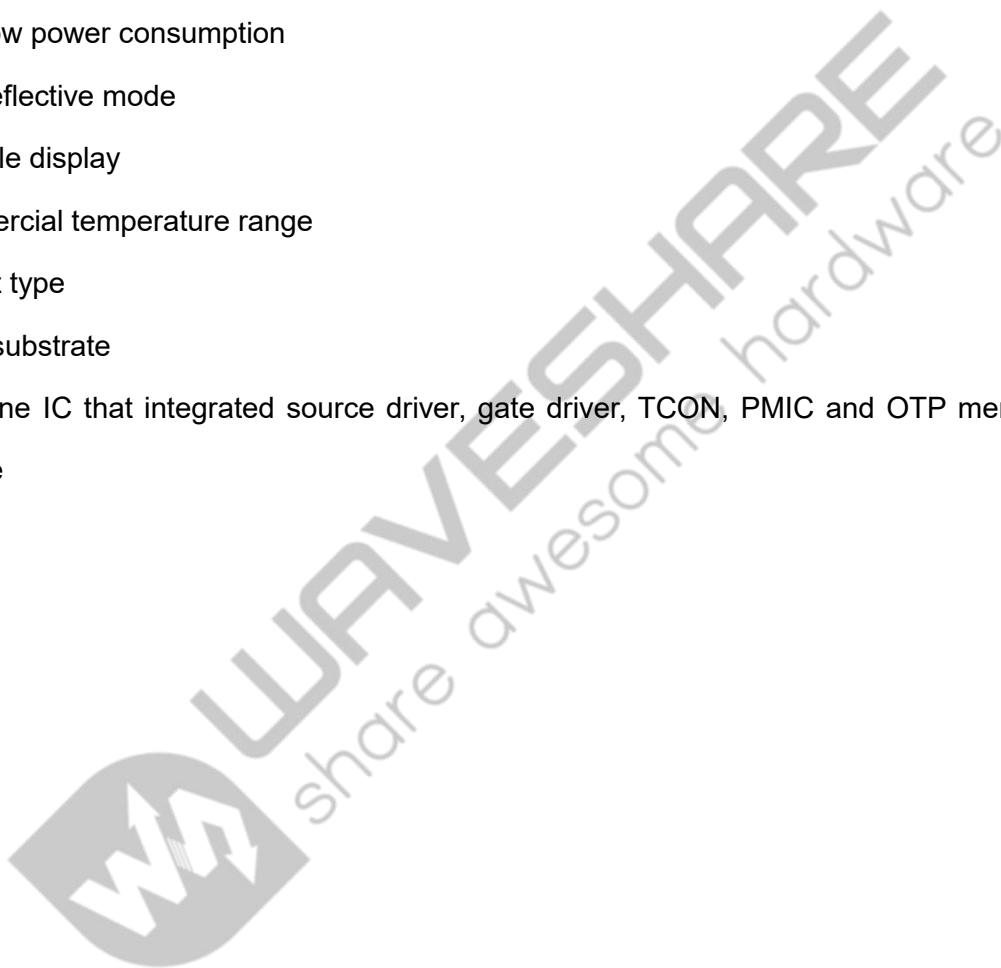
1. OVERVIEW

The display is a reflective electrophoretic display module based on glass active matrix TFT substrate. It has 3.6" active area with 400(H) x 600(V) pixels. The panel can display vivid colors that include black, white, yellow, red, green and blue depending on the associated lookup table used. The display is capable of displaying full-color images driven by the all-in-one display controller and the associated waveform file.



2. FEATURES

- ✧ High contrast reflective / electrophoretic technology
- ✧ 400(H) x 600(V) display
- ✧ Full color
- ✧ Ultra-wide viewing angle
- ✧ Ultra-low power consumption
- ✧ Pure reflective mode
- ✧ Bi-stable display
- ✧ Commercial temperature range
- ✧ Portrait type
- ✧ Glass substrate
- ✧ All-in-one IC that integrated source driver, gate driver, TCON, PMIC and OTP memory in the module



3. MECHANICAL SPECIFICATIONS

Parameter	Specifications	Unit	Remark
Screen Size	3.6	Inch	
Display Resolution	400(H)×600(V)	Pixel	
Active Area	50.8(H)×7.2(V)	mm	
Pixel Pitch	0.127(H)×0.127(V)	mm	200PPI
Pixel Configuration	Square		
Outline Dimension	56.0(H)×86.6(V)×0.74(D)	mm	w/o PF
Module Weight	TBD	g	
Display Operating Mode	Reflective mode		
Surface Treatment	AG		

5. PIN ASSIGNMENT

NO.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	TFT_VCOM	P	TFT_VCOM driving voltage	
3	FPL_VCOM	P	FPL_VCOM driving voltage	
4	NC		NC	
5	GDRH	I/O	N-Channel MOSFET Gate Drive Control	
6	RESEH	I/O	Current Sense Input for the Control Loop	
7	GDRL		Reserved	
8	GND	P	Ground	
9	GDRC	I/O	P-Channel MOSFET Gate Drive Control	
10	RESEC	I/O	Current Sense Input for the Control Loop	
11	VPC	P	VPC driving voltage	
12	GND	P	Ground	
13	VGL	P	Negative Gate driving voltage	
14	VPH	P	VPH driving voltage	
15	VSH	P	Positive Source driving voltage	
16	VSH_LV	P	Positive Source driving voltage	
17	VSH_LV2	P	Positive Source driving voltage	
18	VSL	P	Negative Source driving voltage	
19	VSL_LV	P	Negative Source driving voltage	
20	VSL_LV2	P	Negative Source driving voltage	
21	GNDA	P	Ground; Connect to GND	
22	REFN		Reserved	
23	REFP		Reserved	
24	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
25	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
26	BS0	I	Bus selection pin; L: 4-wire IF. H: 3-wire IF. (Default)	
27	BS1	I	Bus selection pin; L: refer to BS0. (Default) H: Standard 4-wire SPI/dual SPI/quad SPI	
28	RES#	I	Reset	
29	BUSY_N	O	Busy state output pin	
30	D/C#	I	Data/Command control pin (D/C)	
31	CS#	I	Chip Select input pin (CSB)	
32	SCL	I	Serial clock pin (SPI)	
33	SI0	I/O	Serial data pin (SPI)	
34	SI1	I/O	Serial data pin; Reserved	
35	SI2	I/O	Serial data pin; Reserved	
36	SI3	I/O	Serial data pin; Reserved	

37	VDDDO	P	Core logic power pin; Connect to VDDD	
38	VDD	P	Supply voltage	
39	GND	P	Ground; Connect to GNDA	
40	VDDIO	P	Supply voltage	
41	VCP2	P	Charge Pump Pin	
42	CP2N	P	Charge Pump Pin	
43	CP2P	P	Charge Pump Pin	
44	VCP1	P	Charge Pump Pin	
45	CP1N	P	Charge Pump Pin	
46	CP1P	P	Charge Pump Pin	
47	CGH1N		Charge Pump Pin; Reserved	
48	CGH1P		Charge Pump Pin; Reserved	
49	VGH	P	Positive Gate driving voltage	
50	VCOMBD	P	VCOMBD driving voltage	

Notes:

- 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.
- 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.
- 5-3: This pin (RES#) is reset signal input. The Reset is active Low.
- 5-4: This pin (BUSY_N) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:
- Outputting display waveform; or
 - Programming with OTP
 - Communicating with digital temperature sensor
- 5-5: This pin (BS0) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-line serial peripheral interface (SPI)
H	3-line serial peripheral interface (SPI) - 9 bits SPI

6. TYPICAL APPLICATION CIRCUIT

