3.97inch e-Paper

User Manual

Revision History

Version	Content	Date	Page
1.0	New creation	2025/04/24	All

Contents

1. OVERVIEW

The display is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The display is capable to display image at 1-bit white and black full display capabilities. The 3.97inch active area contains 800x480 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, and VCOM. The module can be used in portable electronic devices, such as Electronic Shelf Label(ESL) System.

2. FEATURES

- 800 × 480 pixels display
- High contrast and high reflectance
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape and portrait modes
- Hard-coat anti-glare display surface
- Ultra-low current deep sleep mode
- On-chip display RAM
- The waveform can be stored in on-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor
- Built-in temperature sensor

3. MECHANICAL AND OPTICAL SPECIFICATIONS

Parameter	Specifications	Unit	Remark
Screen Size	3.97	Inch	
Display Resolution	800(V)×480(H)	Pixel	DPI:235
Active Area	86.40×51.84	mm	
Pixel Pitch	0.108×0.108	mm	
Pixel Configuration	Rectangle		
Outline Dimension	56.24(H)×96.62(V)×0.92(D)	mm	
Weight	10.44±0.5	g	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Note
KS	Black State L* value		-	24	30		3-1
WS	White State L* value		58	62	-		3-1
	White Ghosting ΔL	Full Display Mode	-	1	-		3-1
		Partial Display Mode	-	1	-		3-1
		Full-Partial Display Mode	-	1	-		3-1
R	White Reflectivity	White	26	30	-	%	3-1
CR	Contrast Ratio	Indoor	5	7	-		3-1 3-2
GN	2Grey Level	-	-	-	-		
Life		Temp: 23±3℃ Humidity: 55±10%RH		5years			3-3

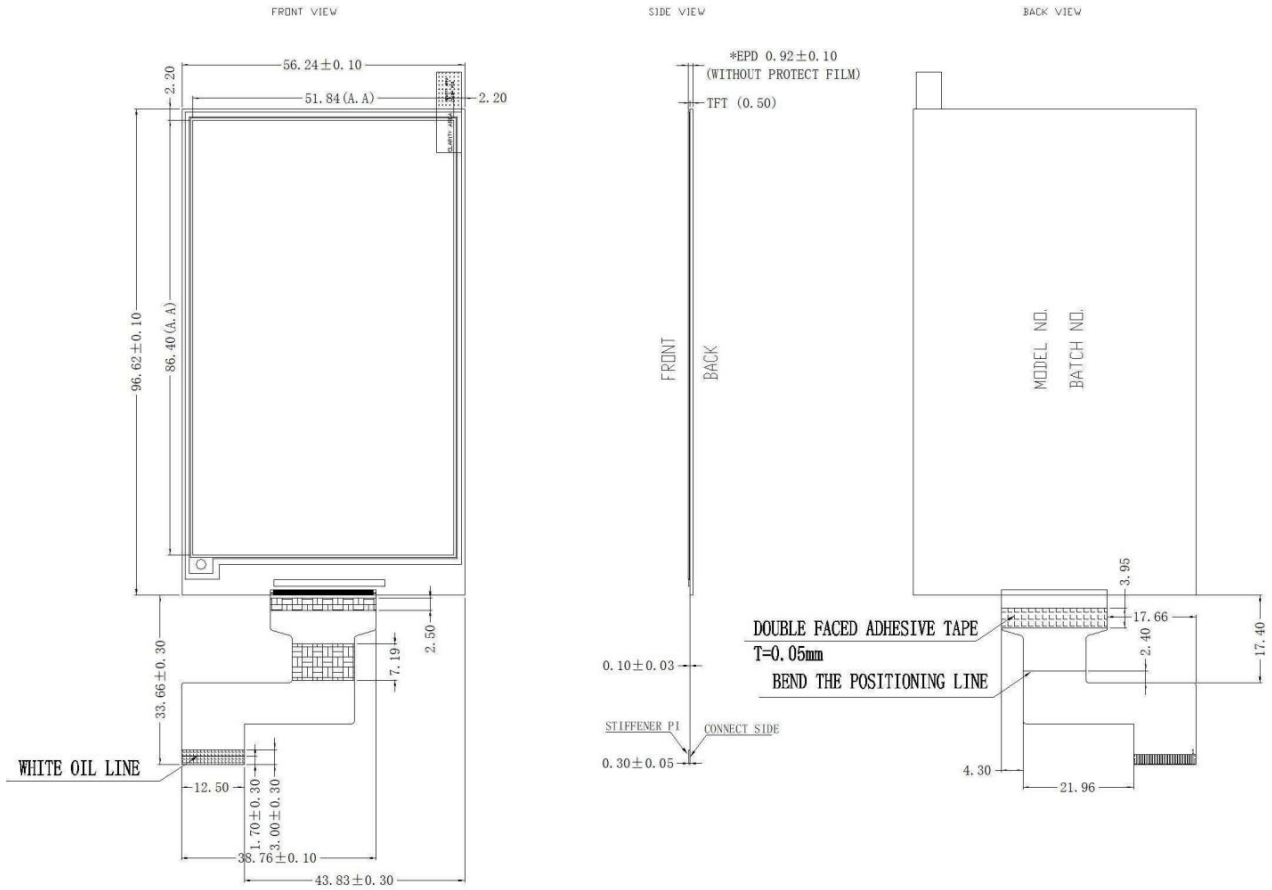
Notes:

3-1: Luminance meter: Eye-One Pro Spectrophotometer.

3-2: CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3: When the product is stored, the display screen should be kept white and face up.

4. MECHANICAL DRAWING OF EPD MODULE



Notes:

4-1: Display module 3.97″ array for EPD;

4-2: Driver IC: SSD1677;

4-3: Resolution: 800gate×480source;

4-4: Pixel size: 0.108mm×0.108mm.

5. PIN ASSIGNMENT

NO.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep open
5	VDHR	C	Positive Source driving voltage	
6	NC		Do not connect with other NC pins	
7	NC		Do not connect with other NC pins	
8	BS	I	Bus Interface selection pin	Note 5-5
9	BUSY_N	O	Busy state output pin	Note 5-4
10	RST_N	I	Reset signal input. Active Low	Note 5-3
11	DC	I	Data / Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins. It should be connected with VCI	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep open
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O = Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Notes:

5-1: This pin(CS#) is the chip select input pin connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

5-2: This pin(D/C#) is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will

be interpreted as command.

5-3: This pin(RES#) is reset signal input pin. The Reset is active low.

5-4: This pin is Busy state output pin. When Busy is High, the operation of the chip should not be interrupted, the command should not be sent. The chip would put Busy pin High when

- Outputting display waveform
- Communicating with digital temperature sensor

5-5: Bus interface selection pin.

BS1 State	MCU Interface
L	4-line serial peripheral interface(SPI) - 8 bits SPI
H	3-line serial peripheral interface(SPI) - 9 bits SPI

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CI}, V_{DDIO}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to V_{DDIO} +0.5	V
Logic Output voltage	V_{OUT}	-0.5 to V_{DDIO} +0.5	V
Operating Temp range	T_{OPR}	0 to +50	℃
Storage Temp range	T_{STG}	-25 to +70	℃
Optimal Storage Humidity	H_{STGO}	55±10	%RH

Notes:

6-1-1: Maximum ratings are those values beyond which damages to the device may occur. Functional operations should be restricted to the limits in the Panel DC Characteristics table.

6-1-2: The display screen should be kept white and face up during storage. Please refer to the Reliability Test section.

6.2 PANEL DC CHARACTERISTICS

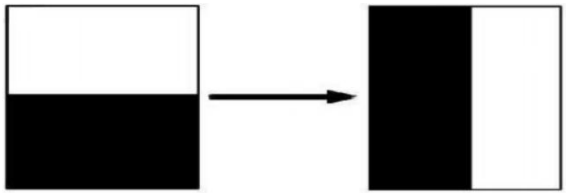
The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, T_{OPR} =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-	-	-	0	-	V
Logic supply voltage	V_{CI}	-	V_{CI}	2.2	3.0	3.3	V
Power for interface logic pins	V_{DDIO}	-	V_{DDIO}	2.2	-	3.3	V
Core logic voltage	V_{DD}	-	V_{DD}	1.7	1.8	1.9	V
VCOM DC output voltage	V_{COM}	-	V_{COM}	-4.0	-	-0.1	V
High level input voltage	V_{IH}	-	-	0.8V_{DDIO}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2V_{DDIO}	V
High level output voltage	V_{OH}	I_{OH} = -100 μ A	-	0.9V_{DDIO}	-	-	V
Low level output voltage	V_{OL}	I_{OL} = 100 μ A	-	-	-	0.1V_{DDIO}	V
Typical power	P_{TYP}	V_{CI}=3.0V	-	-	36	-	mW
Deep sleep mode	P_{STPY}	V_{CI}=3.0V	-	-	0.003	-	mW

Typical operating current	$I_{opr}\_V_{CI}$	V_{CI}=3.0V	-		12	-	mA
Full update time	-	23℃	-		3	-	sec
Fast update time	-	23℃	-		1.5	-	sec
Partial update time	-	23℃	-		0.3	-	sec
4-Greys update time	-	23℃	-		3	-	sec
Typical peak current	$I_{opr}\_V_{CI}$	2.3～3.6℃	-	-	120	-	mA
Deep sleep mode current	$I_{dslp}\_V_{CI}$	DC/DC OFF No clock No input load Ram data not retain	-	-	1	5	μA

Notes:

6-2-1: The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



6-2-2: The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

6-2-3: The listed electrical characteristics are only guaranteed under the controller & waveform provided by Waveshare.

6-2-4: Electrical measurement: Tektronix oscilloscope - MDO3014,
Tektronix current probe - TCP0030A.

6.3 PANEL AC CHARACTERISTICS

The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, T_{OPR} =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{COM} output voltage	V_{COM}	V_{CI}=3.0V Enable Clock and Analog by Master Activation Command V_{GH}=20V V_{GL}=-V_{GH} V_{SH1}=15V V_{SH2}=5V V_{SL}=-15V V_{COM}=-2V	V_{COM}	-2.2	-2	-1.8	V
Positive Source output voltage	V_{SH}		S_0～S_{127}	+14.8	+15	+15.2	V
Negative Source output voltage	V_{SL}		S_0～S_{127}	-15.2	-15	-14.8	V
Positive gate output voltage	V_{GH}		G_0～G_{295}	+19.5	+20	+20.5	V
Negative gate	V_{GL}		G_0～G_{295}	-20.5	-20	-19.5	V

output voltage		No waveform transitions No loading No RAM read/write No OTP read/write					

6.4 MCU INTERFACE

6.4.1 MCU Interface Selection

The pin assignment at different interface modes is summarized in Table 6-4-1. Different MCU modes can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 6-4-1: MCU interface assignment under different bus interface modes

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table 6-4-2: Control pins of 4-wire Serial Peripheral Interface

In the Write mode:
SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

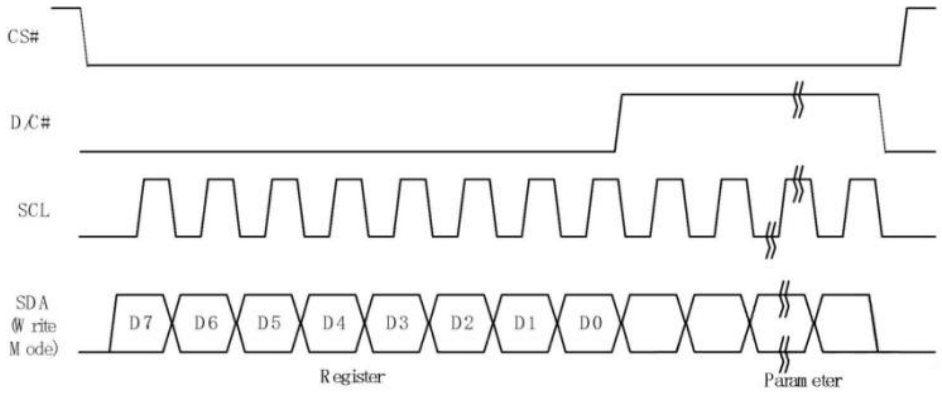


Figure 6-1: Write procedure in 4-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

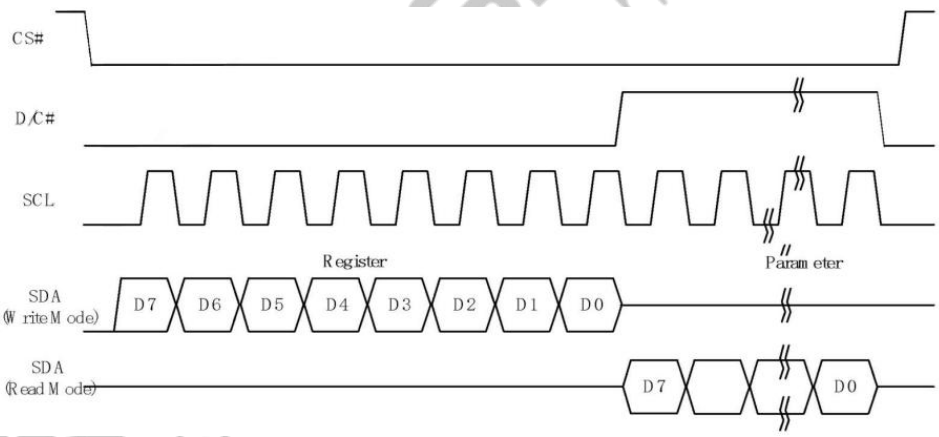


Figure 6-2: Read procedure in 4-wire SPI mode

6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9 bits that will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit.

The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit=1) or the command register (D/C# bit=0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

Table 6-4-3: Control pins of 3-wire Serial Peripheral Interface

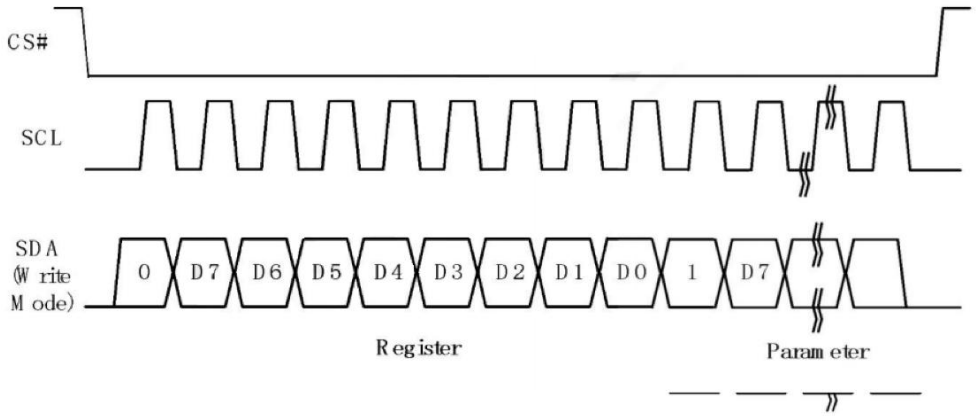


Figure 6-3: Write procedure in 3-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL.
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL.
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

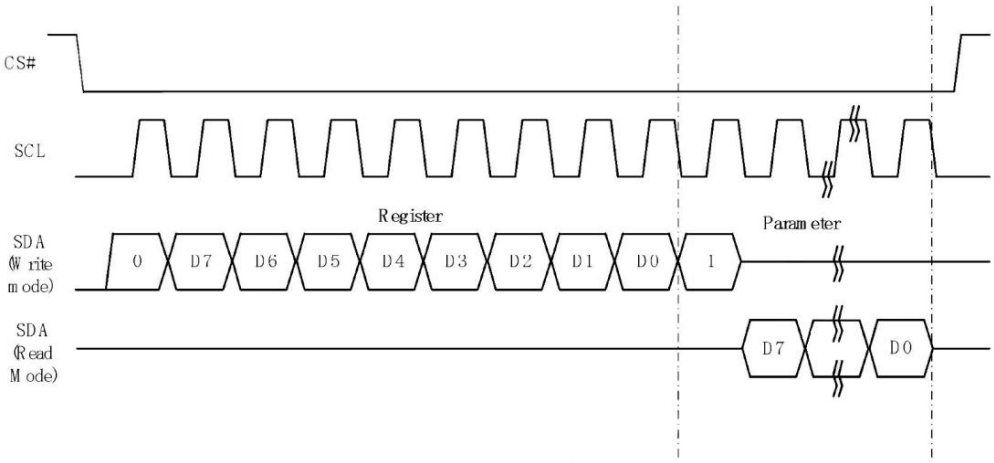
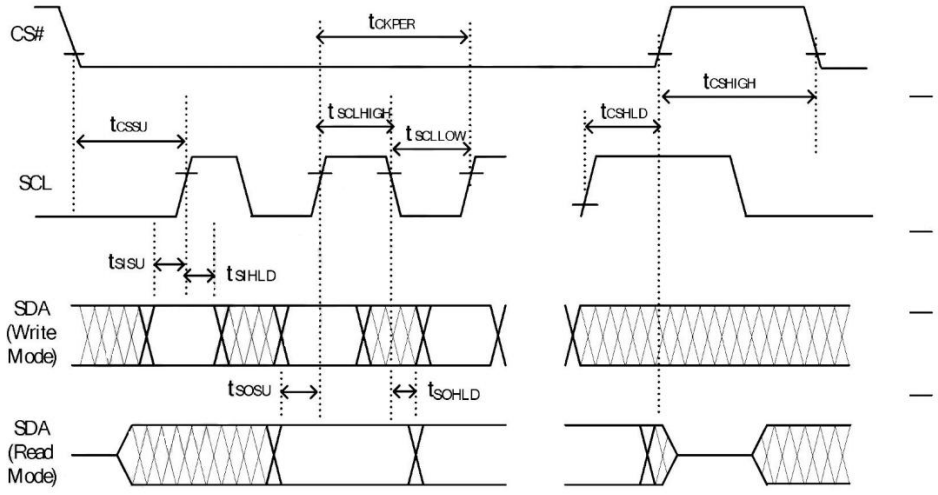


Figure 6-4: Read procedure in 3-wire SPI mode

6.4.4 Interface Timing

The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, T_{OPR} =23°C.



Changed Diagram

Serial Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.2V to 3.7V, T_{OPR} = 23℃, CL = 30pF)

Write mode:

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SCL}	SCL frequency (Write Mode)			20	MHz
T_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	20			ns
T_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	20			ns

T_{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
T_{SCLCYC}	SCL cycle time	50			ns
$T_{SCLHIGH}$	Part of the clock period where SCL has to remain high	25			ns
T_{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
T_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
T_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the next rising edge of SCL	40			ns

Read mode:

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SCL}	SCL frequency (Read Mode)			2.5	MHz
T_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
T_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
T_{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
$T_{SCLHIGH}$	Part of the clock period where SCL has to remain high	180			ns
T_{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
T_{SOSU}	Time SO (SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
T_{SOHLD}	Time SO (SDA Write Mode) will remain stable after the rising edge of SCL		0		ns

7. COMMAND TABLE

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting Set A[9:0]=2A7h[POR] ,680MUX Set B[2:0]=000[POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		
0	1		0	0	0	0	0	B2	B1	B0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage control	SetGate Driving voltage A[4:0]=17h[POR],VGH at 20V[POR] VGH setting from 12V to 20V
0	1		0	0	0	A4	A3	A2	A1	A0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage control	SetSource Driving voltage A[7:0]= 41h[POR],VSH1 at 15V B[7:0]=A8h[POR],VSH2 at 5.0V C[7:0]= 32h[POR], VSL at -15V
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control A[1:0] : Description 00 Normal Mode [POR] 11 Enter Deep Sleep Mode After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.
0	1		0	0	0	0	0	0	A_1	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0]Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 – Y decrement, X decrement, 01 – Y decrement, X increment, 10 – Y increment, X decrement, 11 – Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		

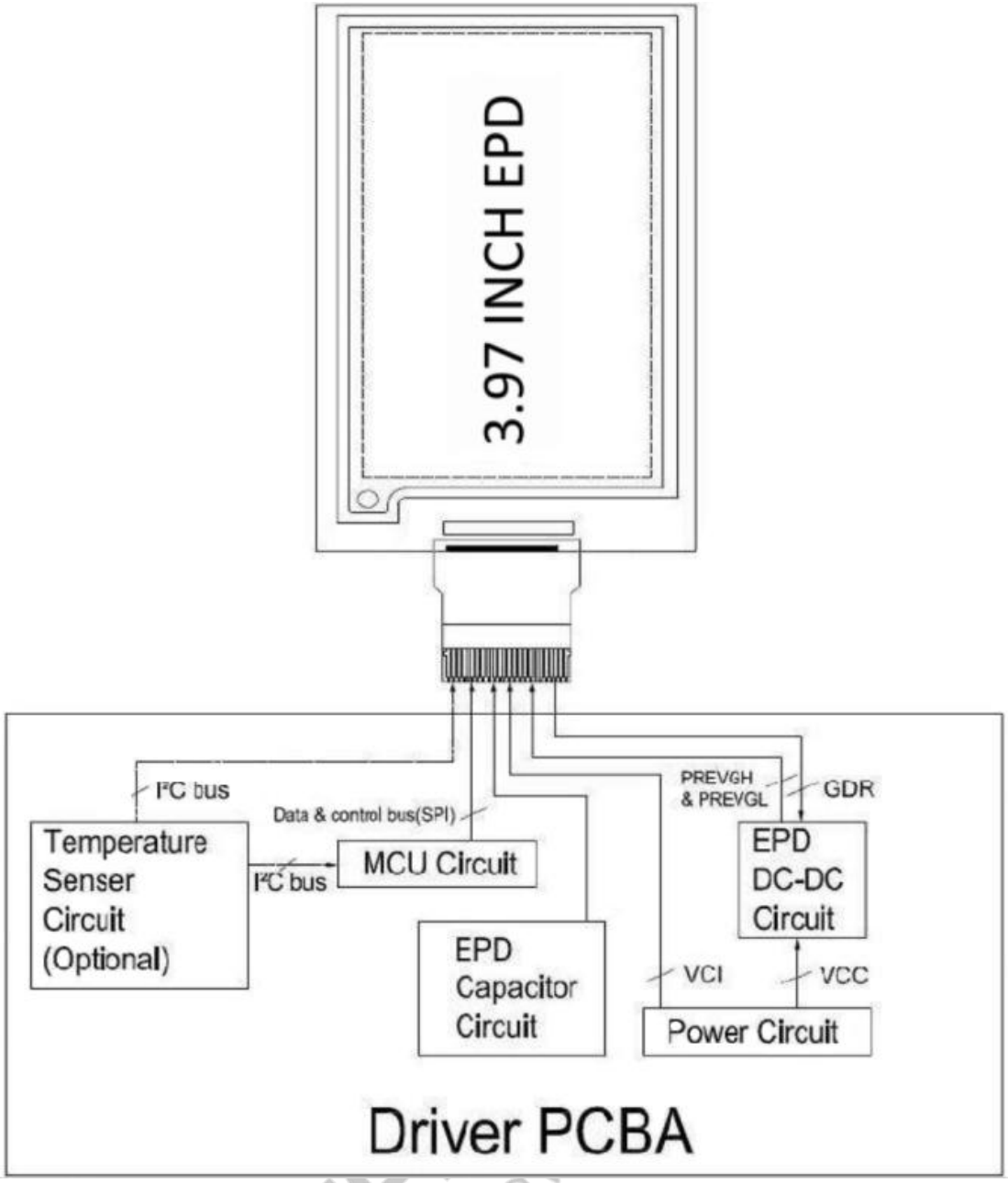
<table>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>SWRESET</td><td>It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode
During operation ,BUSY pad will output high.
Note: RAM are unaffected by this command.</td></tr>
<tr><td>0</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Temperature Sensor Control</td><td rowspan="2">Temperature Sensor Selection
A[7:0] = 48h [POR], external temperature sensor
A[7:0] = 80h Internal temperature sensor</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="3">Temperature Sensor Control (Write to temperature register)</td><td rowspan="3">Write to temperature register.
A[11:0]=7FFh[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A11</td><td>A10</td><td>A9</td><td>A8</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence
The Display Update Sequence Option is located at R22h
User should not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Display Update Control 1</td><td rowspan="2">RAM content option for Display Update
A[7:0]=00h[POR]
A[7:4] Red RAM option
0000 Normal
0100 Bypass RAM content as 0
1000 Inverse RAM content

A[3:0] BW RAM option
0000 Normal
0100 Bypass RAM content as 0
1000 Inverse RAM content</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation
Setting for LUT from MCU
Enable Clock Signal,
Then Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC
C7
Setting for LUT from OTP according to external Temperature Sensor operation
Then Enable Analog
Then Load LUT
90
Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC
47</td></tr>
<tr><td></td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

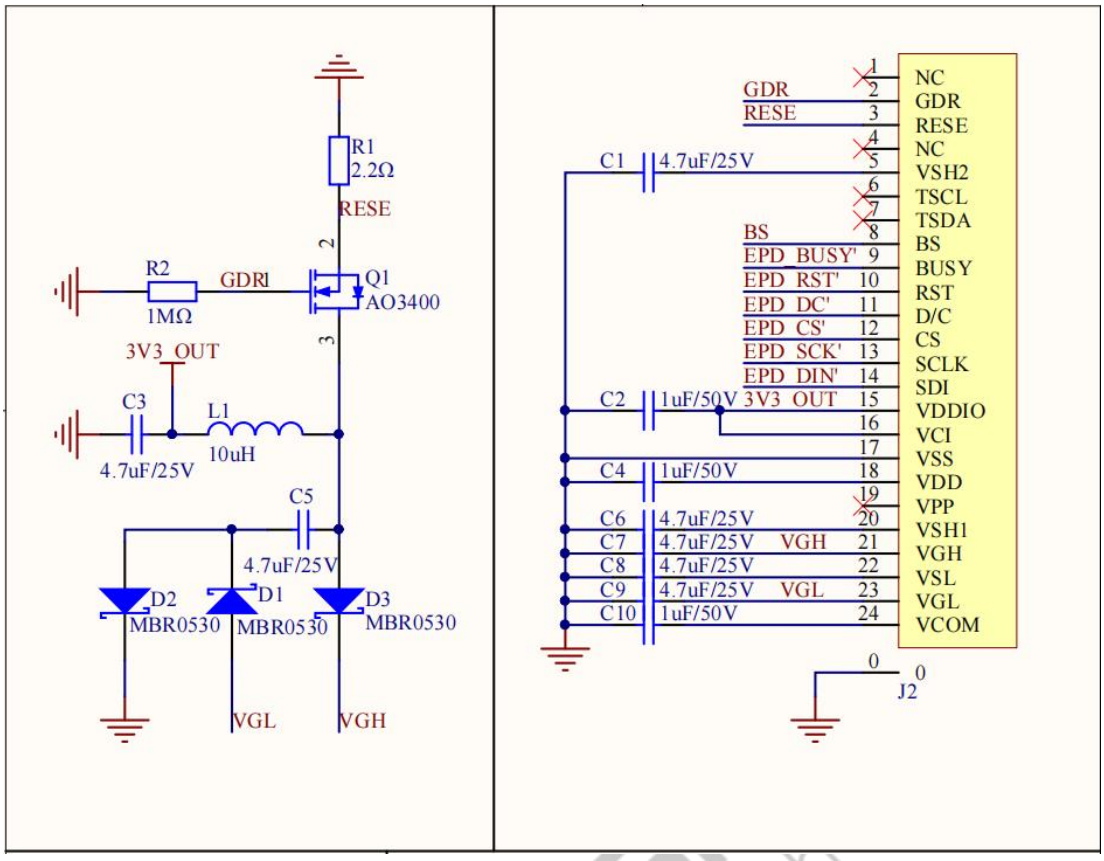
0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the 2 RAM until another command is written. Address pointers will advance accordingly. For RED pixel: Content of write RAM(RED)=1 For White/Black pixel: Content of write RAM(RED)=0
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=50h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read	Read Register stored in OTP: 1. A[7:0]~ B[7:0]: VCOM Information 2. C[7:0]~G[7:0]:Display mode 3. H[7:0]~K[7:0]: Waveform Version [4bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
1	1		K7	K6	K5	K4	K3	K2	K1	K0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x21] A[5]: HV Ready Detection flag [POR=1] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A5	A4	0	0	A1	A0		
0	0	32	0	0	1	1	0	0	1	0	Write LUT	Write LUT register from MCU interface

<table>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>register</td><td>[105 bytes].</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Border Waveform Control</td><td>Select border waveform for VBD
A [7:0]=C0h[POR],set VBD as HIZ
A [7:6] Select VBD option<table><tr><td>A[7:6]</td><td>Select VBD as</td></tr><tr><td>00</td><td>GS Transition
Define A[1:0]</td></tr><tr><td>01</td><td>Fix Level
Define A [5:4]</td></tr><tr><td>10</td><td>VCOM</td></tr><tr><td>11[POR]</td><td>HIZ</td></tr></table>A [5:4] Fix Level Setting for VBD<table><tr><td>A[5:4]</td><td>VBD level</td></tr><tr><td>00[POR]</td><td>VSS</td></tr><tr><td>01</td><td>VSH1</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11</td><td>VSH2</td></tr></table>A[1:0]) BW Transition setting for VBD<table><tr><td>A[1:0]</td><td>VBD Transition</td></tr><tr><td>00 [POR]</td><td>LUT0</td></tr><tr><td>01</td><td>LUT1</td></tr><tr><td>10</td><td>LUT2</td></tr><tr><td>11</td><td>LUT3</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Set RAM X - address Start / End position</td><td>Specify the start/end positions of the window address in the X direction by an address unit
A[9:0]: XSA[9:0], X Start, POR = 000h
B[9:0]: XEA[9:0], X End, POR = 3BFh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B_9</td><td>B_8</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Set Ram Y-address Start / End position</td><td>Specify the start/end positions of the window address in the Y direction by an address unit
A[9:0]: YSA[9:0], Y Start, POR = 000h
B[9:0]: YEA[9:0], Y End, POR = 2A7h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B_9</td><td>B_8</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>4E</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Set RAM X address counter</td><td>Make initial settings for the RAM X address in the address counter (AC)
A[9:0]: 000h[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>4F</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Set RAM Y address counter</td><td>Make initial settings for the RAM Y address in the address counter (AC)
A[9:0]: 000h[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
</table>

8. BLOCK DIAGRAM



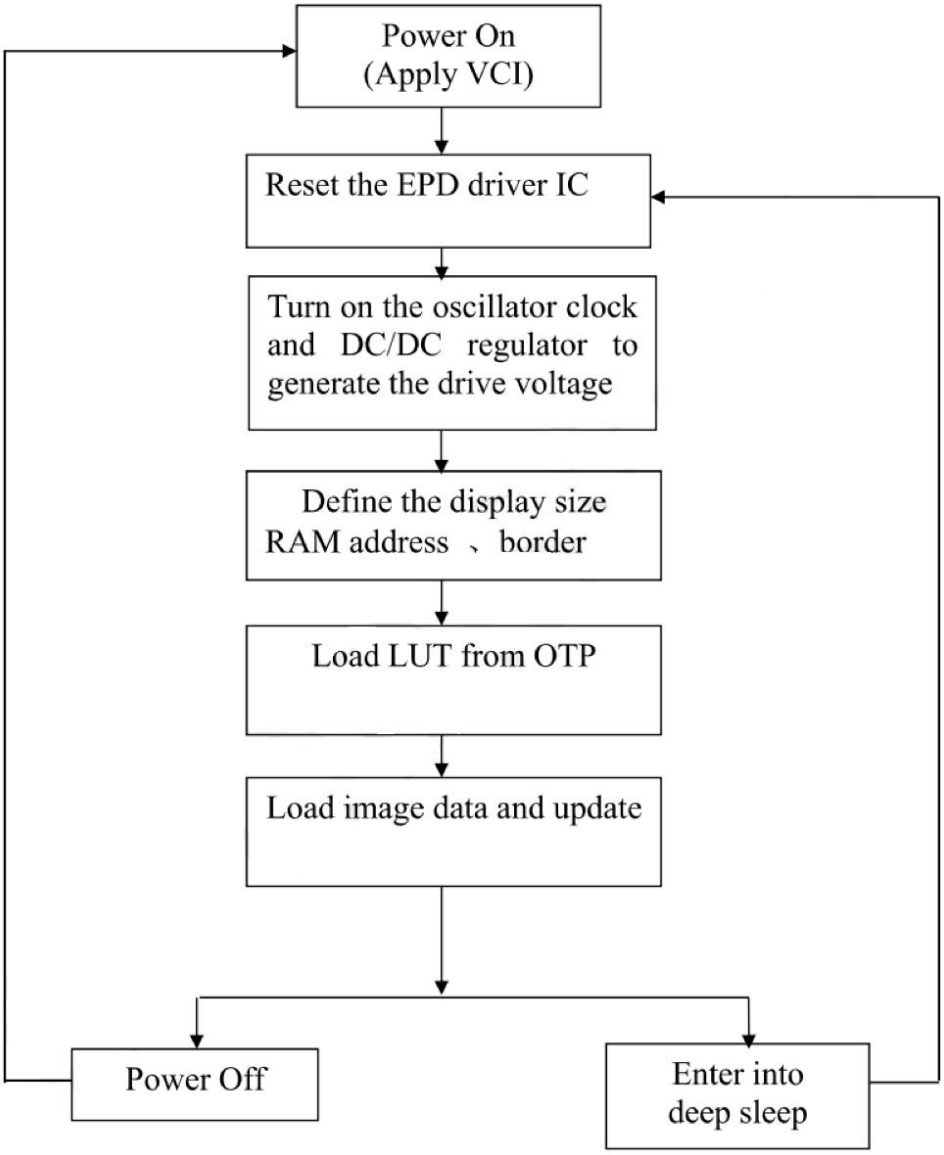
9. TYPICAL APPLICATION CIRCUIT WITH SPI INTERFACE



Part Name	Requirements for spare parts
C1—C12	0603/0805; X5R/X7R; Voltage Rating: ≥25V
R1, R2	0603/0805; 1% variation, ≥0.05W
D1—D3	MBR0530: 1) Reverse DC Voltage≥30V; 2) Io≥500mA; 3) Forward voltage ≤430mV
Q1	Si1308EDL:1) Drain-Source breakdown voltage ≥30V; 2) Vgs(th)≤1.5V; 3) Rds(on)≤400mΩ
L1	Refer to NR3015: Io=500mA(max)
P1	24pins, 0.5mm pitch

10. TYPICAL OPERATING SEQUENCE

10.1 LUT FROM OTP OPERATION FLOW



10.2 OTP OPERATION REFERENCE PROGRAM CODE

ACTION	VALUE/DATA	COMMENT
POWER ON 3v		
delay	10ms	
PIN CONFIG		
RES#	low	Hardware reset
delay	200us	
RES#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
Command 0x0C	Data 0xAE 0xC7 0xC3 0xC0 0x80	Booster Soft-start Control
Command 0x01	Data 0xDF 0x01 0x02	Set display size and driver output control
Command 0x11	Data 0x01	Ram data entry mode
Command 0x44	Data 0x00 0x00 0x1F 0x03	Set Ram X address
Command 0x45	Data 0xDF 0x01 0x00 0x00	Set Ram Y address
Command 0x3C	Data 0x01	Set border
Command 0x18	Data 0x80	
LOAD IMAGE AND UPDATE		
Command 0x4E	Data 0x00 0x00	Set Ram X address counter
Command 0x4F	Data 0xDF 0x01	Set Ram Y address counter
Command 0x24	48000 bytes	Load BW image (800/8*480)
Command 0x22	Data 0xF7	Image update
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

11. RELIABILITY TEST

No.	Test Items	Test Conditions
1	Low-Temperature Operation	0°C for 240hrs
2	High-Temperature, High-Humidity Storage	60°C/80% RH for 240hrs
3	Thermal Shock	1 cycle: -25°C/30min～60°C/30min for 100 cycles
4	High-Temperature, Low-Humidity Storage	60°C/35% RH for 240hrs
5	High-Temperature, High-Humidity Operation	40°C/80% RH for 240hrs
6	ESD Gun	Air+/-4KV; Contact+/-2KV Contact+/-2KV(HBMC: 100pF; R: 1.5k ohm) Contact+/-200V(MMC: 200pF; R: 0 ohm) (Naked EPD display, including IC and FPC area)
7	Vibration test	Frequency: 10-500Hz; Direction: X, Y, Z Duration: 1 hour in each direction
8	Dropping test	The test height is determined by the weight of the test object. Weight ≤20KG, drop height 1000mm Weight ≤50KG, drop height 500mm Weight ≤100KG, drop height 250mm

Notes:

11-1: Stay white pattern for storage and non-operation test.

11-2: The operation is black → white pattern, the interval is 150s.

12. QUALITY ASSURANCE

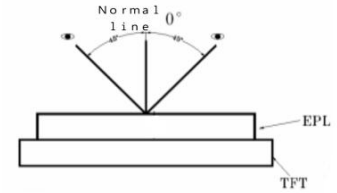
12.1 ENVIRONMENT

Temperature: 23±3℃; Humidity: 55±10%RH

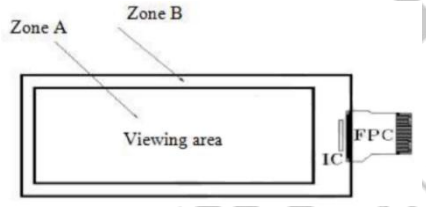
12.2 ILLUMINANCE

Brightness: 1200~1500LUX; Angle: Relate 45° surrounded; Distance: 20-30CM

12.3 INSPECTION METHOD

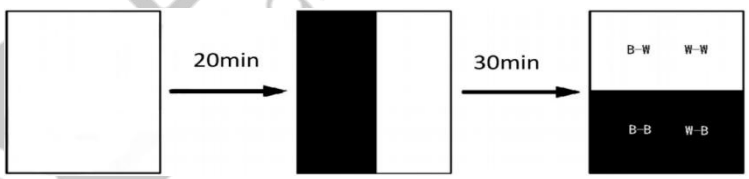


12.4 DISPLAY AREA



12.5 GHOSTING TEST METHOD

Two-color ghosting is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.



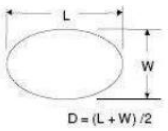
1) Measurement Instrument: X-rite i1Pro
2) Ghosting formula:

W ghosting: ΔL=Max(ΔL(W-W,B-W) - Min(ΔL(W-W,B-W)

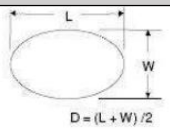
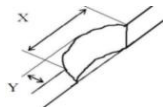
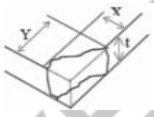
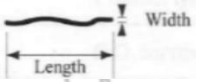
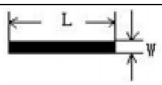
K ghosting: ΔL=Max(ΔL(W-B,B-B) - Min(ΔL(W-B,B-B)

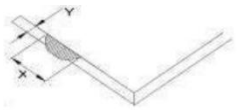
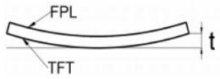
12.6 INSPECTION STANDARD

12.6.1 Electric Inspection Standards

No.	Item	Standard	Defect Level	Method	Scope
1	Display	Clear display; Display complete; Display uniform	MA	Visual inspection	Zone A
2	Black/Write spots	 D≤0.3mm, negligible; 0.3mm<D≤0.5mm, N≤7, allowed; 0.5mm<D≤0.7mm, N≤1, allowed; D>0.7mm, not allowed	MI	Visual/ Inspection card	Zone A
3	Black/White lines (No switch)	 L≤2.0mm, W≤0.2mm, negligible; 2.0mm<L≤8.0mm,0.2mm<W≤0.5mm, N≤4 allowable; L>8.0mm,W>0.5mm, not allowed	MI	Visual/ Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual	Zone A
5	Flash dot/ Multilateral	Flash points are allowed when switching screens; Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment	MA	Visual/ Inspection card	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not allowed	MA	Visual	Zone A
8	Corner mura	 X>1mm, Y>1mm, not allowed	MI	Visual/Ruler	Zone A

12.6.2 Appearance Inspection Standards

No.	Item	Standard	Defect Level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.3mm, negligible; 0.3mm<D≤0.5mm, N≤7, allowed; 0.5mm<D≤0.7mm, N≤1, allowed; D>0.7mm, not allowed	MI	Visual/ Inspection card	Zone A
2	Chips/Scratch/ Edge crown	 X≤3mm, Y≤0.5mm, t=not counted, and without affecting the electrode, permissible;  X≤2mm or Y≤2mm t=not counted, and without affecting the electrode, permissible;  W≤0.1mm, L≤5mm, without affecting the electrode, N≤2	MI	Visual /Ruler	Zone A/B
3	TFT cracks	 Not allowed	MA	Visual /Microscope	Zone A/B
4	Dirty/foreign body	Allowed if can be removed	MI	Visual /Clean cloth	Zone A/B
5	FPC broken/FPC oxidation/scratch	 Not allowed	MA	Visual /Microscope	Zone B
6	B/W line	 L≤2.0mm, W≤0.2mm, negligible; 2.0mm<L≤8.0mm, 0.2mm<W≤0.5mm, N≤4 allowable; L>8.0mm, W>0.5mm, not allowed	MI	Visual /Ruler	Zone A

7	TFT edge bulge/TFT chromatic aberration	 TFT edge bulge: X≤3mm, Y≤0.3mm, allowed; TFT chromatic aberration: Allowed	MI	Visual /Microscope	Zone A/B
8	Electrostatic point	D≤0.3mm, negligible; 0.3mm<D≤0.5mm, N≤4 allowed; D>0.5mm, not allowed; (N≤10 items are allowed within 5mm in diameter)	MI	Visual /Inspection card	Zone A
9	PCB damaged/ Poor welding/Curl	PCB (Circuit area) damaged: not allowed; PCB Poor welding: not allowed; PCB Curl≤1%	MA	Visual /Ruler	Zone B
10	Edge glue height/ Edge glue bubble	Edge adhesive H≤PS surface (including protective film); Edge adhesive overflow onto the protective film ≤1/2 FPL to PS Margin width Length excluding Edge adhesive seep in ≤1/2 FPL Margin width Length excluding Edge adhesive bubble: bubble width ≤1/2 Margin width; Length≤5.0mm. N≤5	MI	Visual /Ruler	Zone B
11	Protective film	Surface scratch but not effect protective function, allowed	MI	Visual	Zone A/B
12	Silicon glue	Thickness ≤PS surface (with protective film): Full cover the IC; Shape: The width on the FPC ≤1.0mm (front); The width on the FPC ≤1.0mm (back); Smooth surface, no obvious protrusion	MI	Visual /Ruler	Zone B
13	Wrap degree (TFT substrate)	 t ≤2.5mm	MI	Ruler	Zone B
14	Color difference in COM area (Silver point area)	Allowed	MI	Visual	Zone B
15	Corner and edge damage of FPL	 Corner and edge damage ≤1/2 border width	MI	Visual /Ruler	Zone A

13. HANDLING, SAFETY, AND ENVIRONMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

14. PRECAUTIONS

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.
(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
(5) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.