4.2inch e-Paper (B) V2

User Manual

Revision History

Version	Content	Date	Page
1.0	New creation	2025/02/21	All

Contents

1. OVERVIEW

4.2inch e-Paper (B) V2 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1 bit white, black and red full display capabilities. The 4.2inch active area contains 400 x 300 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. The module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) system.

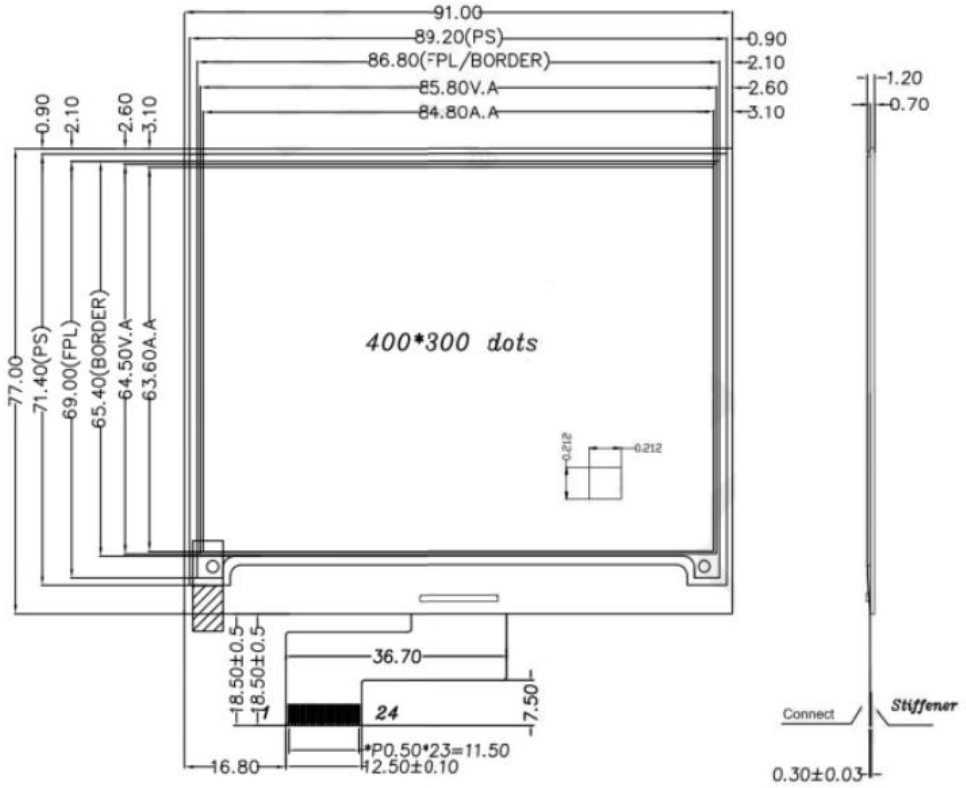
2. FEATURES

- ✧ 400 × 300 pixels display
- ✧ High contrast
- ✧ High reflectance
- ✧ Ultra wide viewing angle
- ✧ Ultra low power consumption
- ✧ Pure reflective mode
- ✧ Bi-stable display
- ✧ Commercial temperature range
- ✧ Landscape and portrait modes
- ✧ Hard-coat antiglare display surface
- ✧ Ultra low current deep sleep mode
- ✧ On-chip display RAM
- ✧ Waveform can be stored in on-chip OTP or written by MCU
- ✧ Serial peripheral interface available
- ✧ On-chip oscillator
- ✧ On-chip booster and regulator control for generating VCOM, gate and source driving voltage
- ✧ I2C signal master interface to read external temperature sensor
- ✧ Support partial update mode
- ✧ Built-in temperature sensor

3. MECHANICAL AND OPTICAL SPECIFICATIONS

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	DPI:132
Active Area	84.8×63.6	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Rectangle		
Outline Dimension	91(H)×77(V)×1.2(D)	mm	
Weight	16.1±0.3	g	

4. MECHANICAL DRAWING OF EPD MODULE



Notes:

4-1: Display mode: EPD, B/W/R;

4-2: Resolution ratio: 4.2″, 400 × 300;

4-3: Operating voltage: VCI=3.0V;

4-4: Operating temp: 0℃～40℃;

4-5: Storage temp: -25℃～60℃;

4-6: Controller/driver: SSD1683;

4-7: Unspecified tolerance: ±0.2;

4-8: RoHS compliant

5. PIN ASSIGNMENT

NO.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep open
5	VSH2	C	Positive Source driving voltage (Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low	Note 5-3
11	D/C#	I	Data / Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins. It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	GND	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O = Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Notes:

5-1: This pin(CS#) is the chip select input pin connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

5-2: This pin(D/C#) is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will

be interpreted as command.

5-3: This pin(RES#) is reset signal input. The Reset is active low.

5-4: This pin is Busy state output pin. When Busy is Low, the operation of the chip should not be interrupted, the command should not be sent. The chip would put Busy pin High when

- Outputting display waveform
- Communicating with digital temperature sensor

5-5: Bus interface selection pin

BS1 State	MPU Interface
L	4-line serial peripheral interface(SPI) - 8 bits SPI
H	3-line serial peripheral interface(SPI) - 9 bits SPI

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CI}	-0.5 to +6.0	V
Logic Input voltage	V_{IN}	-0.5 to VCI +0.5	V
Logic Output voltage	V_{OUT}	-0.5 to VCI +0.5	V
Operating Temp range	T_{OPR}	0 to +40	℃
Storage Temp range	T_{STG}	-25 to +60	℃
Optimal Storage Temp	T_{STGO}	23±2	℃
Optimal Storage Humidity	H_{STGO}	55±10	%RH

Notes:

(1). Maximum ratings are those values beyond which damages to the device may occur. Functional operations should be restricted to the limits in the Panel DC Characteristics table.

(2). One pixel fonts visual readability: 0℃～40℃.

(**3).** Corner mura could be out in 0℃～10℃ conditions.

6.2 PANEL DC CHARACTERISTICS

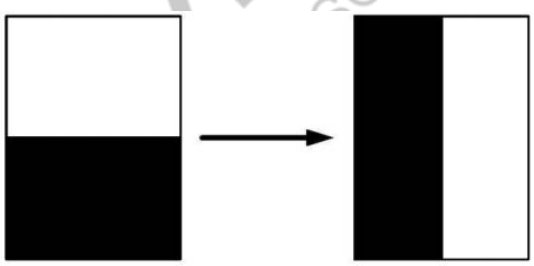
The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, T_{OPR} =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-	-	-	0	-	V
Logic supply voltage	V_{CI}	-	V_{CI}	2.2	3.0	3.7	V
Core logic voltage	V_{DD}	-	V_{DD}	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2V_{CI}	V
High level output voltage	V_{OH}	I_{OH} = -100uA	-	0.9V_{CI}	-	-	V
Low level output voltage	V_{OL}	I_{OL} = 100uA	-	-	-	0.1V_{CI}	V
Typical power	P_{TYP}	V_{CI}=3.0V	-	-	27.0	-	mW
Deep sleep mode	P_{STPY}	V_{CI}=3.0V	-	-	TBD	-	mW
Typical operating current	I_{opr}_V_{CI}	V_{CI}=3.0V	-	-	9.0	-	mA

Image update time	-	25℃	-	-	14	-	sec
Sleep mode current	$I_{slp}\_V_{CI}$	DC/DC OFF No clock No input load Ram data not retain	-	-	TBD	1	uA
Deep sleep mode current	$I_{dslp}\_V_{CI}$	DC/DC OFF No clock No input load Ram data not retain	-	-	TBD	1	uA

Notes:

(1). The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



(2). The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

(3). The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.

6.3 PANEL AC CHARACTERISTICS

6.3.1 MCU Interface Selection

The IC can support 3-wire/4-wire serial peripheral. MCU interface is pin selectable by BS1 shown in Table 6-3-1.

	Pin Name					
MCU interface	**BS1**	**RES#**	**CS#**	**D/C#**	**SCL**	**SDA**
4-wire serial peripheral interface (SPI)	L	RES#	CS#	D/C#	SCL	SDA
3-wire serial peripheral interface (SPI) - 9 bits SPI	H	RES#	CS#	L	SCL	SDA

Table 6-3-1: Interface pins assignment under different MCU interfaces

Note: L is connected to VSS and H is connected to VDDIO.

6.3.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C#, CS#. This control pins status in 4-wire SPI in writing command/data is shown in Table 6-3-2 and the write procedure 4-wire SPI is shown in Figure 6-3-1.

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Table 6-3-2: Control pins status of 4-wire SPI

Notes:
(1). L is connected to VSS and H is connected to VDDIO.
(2). ↑ stands for rising edge of signal.
(3). SDA (Write mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or Command Byte register according to D/C# pin.

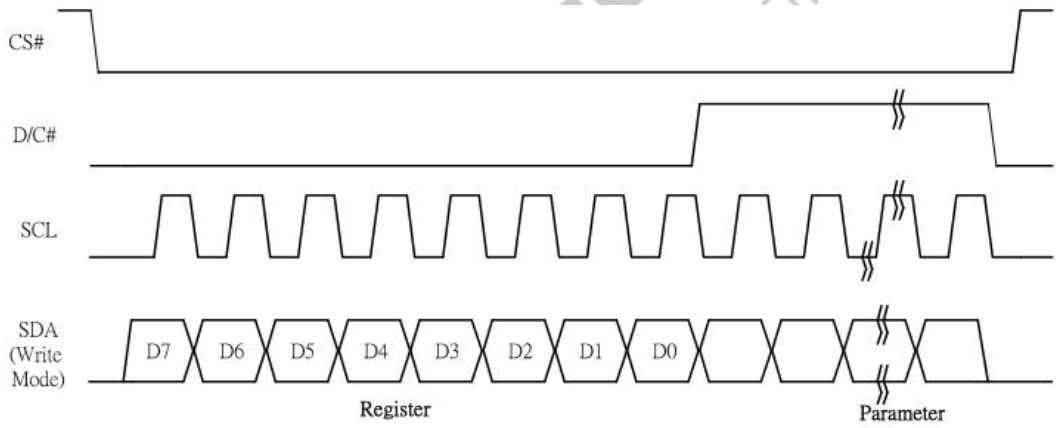


Figure 6-3-1: Write procedure in 4-wire SPI mode

6.3.3 MCU Serial Peripheral Interface (3-wire SPI)

MCU Serial Peripheral Interface (3-wire SPI). The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to DO bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Figure 6-3-2 shows the write procedure in 3-wire SPI.

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Table 6-3-3: Control pins status of 3-wire SPI

Notes:

(1). L is connected to VSS and H is connected to VDDIO.

(2). ↑ stands for rising edge of signal

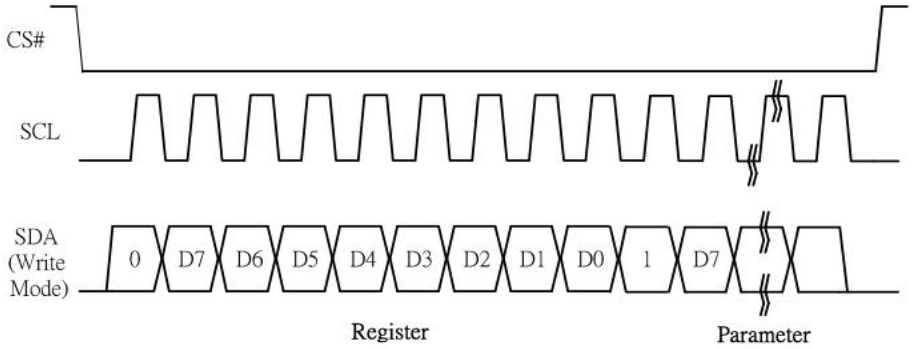
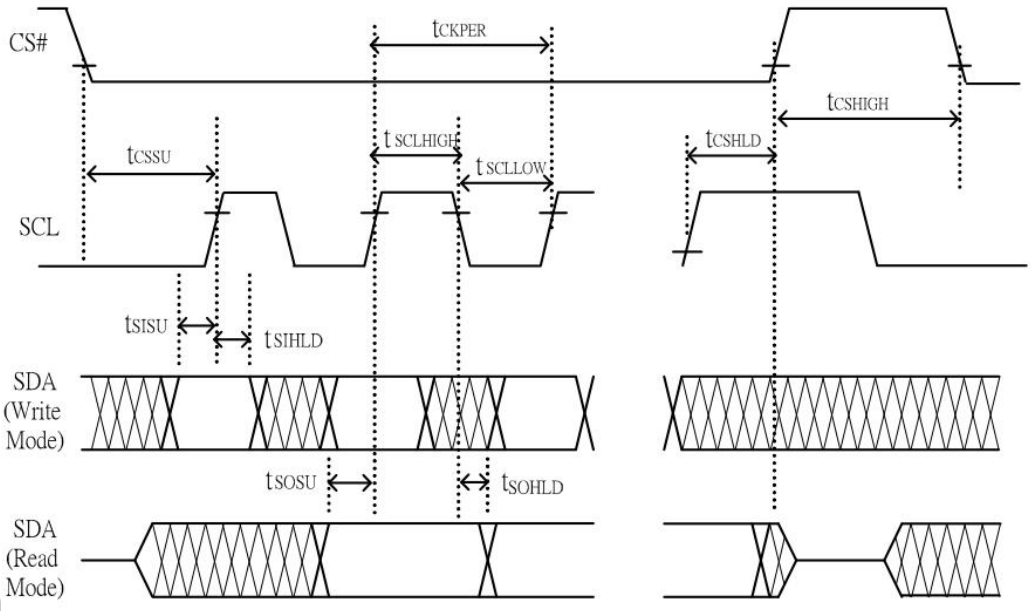


Figure 6-3-2: Write procedure in 3-wire SPI mode

6.3.4 Interface Timing

The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, T_{OPR}=25℃



Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Write Mode)	-	-	20	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	TBD	-	-	ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	TBD	-	-	ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	TBD	-	-	ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	TBD	-	-	ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	TBD	-	-	ns
t_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	TBD	-	-	ns
t_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	TBD	-	-	ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Read Mode)	-	-	2.5	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	TBD	-	-	ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	TBD	-	-	ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	TBD	-	-	ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	TBD	-	-	ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	TBD	-	-	ns
t_{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL	TBD	TBD	-	ns
t_{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL	TBD	TBD	-	ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

7. COMMAND TABLE

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 12Bh [POR], 300 MUX MUX Gate lines setting as (A[8:0] + 1). B [2:0] = 000 [POR]. Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ... B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...299 (left and right gate interlaced) SM=1, G0, G2, G4 ...G294, G1, G3, ...G299 B[0]: TB TB = 0 [POR], scan from G0 to G299 TB = 1, scan from G299 to G0.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 10V to 20V
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		

A[4:0]	VGH	A[4:0]	VGH
00h	20	0Dh	15
03h	10	0Eh	15.5
04h	10.5	0Fh	16
05h	11	10h	16.5
06h	11.5	11h	17
07h	12	12h	17.5
08h	12.5	13h	18
07h	12	14h	18.5
08h	12.5	15h	19
09h	13	16h	19.5
0Ah	13.5	17h	20
0Bh	14	Other	NA
0Ch	14.5		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B [7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

B[7] = 1,
VSH2 voltage setting from 2.4V to 8.6V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AEh	5.6
8Fh	2.5	AFh	5.7
90h	2.6	B0h	5.8
91h	2.7	B1h	5.9
92h	2.8	B2h	6
93h	2.9	B3h	6.1
94h	3	B4h	6.2
95h	3.1	B5h	6.3
96h	3.2	B6h	6.4
97h	3.3	B7h	6.5
98h	3.4	B8h	6.6
99h	3.5	B9h	6.7
9Ah	3.6	BAh	6.8
9Bh	3.7	BBh	6.9
9Ch	3.8	BCh	7
9Dh	3.9	BDh	7.1
9Eh	4	BEh	7.2
9Fh	4.1	BFh	7.3
A0h	4.2	C0h	7.4
A1h	4.3	C1h	7.5
A2h	4.4	C2h	7.6
A3h	4.5	C3h	7.7
A4h	4.6	C4h	7.8
A5h	4.7	C5h	7.9
A6h	4.8	C6h	8
A7h	4.9	C7h	8.1
A8h	5	C8h	8.2
A9h	5.1	C9h	8.3
AAh	5.2	CAh	8.4
ABh	5.3	CBh	8.5
ACh	5.4	CCh	8.6
ADh	5.5	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 8.6V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
21h	8.6	37h	13
22h	8.8	38h	13.2
23h	9	39h	13.4
24h	9.2	3Ah	13.6
25h	9.4	3Bh	13.8
26h	9.6	3Ch	14
27h	9.8	3Dh	14.2
28h	10	3Eh	14.4
29h	10.2	3Fh	14.6
2Ah	10.4	40h	14.8
2Bh	10.6	41h	15
2Ch	10.8	42h	15.2
2Dh	11	43h	15.4
2Eh	11.2	44h	15.6
2Fh	11.4	45h	15.8
30h	11.6	46h	16
31h	11.8	47h	16.2
32h	12	48h	16.4
33h	12.2	49h	16.6
34h	12.4	4Ah	16.8
35h	12.6	4Bh	17
36h	12.8	Other	NA

C[7] = 0,
VSL setting from -5V to -17V

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start	Booster Enable with Phase 1, Phase 2 and Phase 3

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Control	for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR]
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	0	D_5	D_4	D_3	D_2	D_1	D_0		

Bit Description of each byte:
A[6:0] / B[6:0] / C[6:0]:

Bit[6:4]	Driving Strength Selection
000	1(Weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(Strongest)

Bit[3:0]	Min Off Time Setting of GDR [Time unit]
0000 ~ 0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting of phase
D[5:4]: duration setting of phase 3
D[3:2]: duration setting of phase 2
D[1:0]: duration setting of phase 1

Bit[1:0]	Duration of Phase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: *To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	A_1	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	A_6	A_5	A_4	0	A_2	A_1	A_0		A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect A[2:0] / VCI level 100 / 2.3V 101 / 2.4V 110 / 2.5V 111 / 2.6V Other / NA The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperatrure sensor A[7:0] = 80h Internal temperature sensor
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] = 7Fh [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content A[3:0] BW RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	0	0	0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Operating sequence	Parameter (in Hex)
Enable clock signal	80
Disable clock signal	01
Enable clock signal → Enable Analog	C0
Disable Analog → Disable clock signal	03
Enable clock signal → Load LUT (3-color mode) → Disable clock signal	91
Enable clock signal → Load LUT (black/white mode) → Disable clock signal	99
Enable clock signal → Load temperature value → Load LUT (3-color mode) → Disable clock signal	B1
Enable clock signal → Load temperature value → Load LUT (black/white mode) → Disable clock signal	B9
Enable clock signal → Enable Analog → Display (3-color mode) → Disable Analog → Disable OSC	C7
Enable clock signal → Enable Analog → Display (black/white mode) → Disable Analog →Disable OSC	CF
Enable clock signal →Enable Analog → Load temperature value → Load LUT (3-color mode) → DISPLAY (3-color mode) → Disable Analog → Disable OSC	F7
Enable clock signal →Enable Analog → Load temperature value → Load LUT (black/white mode) → DISPLAY (black/white mode) → Disable Analog → Disable OSC	FF

0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required ENABLE CLOCK SIGNAL and ENABLE ANALOG. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	1		0	1	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required ENABLE CLOCK. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	44h	-1.7
0Ch	-0.3	48h	-1.8
10h	-0.4	4Ch	-1.9
14h	-0.5	50h	-2
18h	-0.6	54h	-2.1
1Ch	-0.7	58h	-2.2
20h	-0.8	5Ch	-2.3
24h	-0.9	60h	-2.4
28h	-1	64h	-2.5
2Ch	-1.1	68h	-2.6
30h	-1.2	6Ch	-2.7
34h	-1.3	70h	-2.8
38h	-1.4	74h	-2.9
3Ch	-1.5	78h	-3
40h	-1.6	Other	NA

0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0] ~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0] ~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
1	1		K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0		

0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]] ~J[7:0]: User ID (R38, Byte A and Byte J) [10 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A_5	A_4	0	0	A_1	A_0		
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [227 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1683 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8		
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required ENABLE CLOCK. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] 0: Display Mode 1(3-color mode) 1: Display Mode 2(black/white mode) F[6]: Ping-Pong for black/white mode 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP by command 0x36 2) RAM Ping-Pong function is not support for 3-color mode
0	1		A_7	0	0	0	0	0	0	0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		0	F_6	0	0	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences
0	1		0	0	0	0	0	0	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		

A[7:6]	Select VBD as
00	GS Transition, Defined in A[2] and A[1:0]
01	Fix Level, Defined in A[5:4]
10	VCOM
11[POR]	HiZ

A [5:4] Fix Level Setting for VBD

A[5:4]	VBD level
00	VSS
01	VSH1
10	VSL
11	VSH2

A [1:0] GS Transition setting for VBD
VBD Level Selection:
00b: VCOM ; 01b: VSH1;
10b: VSL; 11b: VSH2

A[1:0]	VBD Transition
00	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	Option for LUT end Set this byte to 22h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26 A[4] =0: select CRC check mode to window mode by C44/C45 window set. A[4] =1: select CRC check mode to Counter mode follow {C[7:0], B[7:0]} set values . {C[7:0], B[7:0]} : default is 0x1608, as the LUT bytes is 5640 bytes.
0	1		0	0	0	A_4	0	0	0	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 31h
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 12Bh
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate A[6:4] / Height / A[6:4] / Height 000 / 8 / 100 / 128 001 / 16 / 101 / 256 010 / 32 / 110 / 300 011 / 64 / 111 / NA A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source A[2:0] / Width / A[2:0] / Width 000 / 8 / 100 / 128 001 / 16 / 101 / 256 010 / 32 / 110 / 400 011 / 64 / 111 / NA BUSY pad will output high during operation.
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate A[6:4] / Height / A[6:4] / Height 000 / 8 / 100 / 128 001 / 16 / 101 / 256 010 / 32 / 110 / 300 011 / 64 / 111 / NA A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source A[2:0] / Width / A[2:0] / Width 000 / 8 / 100 / 128 001 / 16 / 101 / 256 010 / 32 / 110 / 400 011 / 64 / 111 / NA During operation, BUSY pad will output high.
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

8. OPTICAL SPECIFICATIONS

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Parameter	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 °C		14	-	sec	
Life	-	Topr		1000000times or 5years			

Notes:

8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3. WS: White state, DS: Dark state

9. HANDLING, SAFETY, AND ENVIRONMENT REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

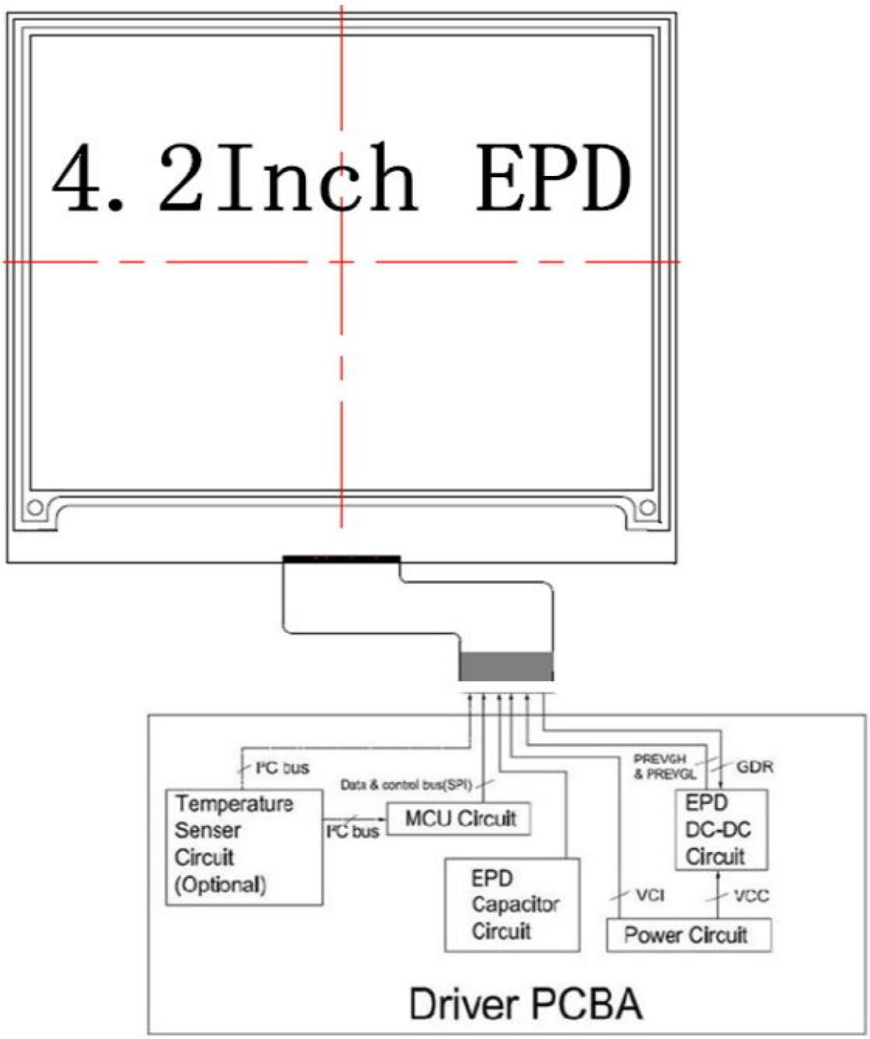
Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

10. RELIABILITY TEST

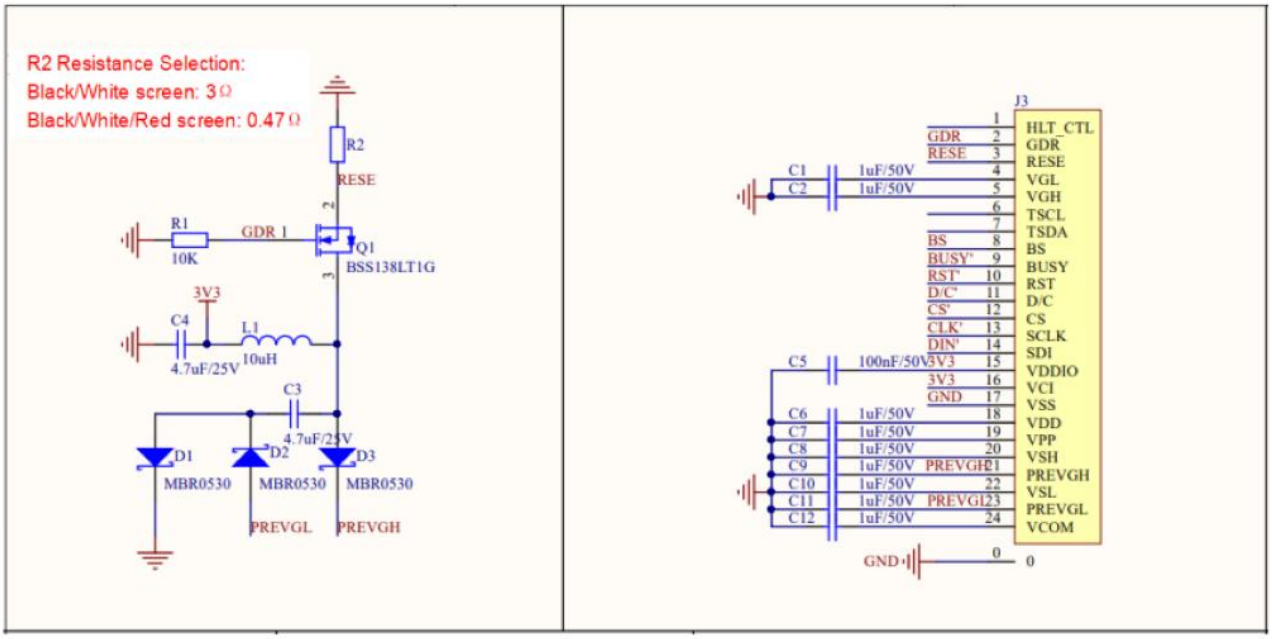
No.	Test Items	Test Conditions
1	Low-Temperature Storage	T= -25°C, 240h Test in white pattern
2	High-Temperature Storage	T= 60°C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T= 40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T= 40°C, RH=80%, 240h
6	High Temperature, High-Humidity Storage	T= 50°C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min] → [+60°C 30min]: 50 cycles Test in white pattern
8	UV Exposure Resistance	765W/m2 for 168hrs,40 C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV: Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1 hour after test finished, the display performance is OK.

11. BLOCK DIAGRAM

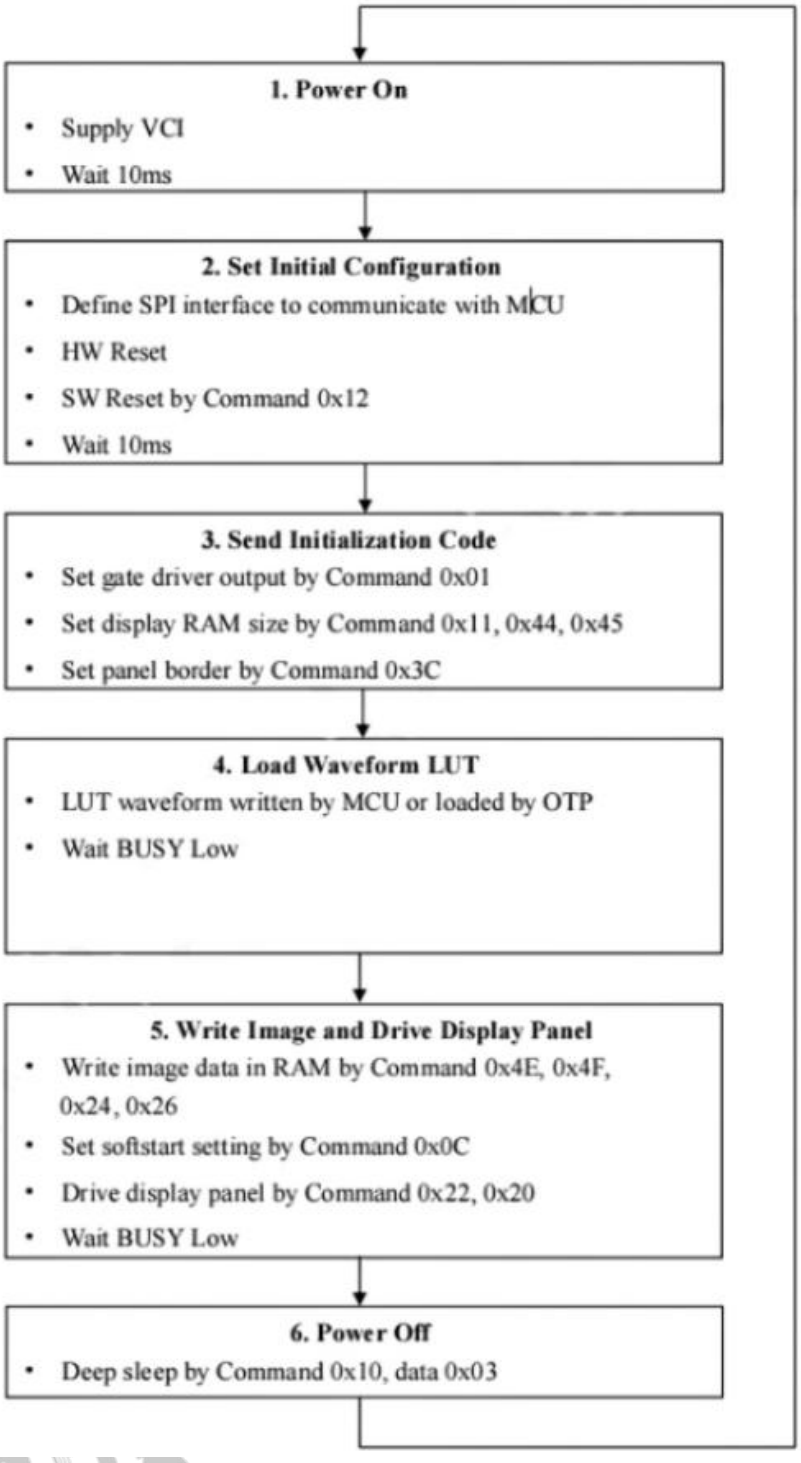


12. REFERENCE CIRCUIT



13. TYPICAL OPERATING SEQUENCE

13.1 NORMAL OPERATION FLOW



13.2 NORMAL OPERATION REFERENCE PROGRAM CODE

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	low	Hardware reset
delay	200us	
RESE#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
Command 0x01	Data0x2b 0x01 0x00	Set display size and driver output control
Command 0x11	Data 0x01	Ram data entry mode
Command 0x44	Data 0x00 0x31	Set Ram X address
Command 0x45	Data 0x2b 0x01 0x00 0x00	Set Ram Y address
Command 0x3C	Data 0x01	Set border
LOAD IMAGE AND UPDATE		
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x2b 0x00	Set Ram Y address counter
Command 0x24	Data 0xXX... , 0xXX	Write B/W image data into to Register 0x24 RAM
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x2b 0x00	Set Ram Y address counter
Command 0x26	Data 0xXX... , 0xXX	Write Red image data into Register 0x26 RAM
Command 0x20		
Read busy pin		
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

14. INSPECTION CONDITIONS

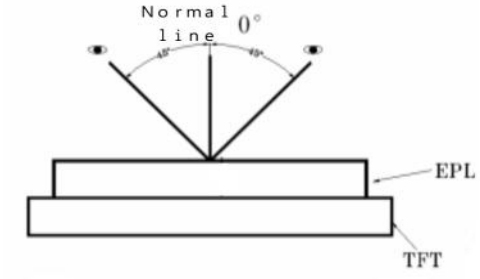
14.1 ENVIRONMENT

Temperature: 25±3℃
Humidity: 55±10%RH

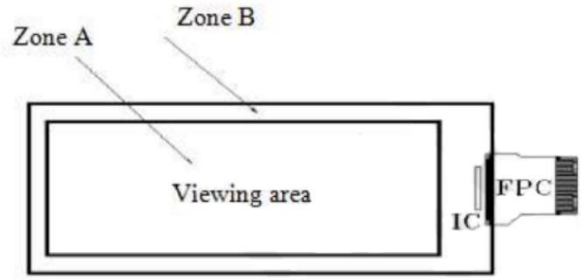
14.2 ILLUMINANCE

Brightness: 1200~1500LUX
Distance: 20-30CM
Angle: Relate 45° surround

14.3 INSPECTION METHOD

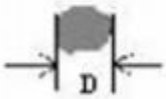
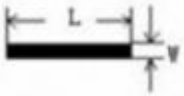


14.4 DISPLAY AREA

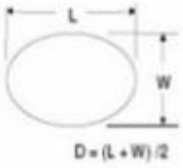


14.5 INSPECTION STANDARD

14.5.1 Electric Inspection Standards

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm。N≤3，and Distance≥5mm 0.4mm＜D Not Allow	MI		
3	Black/White spots (No switch)	 L≤0.6mm，W≤0.2mm，N≤1 L≤2.0mm,W＞0.2mm，Not Allow L＞0.6mm，Not Allow		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash spots/ Larger FPL size	Flash spots in switching, Allowed FPL size larger than viewing area, Allowed	MI	Visual/ Inspection card	Zone A Zone B
6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Display abnormal	Not Allow			

14.5.2 Appearance Inspection Standards

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm，N≤3 D＞0.4mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm  2mm≤X or 2mm≤Y Allow  W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B
5	Substrate color difference	Allowed			
6	FPC broken/ Goldfingers oxidation/ scratch	  Not Allow	MA	Visual / Microscope	Zone B

7	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
8	Edge Adhesives height/FPL/ Edge adhesives bubble	Edge Adhesives height≤ Display surface Edge adhesives seep in≤1/2 Margin width FPL tolerance ±0.3mm Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤3			
9	Protect film	Surface scratch but not effect protect function, Allow		Visual Inspection	

15. PRECAUTIONS

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.
(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue.
(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.