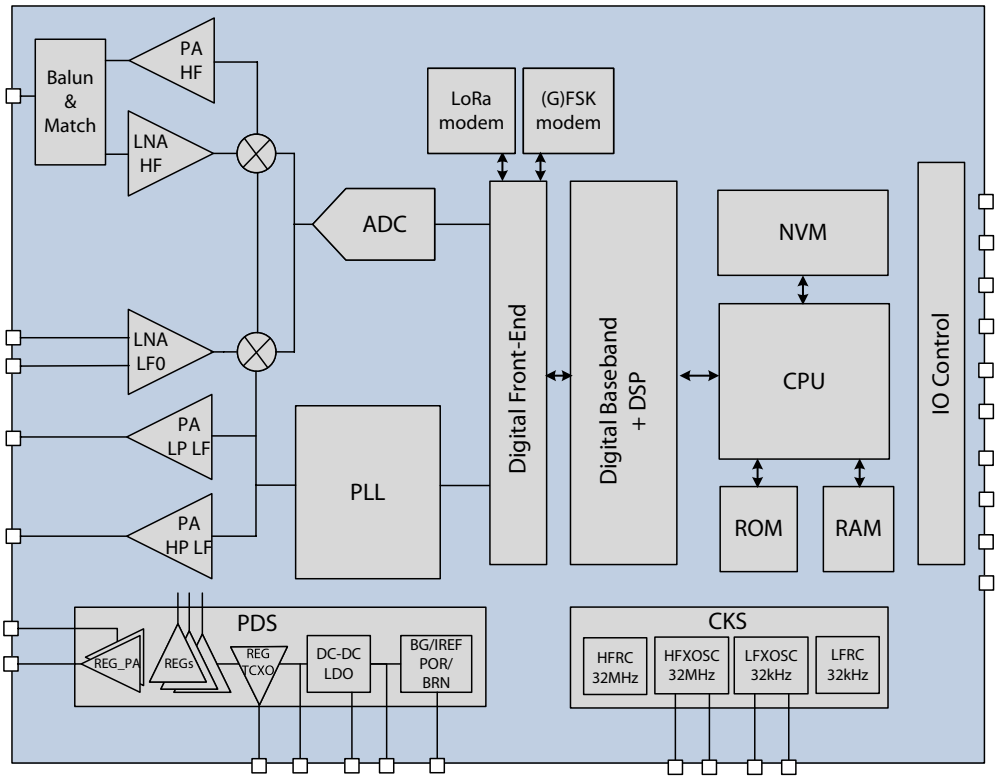
LR1121 Datasheet

Long Range, Low Power, Multi-band LoRa® Transceiver



The LR1121 is an ultra-low power, long range LoRa® transceiver that provides support for terrestrial ISM band communications in the sub-GHz and global 2.4GHz spectrum, as well as S-Band support for satellite connectivity.

For LPWAN use cases, the LR1121 supports LoRa and (G)FSK modulation on both sub-GHz and 2.4GHz bands, as well as Sigfox® modulation on sub-GHz bands, and Long Range Frequency Hopping Spread Spectrum (LR-FHSS) on sub-GHz, 1.9-2.1GHz Satellite, and 2.4GHz ISM bands.

The LR1121 complies with the physical layer requirements of the LoRaWAN® specification released by LoRa Alliance®, while remaining highly configurable to meet different application requirements and proprietary protocols.

The transceiver is suitable for systems targeting compliance with radio standards including but not limited to ETSI EN 300 220, FCC CFR 47 Part 15, ARIB, and Chinese regulatory requirements.

Disclaimer

Long Range-Frequency Hopping Spread Spectrum (LR-FHSS) is a high link-budget, high-performance technology combining the benefits of a modulation employing low energy per bit and advanced frequency hopping schemes to achieve improved coexistence, spectral efficiency and sensitivity. Semtech Corp. holds patents directed to aspects of the LR-FHSS technology.

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Ordering Information

Part Number	Delivery	Minimum Order Quantity
LR1121IMLTRT	Tape & Reel	3000 pieces

QFN32 Package, Pb-free, Halogen free, RoHS/WEEE compliant product.

Revision History

Version	ECO	Date	Applicable to[1]	Changes
1.0	062817	Jul 2022	Use Case: 03 FW version: 01.00 or later	First Release
1.1	065940	Mar 2023	Use Case: 03 FW version: 01.00 or later	Include S-Band information Modified BRLORA RFIO_HF 2.4GHz typical value Section 1.2.4 rewritten Add reference to AN1200.74 in section 4.5 Modified section 1.2.1: air interface Modified Pinout pin 26 description Modified first 3 bullets of section 3.4 Added IDDTXHF3 & IDDTXHF4, & RXSLHF7 & RXSLHF10 parameters Modified section 4.1 Added section 5.6 Tape and Reel Information
1.2	067385	June 2023	Use Case: 03 FW version: 01.02 or later	Added support of Sigfox modulation Table 3-7 Removed FDAFSK condition
2.0	069610	Dec 2023	Use Case: 03 FW version: 01.03 or later	Added 4.3 Chip Wakeup Sequence Modified Figure 4-1 pins 7,8,10,11 Added RxBoosted = 1 to RXSLHF1-6 in Table 3-9

1. Use Case and Version concepts are defined in the LR1121 User Manual, see the `GetVersion` command.

Table of Contents

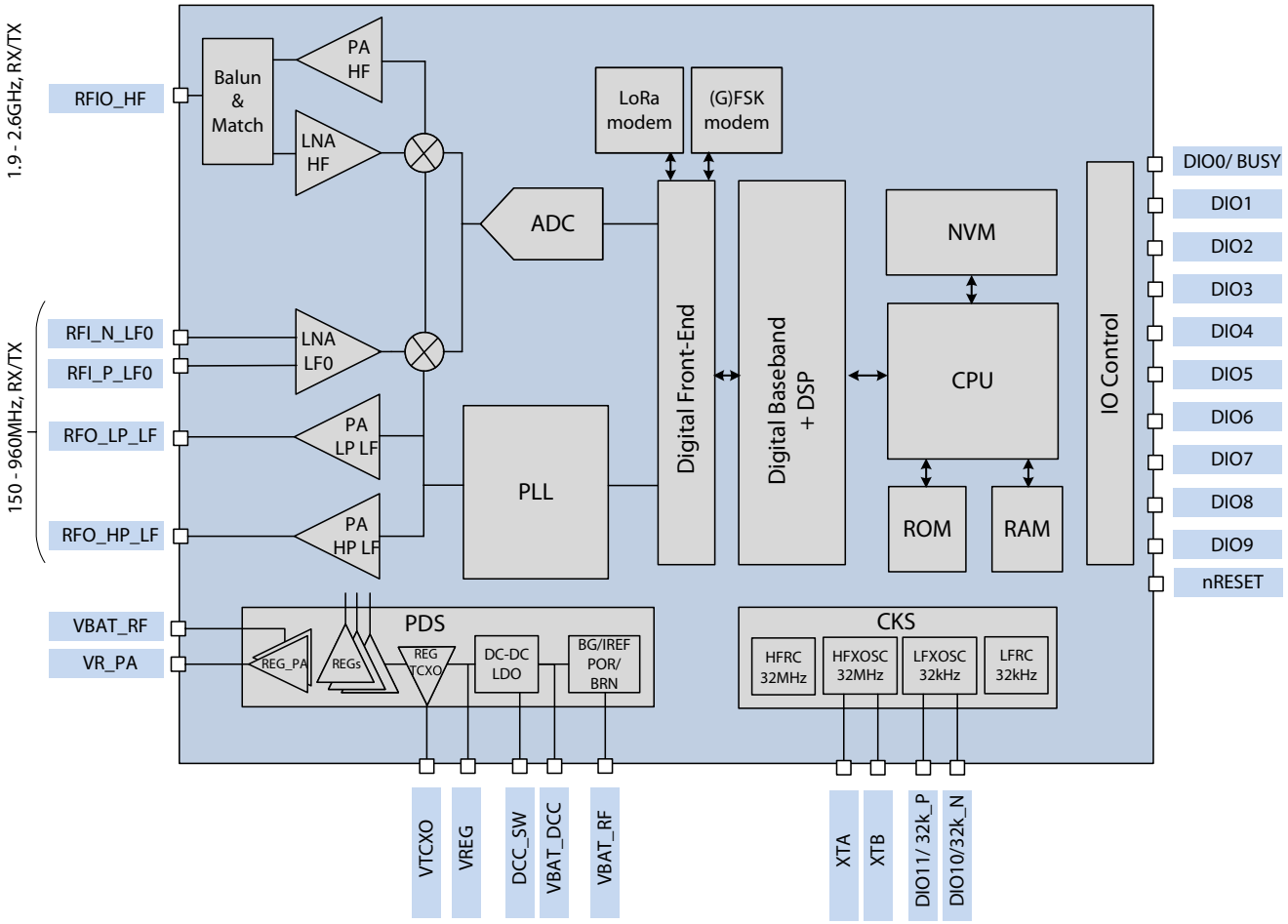
List of Figures

List of Tables

1. System Description

1.1 Simplified Block Diagram

Figure 1-1: LR1121 Simplified Block Diagram



1.2 Overview

1.2.1 Low-Power High-Sensitivity LoRa®/(G)FSK Half-Duplex RF Transceiver

- Worldwide frequency bands support in the range 150 - 960MHz (sub-GHz),1.9-2.1GHz S-band and 2.4GHz ISM band.
- Low Noise Figure modes for enhanced LoRa/ (G) FSK sensitivity (differential input pins RFI_P/N_LF0)
- High power PA path +22dBm (pin RFO_HP_LF) and High efficiency PA path +15dBm (pin RFO_LP_LF) for sub-GHz
- High frequency PA path +13dBm (pin RFIO_HF) for 2.4GHz ISM band and S-band, matched to 50Ohm impedance, reducing the overall Bill Of Materials cost
- Integrated PA regulator supply selector to simplify dual power +15/+22dBm with a single board implementation
- Able to support world-wide multi-region BOM, the circuit adapts to satisfy regulatory limits
- Air interface fully compatible with the SX1261/2/8 family and the LoRaWAN standard, defined by the LoRa Alliance
- LR-FHSS transmitter, with intra-packet hopping capability
- Sigfox transceiver, all Sigfox Radio Configurations (RC1 to RC7) supported. Downlink capability

1.2.2 Multi-Purpose Radio Front-End

- Continuous frequency synthesizer range from 150MHz - 2.5GHz
  - 1.9 to 2.5GHz handled by the RFIO_HF RF port, already matched to 50 Ohms
  - All sub-GHz support handled by the other RF ports
- Digital baseband

1.2.3 Power Management

- Two forms of voltage regulation (DC-DC or linear regulator, LDO) are available depending upon the design priorities of the application. DC-DC usage is recommended for power efficient operation at the cost of an extra inductor.
- Power On Reset (POR), Brown-out detection and Low Battery indication are supported
- Battery voltage measurement

1.2.4 Clock Sources

- 32.768kHz Low Frequency (LF) internal RC oscillator, optionally used by the circuit Real Time Clock (RTC)
- 32.768kHz LF crystal oscillator (XOSC), used for the RTC. An external 32.768kHz reference from a host, applied to pin DIO11, is also possible.
- 32MHz HF RC (HFRC) oscillator allows configuration of the device without the need to start the main crystal oscillator
- 32MHz HF crystal oscillator (HFXOSC) for radio operations and to calibrate frequency error of internal RC oscillators
- 32MHz TCXO can be used to supply the main clock to the circuit, its power supply being integrated on-chip by REG_TCXO, on pin VTCXO. The circuit is able to boot when a TCXO is connected instead of a 32MHz crystal, however all start-up (POR) calibrations are skipped. The host processor should program the TCXO configuration and re-launch the calibrations before further usage of the chip.
- For additional guidance on external clock sources (crystal and TCXO), refer to Section 4.7.

1.2.5 Digital Subsystem

The circuit on-boards power-efficient functionalities, with sufficient hardware resources to implement a wide range of applications:

- Logic to control chip modes, radio front-end, power management and digital interfaces
- RAM partially retained during sleep mode
- Non-volatile memory (NVM)
- Slave serial peripheral interface (SPI)
- DIO0 used as “BUSY” indicator, indicating that the internal MCU cannot receive any commands from the host controller
- Hardware de-bounce and event detection (IOCD)
- Low-power real-time counter (RTC) and watch-dog timer (WDG)
- LoRa, (G)FSK, modems compatible with the SX126x and SX127x product families in sub-GHz bands
- LoRa, (G)FSK, modems compatible with the SX128x product families in the 2.4GHz ISM band
- Long Range FHSS in transmit mode, with intra-packet hopping capability

1.2.6 Cryptographic Engine

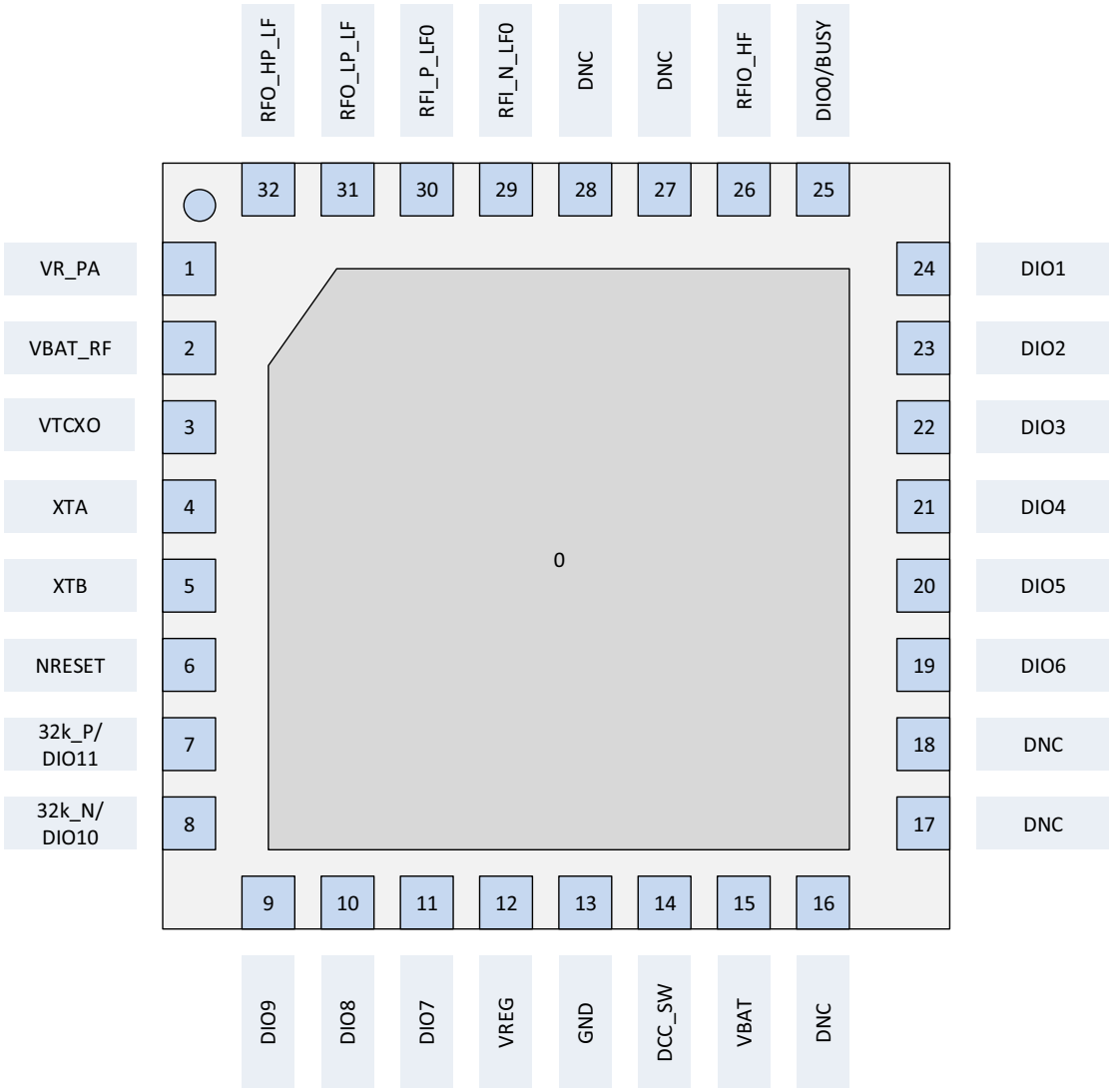
- Hardware support for AES-128 encryption/decryption based algorithms
- Handling device parameters such as DevEUI and JoinEUI, as defined by the LoRa Alliance
- Protects confidential information such as encryption keys against unauthorized access
- Stores NwkKey, AppKey, as defined in the LoRaWAN standard

2. Pin Connection

Table 2-1: LR1121 Pinout

Pin	Name	Type	Description
0	GND	-	Exposed Ground pad
1	VR_PA	O	Regulated power amplifier supply, for all power amplifiers
2	VBAT_RF	I	Battery supply
3	VTCXO	O	Internally generated supply for external TCXO frequency reference
4	XTA	-	32MHz crystal connection, or external TCXO frequency reference input
5	XTB	-	32MHz crystal connection, or NC in case of external TCXO usage
6	NRESET	I	Reset signal, active low
7	32k_P/ DIO11	I/O	32.768kHz crystal connection, or input for 32.768kHz reference clock/ Multi-purpose digital I/O
8	32k_N/ DIO10	I/O	32.768kHz crystal oscillator connection/ Multi-purpose digital I/O
9	DIO9	I/O	Multi-purpose digital I/O
10	DIO8	I/O	Multi-purpose digital I/O
11	DIO7	I/O	Multi-purpose digital I/O
12	VREG	O	Regulated output voltage from the internal regulator LDO/ DC-DC
13	GND	-	Ground
14	DCC_SW	-	DC-DC Switcher Output
15	VBAT	I	Battery supply
16	DNC	-	Do not connect
17	DNC	-	Do not connect
18	DNC	-	Do not connect
19	DIO6	I/O	Multi-purpose digital I/O
20	DIO5	I/O	Multi-purpose digital I/O
21	DIO4	I/O	Multi-purpose digital I/O
22	DIO3	I/O	Multi-purpose digital I/O
23	DIO2	I/O	Multi-purpose digital I/O
24	DIO1	I/O	Multi-purpose digital I/O
25	DIO0/BUSY	I/O	Multi-purpose digital I/O
26	RFIO_HF	I/O	RF input/output for any frequency over 1.9GHz
27	DNC	-	Do not connect
28	DNC	-	Do not connect
29	RFI_N_LF0	I	RF LF receiver input, sub-GHz operation
30	RFI_P_LF0	I	RF LF receiver input, sub-GHz operation
31	RFO_LP_LF	O	RF transmitter output for the low power PA, sub-GHz operation
32	RFO_HP_LF	O	RF transmitter output for the high power PA, sub-GHz operation

Figure 2-1: LR1121 Pinout



3. Specifications

3.1 Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability, reducing product life time.

Table 3-1: Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
VDDmr	Supply voltage	-0.5	-	3.9	V
Tmr	Temperature	-55	-	125	°C
Pmr	RF Input level	-	-	10	dBm

3.2 Operating Range

Operating ranges define the limits for functional operation and parametric characteristics of the device as described in this section. Functionality outside these limits is not guaranteed.

Table 3-2: Operating Range

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDDop	Supply voltage		1.8	-	3.7	V
Top	Temperature under bias (ambient)		-40	-	85	°C
Clop	Load capacitance on digital ports		-	-	20	pF
ML	Maximum Input power	Sub-GHz path	-	-	0	dBm
VSWR	Voltage Standing Wave Ratio	Sub-GHz and RFIO_HF path	-	-	10:1	-

3.3 ESD and Latch-up

The LR1121 is a high performance radio frequency device presenting high ESD and latch-up robustness on all pins. The chip should be handled with all the necessary ESD precautions to avoid any permanent damage.

Table 3-3: ESD and Latch-up

Symbol	Description	Min	Typ	Max	Unit
ESD_HBM	Human Body Model, JEDEC standard JESD22-A114, class II	-	-	2.0	kV
ESD_CDM	ESD Charged Device Model, JEDEC standard JESD22-C101, class II	-	-	500	V
LU	Latch-up, JEDEC standard JESD78, class II level A	-	-	100	mA

3.4 Electrical Specifications

The following tables give the electrical specifications of the LR1121 transceiver under the following conditions, unless otherwise specified:

- VBAT_RF = VBAT = 3.3V, Temperature = 25°C, FXOSC = 32MHz, crystal oscillator
- FRF = 915/869MHz on sub-GHz path RFI_N/P_LF0 and RFO_HP/LP_LF for FSK and LoRa
- Satellite band (S-band) in these tables describes specifications between 1.9 and 2.2GHz
- FRF = S-band and 2.45GHz for the RFIO_HF path, same BOM used for all S-band and 2.45GHz specifications
- All RF impedances on the sub-GHz and RFIO_HF path are matched using multi-band reference design, transmit mode output power defined in 50Ω load, RxBoosted = 1 for LoRa and FSK, differential use of the LNAs (receiver gain levels are referenced in the device's User Manual)
- FSK Bit Error Rate (BER) = 0.1%, 2-level FSK modulation without pre-filtering, BR = 4.8kb/s, FDA = 5kHz, BWF = 20kHz
- LoRa Packet Error Rate (PER) = 1%, BWL= 125kHz, packet of 64 bytes, preamble of 8 symbols, error correction code CR=4/5, CRC on payload enabled, explicit header, sub-GHz frequency range
- Blocking Immunity, ACR, and co-channel rejection are given for a single tone interferer and referenced to sensitivity +3dB, blocking tests are performed with unmodulated interferer
- All power consumption numbers are given with XTAL mode used, the consumption of the TCXO has to be added
- All receiver bandwidths (BW) are expressed as **Double SideBand (DSB)** throughout this document

3.4.1 Power Consumption

The tables below give the total consumptions of all blocks in the specified modes of the circuit.

Table 3-4: Basic Modes Power Consumption

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDPDN	Supply current in power down mode		-	0.8	-	µA
IDDSL3	Supply current in SLEEP mode, no RTC	8kB RAM retained	-	1.6	-	µA
IDDSL1	Supply current in SLEEP mode	No RAM retained	-	1.6	-	µA
IDDSL3A	LFRC (32kHz) based RTC	8kB RAM retained	-	1.85	-	µA
IDDSL2	Supply current in SLEEP mode	No RAM retained	-	1.5	-	µA
IDDSL4A	LFXOSC (32kHz) based RTC	8kB RAM retained	-	1.75	-	µA
IDDSBRLD	Supply current in STBY_RC	HFRC (32MHz) ON, LDO, System clock 16MHz	-	1.25	-	mA
IDDSBXLD	Supply current in STBY_XOSC	HFXOSC ON, LDO	-	1.3	-	mA
IDDSBXDC		HFXOSC ON, DC-DC	-	1.1	-	mA
IDDFSDC	Supply current in Synthesizer mode	DC-DC, system clock 32MHz	-	2.85	-	mA

Table 3-5: Receive Mode Power Consumption, DC-DC Mode Used

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDRXF1	Supply current in Receive mode	FSK 4.8kb/s sub-GHz	-	5.4	-	mA
		with RxBoosted = 1	-	7.5	-	mA
IDDRXF2		FSK 4.8kb/s 2.4GHz/S-band	-	5.9	-	mA
		with RxBoosted = 1	-	6.6	-	mA
IDDRXL1		LoRa® SF12 125kHz sub-GHz	-	5.7	-	mA
		with RxBoosted = 1	-	7.8	-	mA
IDDRXL2		LoRa® SF12 125kHz 2.4GHz/S-band	-	6	-	mA
		with RxBoosted = 1	-	6.7	-	mA
		LoRa® SF12 406kHz 2.4GHz/S-band	-	7.6	-	mA
		with RxBoosted = 1	-	8.3	-	mA
		LoRa® SF12 812kHz 2.4GHz/S-band	-	6.8	-	mA
		with RxBoosted = 1	-	7.5	-	mA

Table 3-6: Transmit Mode Power Consumption[1]

Symbol	Frequency Band	PA Match	Output Power	Min	Typ	Max	Unit
IDDTXLP1	868/915MHz	+14dBm, LP PA[2]	+15dBm	-	36	-	mA
IDDTXLP2			+14dBm	-	28	-	mA
IDDTXLP3			+10dBm	-	18.5	-	mA
IDDTXLP4	434/490MHz		+15dBm	-	35	-	mA
IDDTXLP5			+14dBm	-	28	-	mA
IDDTXLP6			+10dBm	-	19	-	mA
IDDTXHP1	868/915MHz	+22dBm, HP PA[3]	+22dBm	-	118	-	mA
IDDTXHP2			+20dBm	-	96	-	mA
IDDTXHP3			+17dBm	-	73	-	mA
IDDTXHP4			+14dBm	-	50	-	mA
IDDTXHP5	434/490MHz		+22dBm	-	100	-	mA
IDDTXHP6			+20dBm	-	86	-	mA
IDDTXHP7			+17dBm	-	70	-	mA
IDDTXHP8			+14dBm	-	45	-	mA
IDDTXHF1	2.4GHz	+13dBm, HF PA	+13dBm	-	26	-	mA
IDDTXHF2			+10dBm	-	23	-	mA
IDDTXHF3	S-band	+13dBm, HF PA	+13dBm	-	28	-	mA
IDDTXHF4			+10dBm	-	24	-	mA

1. Using optimized settings described in the LR1121 User Manual.
2. DC-DC mode of the LDO/DC-DC combo is used to supply the entire circuit.
3. Battery used to supply the PA, and DC-DC used to supply the rest of the circuit.

3.4.2 General Specifications

Table 3-7: General Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FRSYNTH	Synthesizer frequency range		150	-	2500	MHz
FSTEP	Synthesizer frequency step	FXOSC/ 2	-	0.9536	-	Hz
HFOSCCP	32MHz Crystal oscillator supported off-chip capacitance	Single ended on XTA and XTB	0.2	1	3	pF
OSCTRM1	HF Crystal oscillator trimming step		-	1	-	ppm
LFCLKFR	Frequency of external LF clock applied on pin DIO11		-	32.768	-	kHz
LFCLKRF	Rise/fall time for external LF clock applied on pin DIO11		-	-	5	ns
BRFSK	Bit rate, FSK	Programmable, lowest setting	-	0.6	-	kb/s
	Minimum modulation index is 0.5	Programmable, highest setting	-	300[1]	-	kb/s
FDAFSK	Frequency deviation, FSK	Programmable	0.6	-	200	kHz
BRLORA	Raw data rate, LoRa, sub-GHz	SF12, BWL = 62.5kHz, CR = 1/2	-	91	-	b/s
		SF5, BWL = 500kHz, CR = 4/5	-	62.5	-	kb/s
	Raw data rate, LoRa, RFIO_HF S-band	SF12, BWL=125kHz, CR=4/5	-	0.292	-	kb/s
		SF5, BWL=500kHz, CR=4/5	-	87.5	-	kb/s
	Raw data rate, LoRa, RFIO_HF 2.4GHz	SF12, BWL=203kHz, CR=4/5	-	0.476	-	kb/s
		SF5, BWL=812kHz, CR=4/5	-	101.5	-	kb/s
BWL	Signal BW, LoRa	Programmable, lowest setting	-	62.5	-	kHz
		Programmable, highest setting	-	500[2]	-	kHz
	Signal BW, LoRa, RFIO_HF S-band	Programmable, lowest setting	-	125	-	kHz
		Programmable, highest setting	-	500	-	kHz
	Signal BW, LoRa, RFIO_HF 2.4GHz	Programmable, lowest setting	-	203	-	kHz
		Programmable, highest setting	-	812	-	kHz
SF	Spreading factor coefficient, LoRa	Programmable, lowest setting	-	5	-	-
	chips/symbol = 2^SF	Programmable, highest setting	-	12	-	-
BWF	DSB channel filter BW, FSK,	Programmable, lowest setting	-	4.8	-	kHz
	sub-GHz path	Programmable, highest setting	-	467	-	kHz

1. Maximum bit rate is assumed to scale with the RF frequency; example 300kb/s in the 869/915MHz frequency bands and only 50kb/s @150MHz.
2. For RF frequencies below 300MHz, the LoRa signal BW is limited to maximum 250kHz, the data rate being reduced accordingly.

3.4.3 Receiver

Table 3-8: Receiver Specifications, Sub-GHz Bands (Sheet 1 of 2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
FRRXLF	RX input frequency	Sub-GHz frequency range, LoRa and FSK[1]	150	-	960	MHz
ZINRXLF	RX input impedance	Impedance across RFI_N_LF0 / RFI_P_LF0[2]				
		433MHz	-	29 - j289	-	Ohm
		868MHz	-	9.4 - j141	-	Ohm
		920MHz	-	9.5 - j131	-	Ohm
PHNLF1	Synthesizer phase noise[3,4] sub-GHz band	100kHz offset	-	-102	-	dBc/Hz
PHNLF2		1MHz offset	-	-120	-	dBc/Hz
PHNLF3		10MHz offset	-	-129	-	dBc/Hz
RXS2F1	Sensitivity 2-FSK	BRF = 0.6kb/s, FDA = 0.8kHz, BWF = 4kHz	-	-123	-	dBm
RXS2F2		BRF = 1.2kb/s, FDA = 5kHz, BWF = 20kHz	-	-122	-	dBm
RXS2F3		BRF = 4.8kb/s, FDA = 5kHz, BWF = 20kHz	-	-117.5	-	dBm
RXS2F4		BRF = 38.4kb/s, FDA = 40kHz, BWF = 160kHz	-	-109	-	dBm
RXS2F5		BRF = 250kb/s, FDA = 125kHz, BWF = 500kHz	-	-103.5	-	dBm
RXS2F1HP3	Sensitivity 2-FSK, RxBoosted = 1	BRF = 0.6kb/s, FDA = 0.8kHz, BWF = 4kHz	-	-125	-	dBm
RXS2F2HP3		BRF = 1.2kb/s, FDA = 5kHz, BWF = 20kHz	-	-124	-	dBm
RXS2F3HP3		BRF = 4.8kb/s, FDA = 5kHz, BWF = 20kHz	-	-119	-	dBm
RXS2F4HP3		BRF = 38.4kb/s, FDA = 40kHz, BWF = 160kHz	-	-111	-	dBm
RXS2F5HP3		BRF = 250kb/s, FDA = 125kHz, BWF = 500kHz	-	-105	-	dBm
CCRFSK	Co-channel rejection, FSK		-	-8	-	dB
ACRFSK	Adjacent channel rejection, FSK	Offset = +/- 50kHz	-	47	-	dB
BIFSK1	Blocking immunity, FSK	BRF = 4.8 kb/s, FDA = 5kHz, BWF = 20kHz Offset = +/- 1MHz	-	67	-	dB
BIFSK2		Offset = +/- 2MHz	-	70	-	dB
BIFSK3		Offset = +/- 10MHz	-	80	-	dB
IIP3FSK	3rd order input intercept point, FSK	Unwanted tones @1MHz and 1.96MHz	-	-12	-	dBm
IMRFSK	Image attenuation, sub-GHz path	Without IQ calibration	-	40	-	dB
		With IQ calibration	-	50	-	dB
RXSIG	Sigfox receive sensitivity	BRF = 0.6 kb/s, FDA = 0.8 kHz, BWF = 4 kHz	-	-125	-	dBm
RXSL1	Sensitivity LoRa	BWL = 62.5kHz, SF = 7	-	-128	-	dBm
RXSL2		BWL = 62.5kHz, SF = 12	-	-142	-	dBm
RXSL3		BWL = 125kHz, SF = 7	-	-125	-	dBm
RXSL4		BWL = 125kHz, SF = 12	-	-139	-	dBm
RXSL5		BWL = 250kHz, SF = 7	-	-122	-	dBm
RXSL6		BWL = 250kHz, SF = 12	-	-136	-	dBm
RXSL7		BWL = 500kHz, SF = 7	-	-118	-	dBm
RXSL8		BWL = 500kHz, SF = 12	-	-132	-	dBm

Table 3-8: Receiver Specifications, Sub-GHz Bands (Sheet 2 of 2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
RXSL1HP7	Sensitivity LoRa, RxBoosted = 1	BWL = 62.5kHz, SF = 7	-	-130	-	dBm
RXSL2HP7		BWL = 62.5kHz, SF = 12	-	-144	-	dBm
RXSL3HP7		BWL = 125kHz, SF = 7	-	-127	-	dBm
RXSL4HP7		BWL = 125kHz, SF = 12	-	-141	-	dBm
RXSL5HP7		BWL = 250kHz, SF = 7	-	-124	-	dBm
RXSL6HP7		BWL = 250kHz, SF = 12	-	-138	-	dBm
RXSL7HP7		BWL = 500kHz, SF = 7	-	-121	-	dBm
RXSL8HP7		BWL = 500kHz, SF = 12	-	-134	-	dBm
CCRLORA1	Co-channel rejection, LoRa	SF = 7	-	5	-	dB
CCRLORA2		SF = 12	-	19	-	dB
ACRLORA1	Adjacent channel rejection, LoRa	Offset = +/- 1.5 x BW_L BW_L = 125kHz, SF = 7	-	60	-	dB
ACRLORA2		BW_L = 125kHz, SF = 12	-	73	-	dB
BILORA1	Blocking immunity, LoRa, BW_L = 125kHz	SF =12, offset = +/- 1MHz	-	88	-	dB
BILORA2		SF =12, offset = +/- 2MHz	-	91	-	dB
BILORA3		SF =12, offset = +/- 10MHz	-	103	-	dB
BILORA4		SF =7, offset = +/- 1MHz	-	74	-	dB
BILORA5		SF =7, offset = +/- 2MHz	-	77	-	dB
BILORA6		SF =7, offset = +/- 10MHz	-	90	-	dB
FERR	Max. tolerated frequency offset between Tx and Rx	SF5 to SF12 All bandwidths, ±25% of BW. The tighter limit applies (see below)	-	+/- 25%	-	BW_L
	Max. tolerated frequency offset between Tx and Rx	SF12	-50	-	50	ppm
		SF11	-100	-	100	ppm
		SF10	-200	-	200	ppm
FDRIFT	LoRa frequency drift tolerance	For sensitivity degradation below 3dB BW_L=125kHz, SF12, LowDataRateOptimize = 1	-	-	120	Hz/s

1. LoRa operation is on the 150 - 960MHz band.
2. Single ended impedance presented at the package level, without the effect of the PCB.
3. Phase Noise specifications are given for the recommended PLL bandwidth to be used for the specific modulation/ bit rate.
4. Phase Noise is not constant over frequency, the topology of VCO + DIV used, for two frequencies close to each other, the phase noise could change significantly; the specification covers the worse value.

Table 3-9: Receiver Specifications, S-Band and 2.4GHz ISM Band (Sheet 1 of 2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
FRRXHF	RX input frequency	S-Band, LoRa	1900	-	2200	MHz
		2.4GHz frequency range, LoRa and FSK	2400	-	2500	MHz
ZINRXHF	RX input impedance	Impedance across RFIO_HF, 2.4GHz	-	50 + j 0	-	Ohm
RXS2FHF2	Sensitivity 2-FSK	BRF = 1.2kb/s, FDA = 5kHz, BWF = 20kHz	-	-117	-	dBm
RXS2FHF3		BRF = 4.8kb/s, FDA = 5kHz, BWF = 20kHz	-	-112	-	dBm
RXS2FHF4		BRF = 38.4kb/s, FDA = 40kHz, BWF = 160kHz	-	-103	-	dBm
RXS2FHF5		BRF = 250kb/s, FDA = 125kHz, BWF = 500kHz	-	-97.5	-	dBm
CCRFSKHF	Co-channel rejection, FSK		-	-8	-	dB
ACRFSKHF1	Adjacent channel rejection, FSK	Offset= = +/- 50kHz	-	33	-	dB
ACRFSKHF2		Offset= = +/- 1MHz	-	58	-	dB
BIFSKHF1	Blocking Immunity, FSK	Offset= = +/- 2MHz	-	63	-	dB
BIFSKHF2		Offset= = +/- 10MHz	-	77	-	dB
IMRFSKHF	Image attenuation, FSK	Without IQ calibration	-	23	-	dB
RXSLHF1	Sensitivity LoRa Signal S-Band RxBoosted = 1	BWL = 125kHz, SF = 7	-	-118	-	dBm
RXSLHF2		BWL = 125kHz, SF = 12	-	-132.5	-	dBm
RXSLHF3		BWL = 250kHz, SF = 7	-	-116	-	dBm
RXSLHF4		BWL = 250kHz, SF = 12	-	-130	-	dBm
RXSLHF5		BWL = 500kHz, SF = 7	-	-112	-	dBm
RXSLHF6		BWL = 500kHz, SF = 12	-	-124.5	-	dBm
RXSLHF7	Sensitivity LoRa Signal 2.4GHz band RxBoosted = 1	BWL = 406kHz, SF = 5	-	-111	-	dBm
RXSLHF8		BWL = 406kHz, SF = 7	-	-129	-	dBm
RXSLHF10		BWL = 812kHz, SF = 5	-	-108	-	dBm
RXSLHF9		BWL = 812kHz, SF = 7	-	-112	-	dBm
CCRLORAHF1	Co-channel rejection, LoRa	BWL = 406kHz, SF = 7	-	5	-	dB
CCRLORAHF2		BWL = 406kHz, SF = 12	-	19	-	dB
CCRLORAHF3		BWL = 812kHz, SF = 7	-	5	-	dB
CCRLORAHF4		BWL = 812kHz, SF = 12	-	19	-	dB
ACRLORAHF1	Adjacent channel rejection, LoRa	BWL = 406kHz, SF=7, Offset = +1.5 x BW_L	-	53	-	dB
ACRLORAHF2		BWL = 406kHz, SF=7, Offset = -1.5 x BW_L	-	34	-	dB
ACRLORAHF3		BWL = 406kHz, SF=12, Offset = +1.5 x BW_L	-	68	-	dB
ACRLORAHF4		BWL = 406kHz, SF=12, Offset = -1.5 x BW_L	-	49	-	dB
ACRLORAHF5		BWL = 812kHz, SF=7, Offset = +1.5 x BW_L	-	59	-	dB
ACRLORAHF6		BWL = 812kHz, SF=7, Offset = -1.5 x BW_L	-	59	-	dB
ACRLORAHF7		BWL = 812kHz, SF=12, Offset = +1.5 x BW_L	-	72	-	dB
ACRLORAHF8		BWL = 812kHz, SF=12, Offset = -1.5 x BW_L	-	72	-	dB

Table 3-9: Receiver Specifications, S-Band and 2.4GHz ISM Band (Sheet 2 of 2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
BILORAHF1	Blocking Immunity, LoRa	BWL = 406kHz, SF=7, Offset= +/- 1MHz	-	59	-	dB
BILORAHF2		BWL = 406kHz, SF=7, Offset= +/- 2MHz	-	64	-	dB
BILORAHF3		BWL = 406kHz, SF=7, Offset= +/- 10MHz	-	80	-	dB
BILORAHF4		BWL = 406kHz, SF=12, Offset= +/- 1MHz	-	73	-	dB
BILORAHF5		BWL = 406kHz, SF=12, Offset= +/- 2MHz	-	79	-	dB
BILORAHF6		BWL = 406kHz, SF=12 Offset= +/- 10MHz	-	94	-	dB
BILORAHF7		BWL = 812kHz, SF=7, Offset= +/- 1MHz	-	57	-	dB
BILORAHF8		BWL = 812kHz, SF=7, Offset= +/- 2MHz	-	61	-	dB
BILORAHF9		BWL = 812kHz, SF=7, Offset= +/- 10MHz	-	78	-	dB
BILORAHF10		BWL = 812kHz, SF=12, Offset= +/- 1MHz	-	70	-	dB
BILORAHF11		BWL = 812kHz, SF=12, Offset= +/- 2MHz	-	76	-	dB
BILORAHF12		BWL = 812kHz, SF=12 Offset= +/- 10MHz	-	91	-	dB

3.4.4 Transmitter

Table 3-10: Transmitter Specifications, Sub-GHz Path

Symbol	Description	Conditions	Min	Typ	Max	Unit
TXOPLP	Maximum TX power	LP PA	+12	+15	-	dBm
TXOPHP		HP PA	+19	+22	-	dBm
TXDRPLF1	Drop in maximum TX power vs. VDD (1.8 to 3.7V)	LP PA operating under DC-DC or LDO	-	0.5	-	dB
TXDRPLF2		HP PA, operating under battery	-	6	-	dB
TXPRNGLF	TX power range	Programmable in steps of -1dB from maximum TX power	-	31	-	steps
TXACCLF	TX output power step accuracy		-	+/- 2	-	dB
TXRMPLF	Power amplifier ramping time	Programmable, lowest step	-	16	-	µs
		Programmable, highest step	-	304	-	µs
TXEVM	EVM for LR-FHSS	GMSK 488b/s	-	-	-20	dB

Table 3-11: Transmitter Specifications, S-band and 2.4GHz ISM Band

Symbol	Description	Conditions	Min	Typ	Max	Unit
TXOPHF	Maximum TX power	HF PA	9	+11.5	-	dBm
TXDRPHF	Drop in maximum TX power vs. VDD (1.8 to 3.7V)	LP PA operating under DC-DC or LDO	-	0.5	-	dB
TXPRNGHF	TX power range	Programmable in steps of -1dB from maximum TX power	-	31	-	steps
TXACCHF	TX output power step accuracy		-	+/- 2	-	dB
TXRMPHF	Power amplifier ramping time	Programmable, lowest step	-	16	-	µs
		Programmable, highest step	-	304	-	µs
TXEVMHF	EVM for LR-FHSS	GMSK 488b/s	-	-	-20	dB

3.5 Reference Oscillator

Table 3-12: 32MHz Crystal Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FXOSCHF	Crystal oscillator frequency		-	32	-	MHz
CLOADHF	Crystal loading capacitance	Differential	9.5	10	10.5	pF
C0XTALHF	Crystal shunt capacitance		0.3	0.6	2	pF
RSXTALHF	Crystal series resistance		-	30	60	Ω
CMXTALHF	Crystal motional capacitance		1.3	1.89	2.5	fF
DRIVEHF	Drive level		-	-	100	µW
FRTOLHF	Crystal frequency accuracy	Initial	-	-	+/- 10	ppm
		Over temperature (-20 to 70°C)	-	-	+/- 10	ppm
		Aging over 10 years	-	-	+/- 10	ppm

Table 3-13: 32MHz TCXO Regulator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
CVTCXO	External decoupling capacitor for REG_TCXO	X5R type recommended	70	100	130	nF
RVTCXO	Equivalent series resistance for CVTCXO		0.1	-	1	Ohm
VTCXO	Regulated voltage range for TCXO voltage supply, VDDop > VTCXO + 200mV	RegTcxoTune = 000	-	1.6	-	V
		RegTcxoTune = 001	-	1.7	-	V
		RegTcxoTune = 111	-	3.3	-	V
ILTCXO	Load current for TCXO regulator		-	1.5	4	mA
ATCXO	Amplitude voltage for external TCXO applied to XTA pin	AC coupled through 10pF DC-cut series with 220Ohm	0.4	0.6	1.2	Vpk-pk

Table 3-14: 32kHz Crystal Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FXOSCLF	Crystal oscillator frequency		32400	32768	33100	Hz
CLOADLF	Crystal loading capacitance	Differential	-	9.0	-	pF
C0XTALLF	Crystal shunt capacitance		0.7	1.1	2	pF
RSXTALLF	Crystal series resistance		25	45	100	kΩ
CMXTALLF	Crystal motional capacitance		1.5	4.7	8	fF
DRIVELF	Drive level		0.5			µW
FRTOLLF	Crystal frequency accuracy	Initial	-	-	+/-20	ppm
		Over temperature (-20 to 70°C)	-	-	+/-180	ppm
		Aging over 10 years	-	-	+/-3	ppm

3.6 Digital I/O, Flash Memory, & Interface Specifications

3.6.1 Digital I/O Specifications

Table 3-15: Digital I/O and NRESET Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Input High Voltage		0.7*VBAT	-	VBAT+0.3	V
VIL	Input Low Voltage		-0.3		0.3*VBAT	V
VOH	Output High Voltage	I_{max} = 2.5mA	0.9*VBAT		VBAT	V
VOL	Output Low Voltage	I_{max} = -2.5mA	0		0.1*VBAT	V

3.6.2 Flash Memory Specifications

The LR1121 embeds a Flash memory for storing the internal firmware, application configuration data, and security keys.

Table 3-16: Flash Memory Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FEND	Flash Memory Endurance	T_{op}=-40 to 85°C	10.000	-	-	Cycles
FRET	Flash Memory Data Retention	T_{op}=85°C	10	-	-	Years

3.6.3 SPI Interface

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 (clock polarity and phase in Motorola/NXP® Freescale™ nomenclature). Only the slave side is implemented. A transfer is always started by a falling edge of NSS. MISO is high impedance when NSS is high. The SPI runs on the external SCK signal to allow high speed operation up to 16MHz.

All timings in the following table are given for a maximum load capacitance of 10pF.

Table 3-17: SPI Timing Requirements

Symbol	Description	Min.	Typ.	Max.	
t1	NSS falling edge to SCK setup time	31.25	-	-	ns
t2	SCK period	61.5	-	-	ns
t3	SCK high time	31.25	-	-	ns
t4	MOSI to SCK hold time	5	-	-	ns
t5	MOSI to SCK setup time	15	-	-	ns
t6	NSS falling to MISO delay	0	-	15	ns
t7	SCK falling to MISO delay	0	-	15	ns

4. Application Information

4.1 Sigfox Transceiver

The LR1121 supports the transmission of Sigfox packets at both 100 and 600bps, allowing compatibility with Sigfox Radio Configurations RC1 to RC7. The LR1121 can also receive Sigfox downlinks.

No Sigfox protocol stack is embedded inside the LR1121, packet transmission has to be handled directly by the host MCU.

4.2 LR-FHSS Modulation

The LR1121 supports LR-FHSS modulation (compliant with the LoRaWAN specification released by the LoRa Alliance), which modulates the packet content across several pseudo-random frequencies, providing the following benefits:

- In FCC regions, the LR-FHSS can eliminate the dwell-time limitation by intra-packet hopping. It thus allows to use slower data rates, which increases the communication range, and to carry a longer payload.
- In ETSI regions, the LR-FHSS can provide improved capacity and an even longer range than LoRa for lower data rate devices where the spectrum is limited such as Europe or India.
- The LR-FHSS modulation provides even better robustness in the presence of interferences than LoRa.

The LR1121 is able to generate LR-FHSS modulated packets on all sub-GHz, S-band and 2.4GHz ISM bands.

LR-FHSS implementation in the LR1121 is transmit only.

4.3 Chip Wakeup Sequence

The supported wakeup sequence is as follows:

1. Bring NSS low.
2. Wait 100µs.
3. Bring NSS high.
4. Wait until the BUSY signal falls before executing the next command.

4.4 Exiting Sleep Mode

The LR1121 exits the lowest-power Sleep mode with:

- A falling edge on the NSS signal
- An RTC Timeout configured in the *SleepConfig* parameter of the `SetSleep()` command

Implementation options are detailed in the User Manual, and both can be combined.

4.5 Digital Inputs/Outputs

The LR1121 features 12 digital input/output (DIO) pins, dedicated to host or sensors/peripherals communication, interruption handling and external RF switches or LNA control.

4.5.1 DIO Configuration

The LR1121 features a DIO switch matrix (SWM), allowing a reconfiguration of the DIOs depending on the application requirements. For a transceiver use case, the LR1121 is controlled by a host MCU, hence the DIOs are dedicated to host communication. In order to reduce the constraints on the MCU pin count, five DIOs can be used to control external RF switches or LNAs.

Table 4-1: LR1121 DIO Mapping

Pin	I/O Name	Function
6	NRESET	NRESET
7	32k_P/ DIO11	32k_P/ NC
8	32k_N/ DIO10	32k_N/ RFSW4
9	DIO9	IRQ
10	DIO8	RFSW3
11	DIO7	RFSW2
19	DIO6	RFSW1
20	DIO5	RFSW0
21	DIO4	SPI MISO
22	DIO3	SPI MOSI
23	DIO2	SPI SCK
24	DIO1	SPI NSS
25	DIO0/ BUSY	BUSY

4.5.2 RF Switch Control

The LR1121 can control up to 5 external RF switches or LNAs on the RFIO_HF and Sub-GHz RF paths, reducing the number of host controller IOs required for the application. This allows you to select application MCUs with a reduced pin count or a smaller footprint and therefore design highly integrated solutions. The polarity of the RF switch control signals can be set in each radio mode. By default no DIO is used as RF switch control line, all RF switch outputs are kept in High-Z state.

4.5.3 Reset

A complete restart of the LR1121 internal firmware can be issued on request by toggling the NRESET pin. It will be automatically followed by the standard calibration procedure and any previous context will be lost. The pin should be held low for more than 100µs for the reset to occur.

4.5.4 Host Interrupts

The LR1121 offers 24 interrupt sources, allowing the host to react to special events in the LR1121 system without the need to poll registers, in order to design power optimized applications.

Interrupts to the host are signalled through one (or more) IRQ lines configured on the DIOs, and can be masked or cleared using dedicated commands.

The interrupt status can be read by the host through the 32-bit interrupt status register. They can be cleared by writing a 1 to the respective bit.

4.6 Firmware Upgrade/ Update

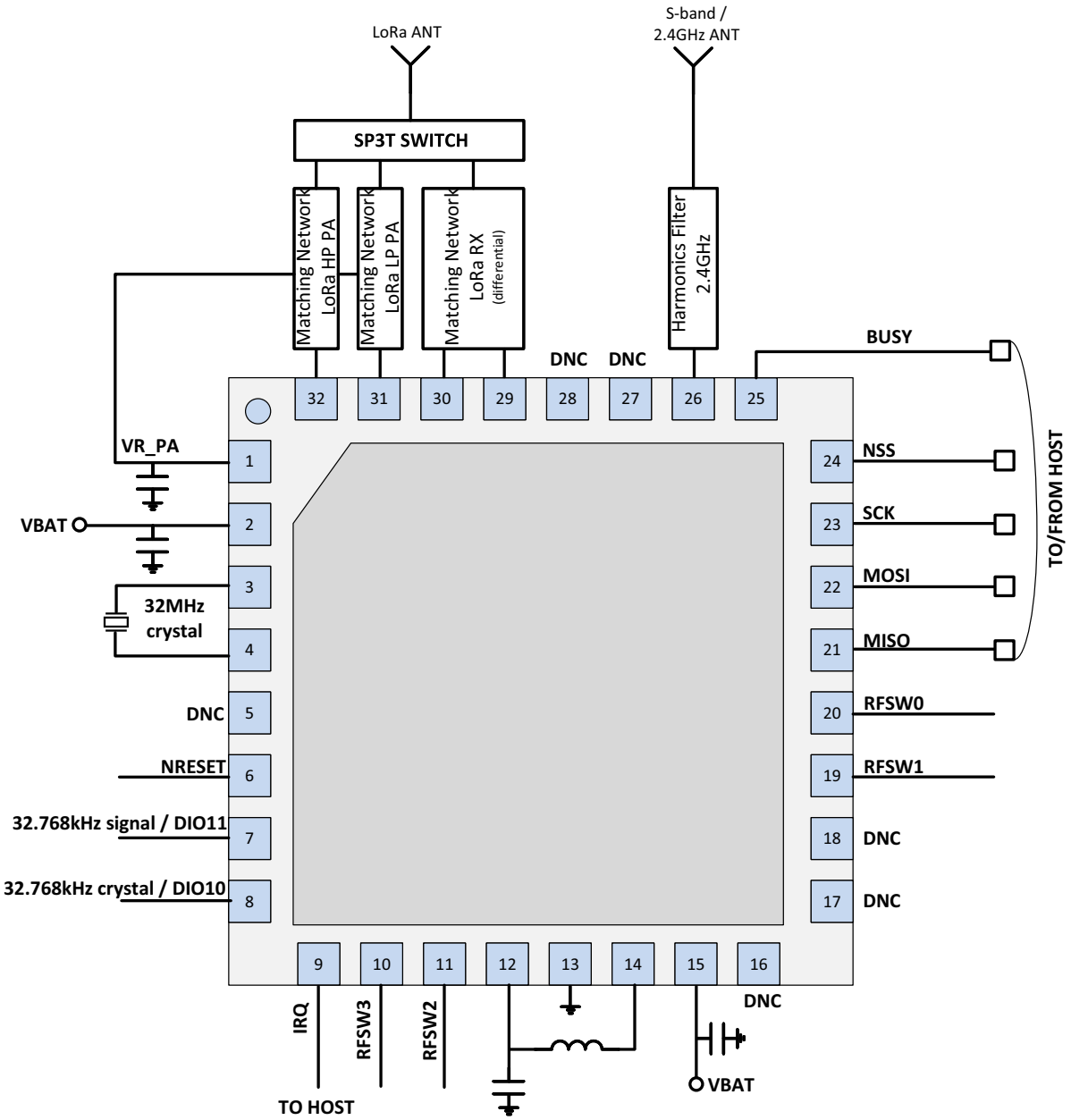
During the manufacturing process, the LR1121 will be provisioned and contain the embedded firmware image.

During the product assembly process, the customer will be able to upgrade the full embedded firmware image running on the LR1121 via the SPI interface. The bootloader of the LR1121 will authenticate the firmware and will allow further execution. Only firmware images provided by Semtech can run on the LR1121. It is advised to flash the device with the latest firmware available.

The LR1121 can also support patch updates, typically for maintenance in the field. Refer to AN1200.57 for additional information.

4.7 Simplified Reference Schematic

Figure 4-1: Multi-band EU/US LoRaWAN Using Sub-GHz PAs

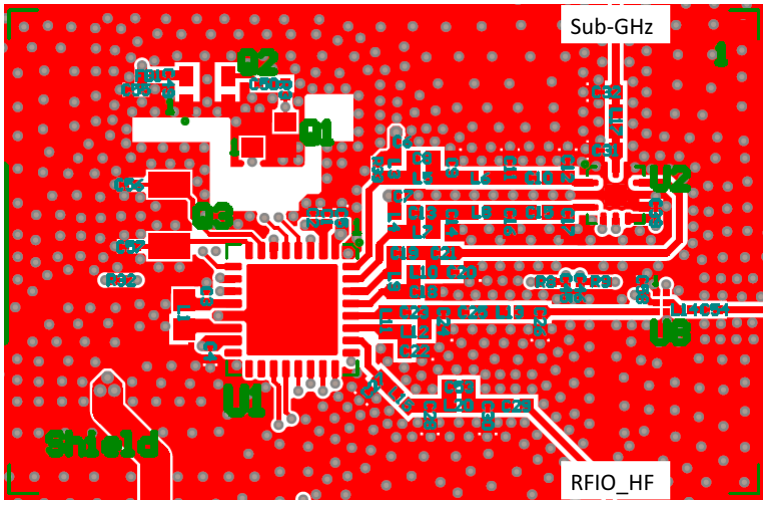


This section provides a reference schematic example using the LR1121.

- For additional guidance about 32MHz and 32kHz clock sources, refer to AN1200.74 LoRa Edge™ Clock Requirements.

4.8 Example Reference Layout

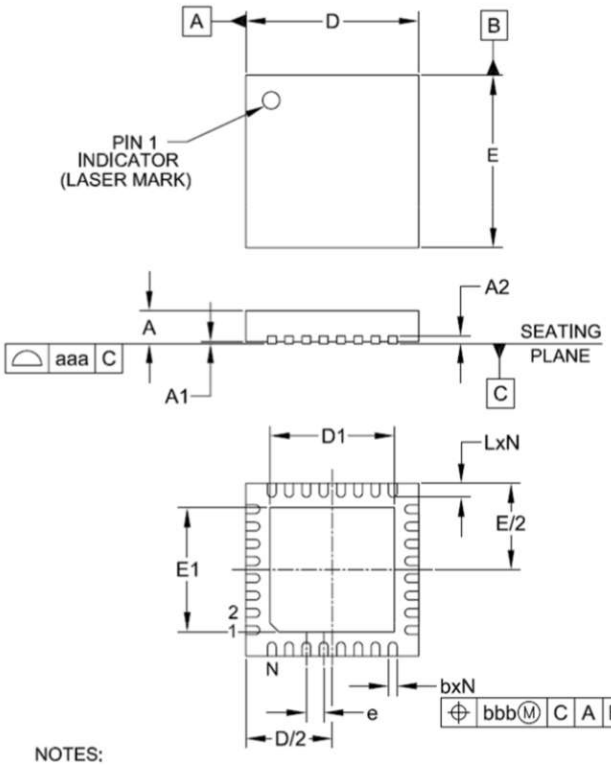
Figure 4-2: Reference Design Layout



5. Package Information

5.1 Package Outline Drawing

Figure 5-1: Package Outline Drawing

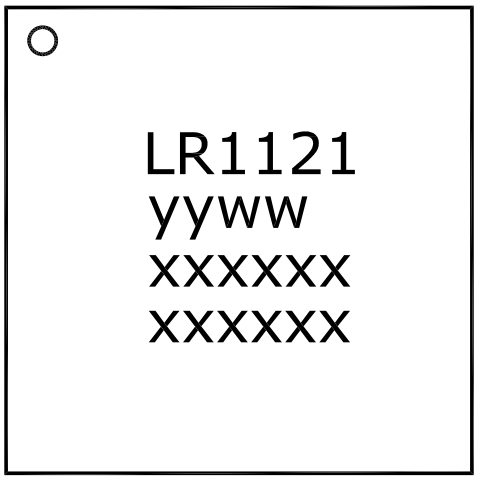


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.140	.146	.150	3.30	3.70	3.80
E	.193	.197	.201	4.90	5.00	5.10
E1	.140	.146	.150	3.30	3.70	3.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

5.2 Package Marking

Figure 5-2: Package Marking



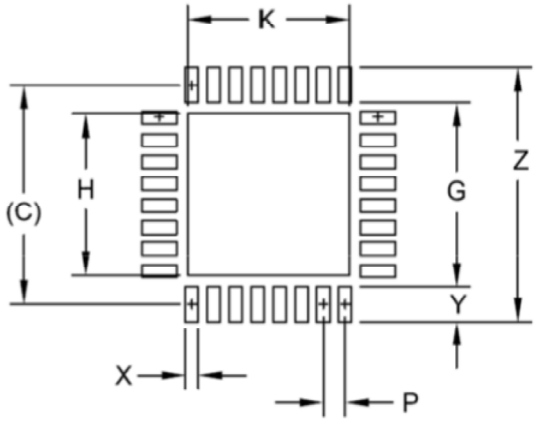
TOP MARK	
CHAR	ROWS
6/6/6/6	4

Marking for the 5 x 5 mm MLPQ 32 Lead package:

nnnnnn = Part Number (Example: LR1121)
yyww = Date Code (Example: 2052)
xxxxxx = Semtech Lot No. (Example: E90101
xxxxxx 0101-1)

5.3 Land Pattern

Figure 5-3: Land Pattern



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.197)	(5.00)
G	.165	4.20
H	.146	3.70
K	.146	3.70
P	.020	0.50
X	.012	0.30
Y	.031	0.80
Z	.228	5.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
3. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

5.4 Reflow Profiles

Reflow process instructions are available from the Semtech website, at the following address: *http://www.semtech.com/quality/ir_reflow_profiles.html*

The device uses a QFN32 5x5mm package, also named MLP package.

5.5 Thermal Information

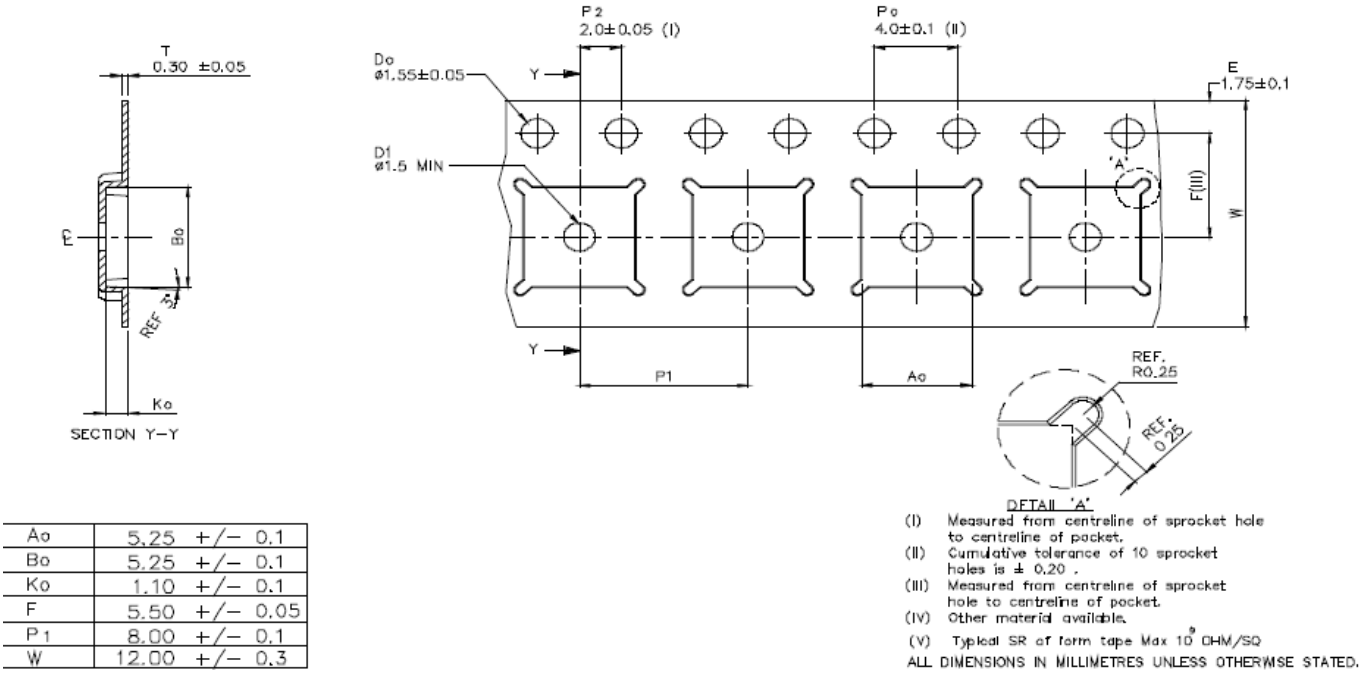
Table 5-1: Package Thermal Information

Name	Value[1]	Unit
Theta j-a, Junction to Ambient	26.7	°C/W

1. As measured on a 4-layer test board with 9 thermal vias, per the Jedec standard

5.6 Tape & Reel Information

Figure 5-4: Tape & Reel Information



Ao	5.25 +/– 0.1
Bo	5.25 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.05
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Glossary

List of Acronyms and their Meaning (Sheet 1 of 2)

Acronym	Meaning
ACR	Adjacent Channel Rejection
ADC	Analog-to-Digital Converter
AP	Access Point
β	Modulation Index
BER	Bit Error Rate
BR	Bit Rate
BW	BandWidth
BWF	FSK BandWidth
BWL	LoRa BandWidth
CPOL	Clock Polarity
CPHA	Clock Phase
CR	Coding Rate
CRC	Cyclical Redundancy Check
DC-DC	Direct Current to Direct Current Converter
DER	Detection Error Rate
DIO	Digital Input / Output
DSB	Double Side Band
ECO	Engineering Change Order
FDA	Frequency Deviation
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
IRQ	Interrupt Request
ISM	Industrial, Scientific and Medical (radio spectrum)
LDO	Low-Dropout
LNA	Low-Noise Amplifier
LoRa®	Long Range Communication The LoRa® Mark is a registered trademark of the Semtech Corporation

List of Acronyms and their Meaning (Sheet 2 of 2)

Acronym	Meaning
LR-FHSS	Long Range Frequency Hopping Spread Spectrum
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSK	Minimum-Shift Keying
NSS	Slave Select active low
PA	Power Amplifier
PER	Packet Error Rate
PLL	Phase-Locked Loop
POR	Power On Reset
RC13M	13MHz Resistance-Capacitance Oscillator
RC64k	64kHz Resistance-Capacitance Oscillator
RFO	Radio Frequency Output
RTC	Real-Time Clock
SCK	Serial Clock
SF	Spreading Factor
SPI	Serial Peripheral Interface
TCXO	Temperature-Compensated Crystal Oscillator
XOSC	Crystal Oscillator

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