MERIDIAN
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Meridian Innovation MI48xx Thermal Image Processor

Data sheet

Revision 4.0.5 – February 2023

Firmware compatibility: 4.2.3 or higher

Contents

1. DESCRIPTION

Meridian Innovation's MI48Dx is a specialised integrated circuit (IC) that is a companion to the MI0802 camera module featuring SenXor™ long-wave infrared (LWIR) imaging sensor. The MI48Dx handles the low-level control signalling necessary to capture raw sensor data from the thermal imaging array. It also provides standard interfaces for communication with a host controller.

The MI48Dx supports two different interfaces to the host system. One way to interface the host MCU is by the Inter-Integrated Circuit (I^2C) bus – for conveying commands to the MI48Dx and obtaining status from it, and serial peripheral interface (SPI) – for readout of thermal data. The alternative way is to interface the MI48Dx is by USB interface for communicating both control/status and thermal data. The communication protocol that must be used by the host application layer to exchange command-acknowledge type of messages is specified elsewhere.

Fig. 1 shows conceptual diagrams of systems that embed the SenXor™ camera module and the MI48Dx with I^2C and SPI interfaces, or alternatively, with USB interface.

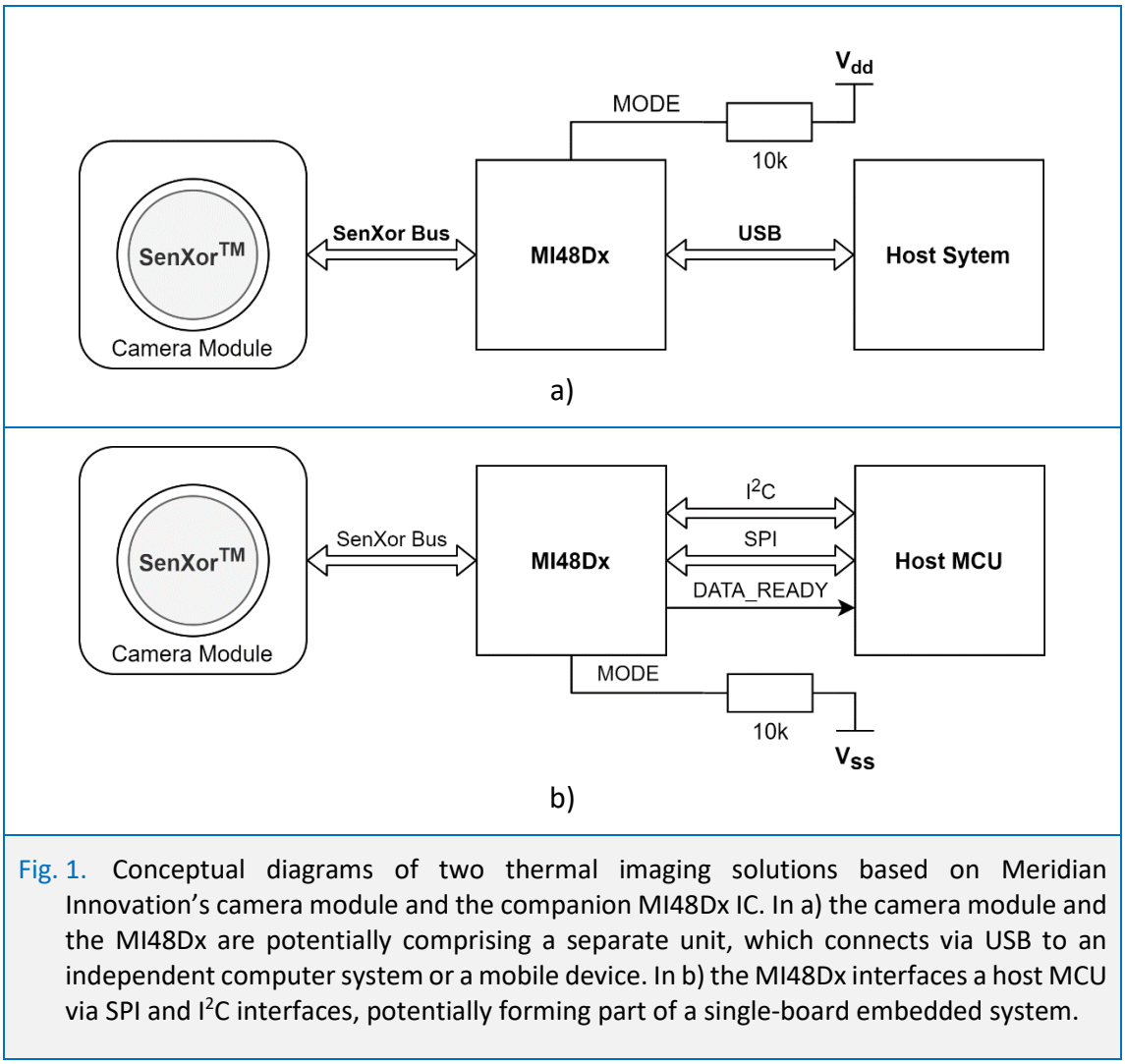


Fig. 1. Conceptual diagrams of two thermal imaging solutions based on Meridian Innovation's camera module and the companion MI48Dx IC. In a) the camera module and the MI48Dx are potentially comprising a separate unit, which connects via USB to an independent computer system or a mobile device. In b) the MI48Dx interfaces a host MCU via SPI and I^2C interfaces, potentially forming part of a single-board embedded system.

The MI48Dx also performs low-level processing of the data read out from the camera modules. Specifically, it handles the per-pixel calibration, performs bad pixel correction (BPC), converts the raw camera data to temperature, and suppresses the noise inherent to the signals coming from the pixels. In this way it greatly facilitates the development of applications embedding the SenXor™ thermal imaging sensor.

The MI48Dx is housed in a 5 mm by 5 mm, 32-pin leadless package featuring an exposed bottom thermal pad – quad flat no-lead QFN33.

2. ORDER INFORMATION

Table 1. ORDERING INFORMATION

Product Code	Package	Firmware Version	Interface	Min. Quantity
MI48D4	QFN33 (plastic, quad-flat, no-leads, thermal ground pad at the bottom)	4.2.3 or higher	SPI/I²C and USB	100

3. PINOUT INFORMATION

3.1. Pin Configuration – MI48Dx

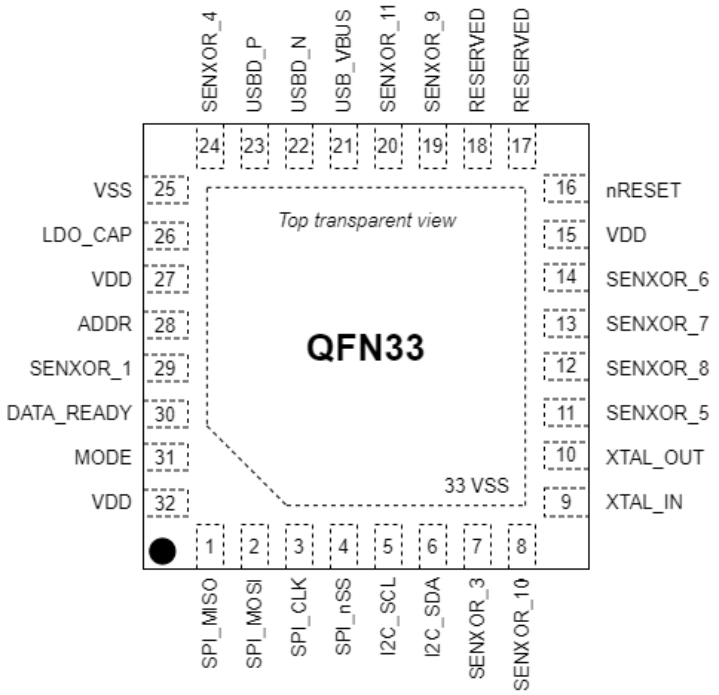


Fig. 2. MI48Dx QFN33-pin Diagram. The pinout features both USB and SPI/I²C interfaces, only of them must be configured for operation.

3.2. Pin Description

Table 2. Pin Description of MI48Dx [1)]

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	SPI_MISO	O	Master Input Slave Output of the SPI bus.
2	SPI_MOSI	I	Master Output Slave Input of the SPI bus.
3	SPI_CLK	I	Serial Clock of the SPI bus.
4	SPI_nSS	I	Slave Select of the SPI bus.
5	I2C_SCL	I	Clock line of the I²C bus.
6	I2C_SDA	I/O	Data line of the I²C bus.
7	SENXOR_3	I/O	SenXor Bus. Connect directly to camera module pin: SENXOR_3.
8	SENXOR_10	I/O	SenXor Bus. Connect directly to camera module pin: SENXOR_10.
9	XTAL_IN	I	External 12MHz crystal input. Connect through a 18pF capacitor to ground, or as recommended for the specific external crystal in use.
10	XTAL_OUT	O	External 12MHz crystal output. Connect through a 18pF capacitor to ground, or as recommended for the specific external crystal in use.
11	SENXOR_5	I/O	SenXor Bus. Connect directly to camera module pin: SENXOR_5.
12	SENXOR_8	I/O	SenXor Bus. Connect directly to camera module pin: SENXOR_8.
13	SENXOR_7	I/O	SenXor Bus. Connect directly to camera module pin: SENXOR_7.
14	SENXOR_6	I/O	SenXor Bus. Connect directly to camera module pin: SENXOR_6.
15	VDD	P	Power supply. Nominal 3.3 V.
16	nRESET	I	Active low hardware reset.
17	RESERVED	-	Reserved pin. Do not connect.
18	RESERVED	-	Reserved pin. Do not connect.
19	RESERVED	-	Reserved pin. Do not connect. SENXOR_9 I/O for MI0801-type module.
20	SENXOR_11	I/O	SenXor Bus. Connect directly to camera module pin: SENXOR_11.
21	USB_VBUS	I	Power supply from USB host.
22	USBD_N	I/O	Full speed USB Data −.
23	USBD_P	I/O	Full speed USB Data +.
24	RESERVED	-	Reserved pin. Do not connect. SENXOR_9 I/O for MI0801-type module.
25	VSS	P	Ground.
26	LDO_CAP	P	Internal LDO output pin. Connect through a 2.2uF capacitor to ground.
27	VDD	P	Power supply. Nominal 3.3V.
28	ADDR	I	I²C chip address select.
29	SENXOR_1	I/0	SenXor Bus. Connect directly to camera module pin: SENXOR_1.
30	DATA_READY	O	Data Ready output, active high.
31	MODE	I	Host Interface Mode Select, sensed during active low reset: Pull up (via 10kΩ resistor) – select USB interface Pull down (via 10kΩ resistor) – select SPI/I²C interface.
32	VDD	P	Power supply.
33	VSS	P	Thermal pad. Connect to ground.

[1)] The term ‘camera module’ in Table 2 and Table 3 refers to the MI08XXX camera module.

3.3. Special Pin Handling

Table 3. PIN TERMINATION – MI48DX

Pin No	Pin Name	Termination	Value
5	I2C_SCL	Pull up	4.7 kΩ
6	I2C_SDA	Pull up	4.7 kΩ
16	nRESET	Pull up resistor, plus a pull down capacitor to drive the line low during power up	10 kΩ, 10 μF
26	LDO_CAP	Connect to capacitor	2.2uF
30	DATA_READY	Pull down	10 kΩ
31	MODE	Pull down or pull up	10 kΩ 10 kΩ

4. FUNCTIONAL DESCRIPTION

4.1. Architectural Overview

Fig. 4 shows the internal block diagram of the MI48Dx and the interfaces that enable the control of acquisition and readout of thermal data.

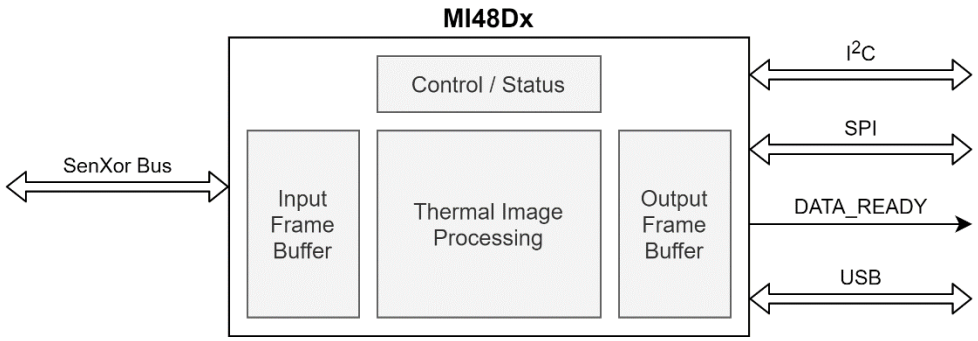


Fig. 3. Block diagram of the MI48Dx. The chip features both USB and SPI/I²C interfaces, only of them must be configured for operation.

4.1.1. SenXor Bus Interface

The SenXor Bus interface serves for capturing raw data from the thermal image sensor.

4.1.2. I²C Bus Interface

In the MI48Dx the slave I²C interface provides software access to the internal registers of the Control and Status block of the MI48Dx.

4.1.3. SPI Interface

In MI48Dx, the slave SPI interface serves to read out a temperature data frame from the Output Frame Buffer, indicated by DATA_READY output signal, as shown in Fig. 6.

4.1.4. USB Interface

In the MI48Dx the USB interface serves for conveying both control and status information, as well as readout of the temperature data from the Output Frame Buffer. The communication via USB relies on a specific protocol which must be implemented at the application layer of the host system; The reference manual can be found on Meridian Innovation's web-site.

4.1.5. Data Frame Buffers and Thermal Image Processing

The Input and Output Frame Buffers allow the dynamics of thermal data capturing via the SenXor Bus to be decoupled from the dynamics of thermal data readout via the SPI interface, and to realise data frame averaging of software-controlled depth as an elementary noise reduction technique. The low-level Thermal Image Processing applies per-pixel calibration and bad pixel correction based on calibration data stored in the camera module, and translates the raw sensor data to temperature in degrees Kelvin. Further noise reduction can be programmatically enabled to reduce the fluctuations in the temperature readout of individual pixels, which leads to a more stable readout and allows for an enhanced image upon visualisation of the thermal data.

4.2. MI48Dx Register Map

The MI48xx has several software-accessible registers that allow the control of thermal image capture and readout, the establishment of a power-down state, as well as obtaining relevant status information from the camera module and the MI48Dx itself.

The registers are summarized in Table 6 and are accessible only via the I^2C interface.

Table 4. REGISTER MAP

Register Name	Address	Access Type	Description
FRAME_MODE	0xB1	RW	Control the capture and readout of thermal data
FW_VERSION_1	0xB2	R	Firmware Version (Major, Minor)
FW_VERSION_2	0xB3	R	Firmware Version (Build)
FRAME_RATE	0xB4	RW	Frame rate
POWER _DOWN_1	0xB5	RW	Control of power down parameters
STATUS	0xB6	R	Status of the attached camera module and MI48xx interface operations

CLK_SPEED	0xB7	RW	Control of internal clock parameters
MODULE_GAIN	0xB9	RW	Module gain control
MODULE_TYPE	0xBB	R	Module type (chip-lens combination)
SENSITIVITY_FACTOR	0xC2	RW	Sensitivity correction factor
SELF_CALIBRATION	0XC5	RW	Self-Calibration of column offset
EMISSIVITY	0xCA	RW	Emissivity value for conversion of SenXor™ data to temperature
OFFSET_CORR	0xCB	RW	Fixed temperature shift of the entire frame for fine tuning the accuracy at product level
SENXOR _ID	0xE0 – 0xE5	R	Serial number of the attached camera module
FILTER_CONTROL	0xD0	RW	Filter configuration and control
FILTER_SETTING_1	0xD1 – 0xD2	RW	Parameters for the temporal filter
FILTER_SETTING_2	0xD3	RW	Parameters for the rolling average filter
USER_FLASH_CTRL	0xD8	RW	Enable/Disable host access to User Flash

4.3. Detailed Register Description

Table 5. FRAME_MODE (0xB1)

Addr.	0xB1	**Reset Value**	0x20
Bits	**Field Name**	**Access**	**Description**
0	GET_SINGLE_FRAME	RW	Setting this bit to 1 leads to the acquisition of a single frame. This bit is automatically reset to 0 after the acquisition of one frame. Note that writing 1 to this bit prior to it being auto-reset and prior to DATA_READY going high will restart the frame acquisition. DATA_READY will remain low until the data from the restarted acquisition is available in the output buffer.
1	CONTINOUS_STREAM	RW	Setting this bit to 1 instructs the MI48xx to operate in Continuous Capture Mode, whereby it continuously acquires data from the camera module and updates the readout buffer accessible through the SPI interface. Resetting this bit to 0 instructs the MI48xx to stop continuous data acquisition. This also resets to 0 the DATA_READY pin and the corresponding bit 4 of the STATUS register.

2-4	READOUT_MODE	RW	Configure the readout mode of the output frame buffer, accessible through the SPI interface. Currently only Full-Frame Readout Mode is implemented, where the host controller can read out the frame only when it is captured and processed in its entirety. Values: 0 – Full-Frame Readout Mode 1 to 7 – Reserved.
5	NO_HEADER	RW	Setting this bit to 1 eliminates the Header from the Thermal Data Frame transferred through the SPI interface. Resetting this bit to 0 includes the HEADER in the Thermal Data Frame, as shown in Section 4.6.
6-7	RESERVED	-	Not accessible.

Table 6. FW_VERSION_1 (0xB2)

Addr.	0xB2	**Reset Value**	As per FW Version
Bits	**Field Name**	**Access**	**Description**
0-3	MINOR	R	Minor Firmware Version Number
4-7	MAJOR	R	Major Firmware Version Number

Table 7. FW_VERSION_2 (0xB3)

Addr.	0xB3	**Reset Value**	As per FW Version
Bits	**Field Name**	**Access**	**Description**
0-7	BUILD	R	Firmware build number

The Firmware version is represented as MAJOR.MINOR.BUILD. The three numbers are stored in FW_VERSION_1 and FW_VERSION_2, as per Table 8 and Table 9 above.

Table 8. FRAME_RATE (0xB4)

Addr.	0xB4	**Reset Value**	0x04
Bits	**Field Name**	**Access**	**Description**
0-6	FRAME_RATE_DIVIDER	RW	The value of these bits establishes the rate at which the host controller can read out thermal data frame from the Output Frame Buffer through the SPI interface. The value must be an unsigned integer representing the frame rate divisor of the maximum frame rate, FPS_MAX, of the attached camera module: FPS = FPS_MAX / FRAME_RATE_DIVIDER. Exception is FRAME_RATE = 0, which yields FPS_MAX.
7	RESERVED	-	Not Accessible

Table 9. SLEEP_MODE (0xB5)

Addr.	0xB5	Reset Value	0x00
Bits	**Field Name**	**Access**	**Description**
0-5	SLEEP_PERIOD	RW	The length of time during which the MI48xx and the attached SenXor™ camera module stay in low power mode (sleep mode) after every frame that has been read out through the SPI interface. The value represents time in units of 10 milliseconds, or time in units of 1 s if PERIOD_X100 (bit 6) is set.
6	PERIOD_X100	RW	When this bit is set, the value of SLEEP_PERIOD is in units of 1 s.
7	SLEEP	RW	When this bit is set to 1 the MI48xx will power down the SenXor™ Camera Module and will enter low power sleep mode itself immediately after. The bit is automatically reset to 0 if MI48xx is addressed via the I²C interface, upon which the chip exits sleep mode and powers up the camera module.

If the MI48Dx is configure to communicate with host MCU via SPI/I²C interface, then, the chip supports two low power modes – host-control and automatic.

In host-control mode, the host system dictates when the MI48Dx enters and exits sleep mode and for how long it remains in that mode. This is accomplished by setting bit 7 of SLEEP_MODE (0xB5) register – to enter sleep mode, and by accessing any of the MI48Dx registers via the I²C interface – to exit sleep mode. Note that the host system does not need to explicitly reset bit 7 of SLEEP_DOWN register; a read or write to any other register automatically resets this bit to 0. After exiting sleep mode, the host must wait for 50 ms before initiating frame capture.

For automatic sleep mode control, the host must only set the duration of the sleep periods by setting a non-zero sleep period – bits 0 – 5 of the SLEEP_MODE register. The MI48xx will automatically enter sleep mode at the end of a frame readout. Upon wake up, the MI48xx will wait for 50 ms before initiating frame capture.

This register should not be used if the MI48Dx is configured for USB communication with the host MCU.

Table 10. STATUS (0xB6)

Addr.	0XB6	Reset Value	0x00
Bits	**Field Name**	**Access**	**Description**
0	RESERVED	-	Not accessible
1	READOUT_TOO_SLOW	R	Reads 1 if the last frame was not readout within the time-period reciprocal to the maximum frame rate of the attached camera module. Relevant only in Continuous Capture Mode (see

			bit 1, CONTINUOUS_STREAM, of register FRAME_MODE, 0xB1). Reads 0 otherwise. Auto-reset upon read. Supported only in SPI/I^{2}C mode.
2	SENXOR_IF_ERROR	R	Reads 1 if an error was detected on the SenXor interface during power up of the MI48xx.
3	CAPTURE_ERROR	R	Communication error on the SenXor interface during thermal data capture.
4	DATA_READY	R	This bit reflects the state of the DATA_READY pin, and is intended to be polled by a system that cannot have a hardware connection to the DATA_READY pin. Note however, that when this bit is polled continuously without delay it might cause a drop in the data frame rate. Therefore, it is recommended to introduce a few milliseconds delay between successive polls.
5	BOOTING_UP	R	Reads 1 if the MI48xx is still booting up. Reads 0 after the MI48xx completes its boot up process. Once it reads zero, write to other registers is allowed, and frame capture can start.

Note: If any of the error flags above is raised, the frame capture stops. Upon reding the register, all error flags are cleared.

Table 11. CLK_SPEED (0xB7)

Addr.	0xB7	**Reset Value**	0x02
Bits	**Field Name**	**Access**	**Description**
0	CLK_SLOW_DOWN	RW	Setting this bit to 0 reduces the internal clock speed of the MI48xx by a half, and leads to a reduction of its dynamic power by approximately the same factor.
1-7	RESERVED	-	Not accessible.

Table 12. GAIN_SELECTION (0xB9)

Addr.	0XB9	**Reset Value**	0x00
Bits	**Field Name**	**Access**	**Description**
0-3	MODULE_GAIN	RW	These bits define the common amplification of the signal generated by each pixel in the SenXor array. The increased amplification improves signal to noise ratio but at the same time limits the range of scene temperatures that can be reported. By default, the sensor module is set at its maximum gain, considered to have a value of 1. Alternatively, the

			gain my be lowered to 0.5 or 0.25 times the maximum gain, in order to increase the observed scene temperature, according to the following: 0 – Default, maximum gain of 1. 1 – AUTO -- Automatic gain selection (one of 1.0, 0.5, 0.25), depending on the detected dynamic range of the input signal 2 – Quarter gain of 0.25 3 – Half gain of 0.5 4 – Maximum gain of 1.0 5 to 15 – Reserved. If MODULE_GAIN is set to AUTO, then reading this register will return the currently selected value.
4-7	RESERVED	-	Not accessible.

Table 13. MODULE_TYPE (0xBB)

Addr.	0xBB	**Reset Value**	As per attached camera module
Bits	**Field Name**	**Access**	**Description**
0-7	MODULE_TYPE	RW	Module type, defined by the combination of SenXor chip type and specific lens, according to Appendix I. The value of this register is typically pre-set during factory calibration of the module. However, for self-calibrated modules, the user must write the correct value before initiating the self-calibration process.

Table 14. SENSITIVITY_FACTOR (0xC2)

Addr.	0xC2	**Reset Value**	Read back from attached camera module and depends on its calibration.
Bits	**Field Name**	**Access**	**Description**
0-7	CORR_FACTOR	RW	Multiplicative factor to the temperature readout of every pixel, allowing correction of the sensitivity, e.g. when a protective filter is placed in front of the thermal camera lens.

Table 15. SELF-CALIBRATION (0xC5)

Addr.	0xC5	**Reset Value**	0x00
Bits	**Field Name**	**Access**	**Description**
0	RESERVED	R	Not used
1	START_COLOFFS_CALIB	RW	Setting this bit to 1 initiates column offsets calibration.

			The bit is automatically set during power up and upon a change in MODULE_GAIN (either manual or automatic).
2	COLOFFS_CALIB_ON	R	After setting START_COLOFFS_CALIB to 1, COLOFFS_CALIB_ON bit reads 1 throughout the process of column offsets calibration. Once the process is complete, this bit read 0.
3	RESERVED	R	Not used
4	USE_SELF_CALIB	RW	If set to 1, the module will not use module-specific calibration data. It will use instead the data obtained during column offset calibration, and predefined generic data for the given chip and lens combination. NOTE: the user must write the correct value of MODULE_TYPE to register 0xBB, in order to achieve a reliable self-calibration operation. In any case, the use of self-calibration cannot be as good as the factory calibration, which is done for each individual module
5-7	SAMPLE_SIZE	RW	These bits define the number of frames acquired during column calibration, according to the formula: (SAMPLE_SIZE + 1) x 100. That is a value of 0 results in 100 frames being acquired, and a value of 7 results in 800 frames being acquired.

Table 16. EMISSIVITY(0xCA)

Addr.	0xCA	**Reset Value**	0x5F (95 decimal value)
Bits	**Field Name**	**Access**	**Description**
0-7	EMISSIVITY	RW	Emissivity value (percent) to be used in the conversion of raw data captured from SenXor to the temperature data that is readout through the SPI interface. The reset value reflects the emissivity of the black body source used for factory calibration of the camera module. If the target object is known to have a different emissivity, programming the correct value will lead to an accurate readout of the absolute temperature.

Table 17. OFFSET_CORR (0xCB)

Addr.	0xCB	**Reset Value**	0x00
Bits	**Field Name**	**Access**	**Description**
0-7	OFFSET	RW	This register represents a temperature offset that will be added to every pixel in the data frame before it is sent

			out to the host system. The value is expressed in 2's complement notation (8-bit signed integer) in units of 0.1 K. This allows for fine tuning any bias in the temperature readout by as much as $+/-12.7$ K with, with 0.1 K increments.
			For example, to correct an apparent bias of 0.7 K, we must add -0.7 K to the data frame, hence write 241 (0xF9) to 0xCB. Conversely, if the apparent offset is -0.75 we must add 0.75 K, hence write 7 (0x07) to 0xCB. The following Python code may be used as a reference for calculating the OFFSET value (n, below):
			
			`def value_0xCB(observed_error, unit=0.1):`
			`  """Calculate necessary value of 0xCB`
			`  to correct for observed error"""`
			`  # the offset to be applied is of`
			`  # opposite sign to the error`
			`  n = - int(round(observed_error/unit))`
			`  if n < 0:`
			`  return 256 - abs(n)`
			`  else:`
			`  return n`

Table 18. SENXOR_ID (0xE0—0xE5)

Addr.	0xE0 – 0xE5	**Reset Value**	As per SenXor's unique ID
Bits	**Field Name**	**Access**	**Description**
0 - 7	PRODUCTION_YEAR	R	Production year (19 – 99) – decimal offset since year 2000, i.e. 19 == 2019
8 – 15	PRODUCTION_WEEK	R	Production week (decimal 1 – 52)
15 – 23	MANUF_LOCATION	R	Manufacturing location (decimal 0 – 99)
24 – 63	SERIAL_NUMBER	R	Serial number of the camera module. This number may roll over, but only at the beginning of a new PRODUCTION_WEEK.

The SENXOR_TYPE and SENXOR_ID uniquely identify every single camera module produced by Meridian Innovation.

Table 19. FILTER_CONTROL (0xD0)

Addr.	0xD0	**Reset Value**	0x00
Bits	**Field Name**	**Access**	**Description**
0	TEMPORAL_ENABLE	RW	Enable temporal data filtering when set to 1. The effect of this filter is determined by the value of register FILTER_SETTING_1 (0xD1 – 0xD2). The higher the value – the more stable the readout temperature, but also – the more noticeable trailing artefacts in a dynamical

			scene. Note that the use of the temporal filter in conjunction with bit 0 of CLK_SPEED register, CLK_SLOW_DOWN, leads to a reduction in the data frame rate.
1	TEMPORAL_INIT	RW	Initialize temporal filter, when set to 1. This bit must be set to one whenever a new value is written to register FILTER_SETTING_1 (0xD1 – 0xD2), in order for the new setting to take effect. The bit will be automatically reset to 0 after the initialisation is complete, which typically takes around 40 ms.
2	ROLL_AVG_ENABLE	RW	Enable rolling average filter when set to 1. The effect of this filter is influenced by the value of register FILTER_SETTING_2 (0xD3).
3-4	RESERVED	-	Not accessible.
5	MEDIAN_KERNEL_SELECT	RW	0 – median filter with a kernel size of 3 1 – median filter with a kernel size of 5
6	MEDIAN_ENABLE	RW	Enable median filter with the kernel size according to the MEDIAN_KERNEL_SELECT bit
7	RESERVED	-	Not accessible.

Table 20. FILTER_SETTING_1 (0xD1—0xD2)

Addr.	0xD1 – 0xD2	**Reset Value**	0x32 (decimal 50)
Bits	**Field Name**	**Access**	**Description**
0 - 7	TEMPORAL_LSB	RW	Least significant 8 bits of the filter strength
8 – 15	TEMPORAL_MSB	RW	Most significant 8 bits of the filter strength

Note that to reproduce the image quality similar to the GUI supplied with the evaluation kit for MI0801 camera module, one must use 125 in FILTER_SETTING_1.

Table 21. FILTER_SETTING_2 (0xD3)

Addr.	0xD3	**Reset Value**	0x04 (decimal 4)
Bits	**Field Name**	**Access**	**Description**
0 - 7	NUM_FRAMES	RW	Number of frames N, over which to perform the rolling average. The readout value $\bar{T}_i$ of a pixel at frame i, is given by the formula: $\bar{T}_i = \bar{T}_{i-1} + \frac{1}{N}(T_i - \bar{T}_{i-1})$, where T_i is the latest measured pixel value, and $\bar{T}_{i-1}$ is the readout value at the previous frame.

Table 22. USER_FLASH_CTRL (0xD8)

Addr.	0xD8	Reset Value	0x00
Bits	**Field Name**	**Access**	**Description**
0	USER_FLASH_ENABLE	RW	When set to 1, enable host to access User Flash via the I2C interface, using register-like byte-access, starting from address 0x00 to address 0x7F inclusive. Once User Flash access has been complete, the host must clear this bit to 0, to regain access to the standard MI48 registers.
1-7	RESERVED	-	Not accessible

4.4. SenXor Bus Interface

The SenXor Bus Interface serves to control the camera module and capture the raw data from the thermal image sensor. The designated pins on the MI48Dx must be directly connected to the corresponding pins on the MI0802 camera modules. The operation of this interface is entirely controlled by the firmware of MI48Dx, which facilitates the design of the host system.

4.5. I²C Bus Interface

The I²C interface provides access to the internal register map of the MI48Dx. The following communication protocol is implemented over the I²C interface of the MI48Dx, whereby communication is always initiated by the master device on the I²C bus, while the MI48Dx acts as a slave device on the I²C bus.

4.5.1. I²C Slave Address

The I²C slave address is composed of 7 bits – A6 to A0. For the MI48Dx bit A6 to A2 are hardwired to '10000', while bit A0 depends on the value registered on the ADDR input pin (pin 22 of the QFN33 package) during hardware reset or power-on reset. Therefore, the MI48Dx can respond to one of two I2C slave addresses, as per Table 22.

Table 23. SELECTION OF I²C SLAVE ADDRESS.

ADDRESS state	I²C chip address
0 (Pull Low)	0x40
1 (Pull High)	0x41

4.5.2. I²C Command

The I²C command consists of 1 byte that includes the 7-bit I²C slave address (A6 to A0), followed by one-bit access type designator $(R/\overline{W})$ – 1 for read access and 0 for write access:

A6	A5	A4	A3	A2	A2	A0	$R/\overline{W}$

Specifically, for the MI48Dx it is:

1	0	0	0	0	0	A0	$R/\overline{W}$

4.5.3. Write Command

- Master initiates a write command by a Start Condition (S), followed by one byte containing Slave Address in the first 7 bits (A6 to A0), and 0 in the last bit.
- Upon acknowledge (A) from slave, master sends one byte with Slave Internal Register Address (B7 to B0) – the register it intends to write to.
- Upon acknowledge from slave (A), master sends one byte of register data (D7 to D0) to be written to the slave.
- Upon acknowledge from slave (A), master terminates the transfer with a Stop Condition (P).

This is summarised below – the shaded fields indicate Slave driving the I²C_SDA line:

S	A6	A5	A4	A3	A2	A2	A0	0	A	B7	B6	B5	B4	B3	B2	B1	B0	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

4.5.4. Read Command

- Master initiates a read command by a Start Condition (S), followed by one byte containing Slave Address in the first 7 bits, (A6 to A0) and 0 in the last bit.
- Upon acknowledge (A) from slave, master sends one byte with Slave Internal Register Address (B7 to B0) – the register it intends to read from.
- Upon acknowledge from slave (A), master sends a Repeated Start Condition (RS) followed by one byte containing Slave Address in the first 7 bits, (A6 to A0) and 1 in the last bit
- Slave then sends Acknowledge (A) followed by the one byte of data (D7 to D0).
- Once the master receives the number of bytes it expects from the slave, the master issues Not-Acknowledge (NA) and terminates the transfer with a Stop Condition (P).

This is summarised below – the shaded fields indicate Slave driving the I²C_SDA line:

S	A6	A5	A4	A3	A2	A2	A0	0	A	B7	B6	B5	B4	B3	B2	B1	B0	A	
RS	A6	A5	A4	A3	A2	A2	A0	1	A	D7	D6	D5	D4	D3	D2	D1	D0	NA	P

The MI48Dx supports multiple reads, whereby the internal register address is automatically incremented if the Master sends Acknowledge (A) instead of Not-Acknowledge (NA), indicating that it is ready to receive more data.

4.6. SPI Interface

The SPI interface enables the host processor to read out the thermal data frame assembled by the MI48Dx. The thermal data frame is held in the Output Frame Buffer of the chip and its availability is indicated by the DATA_READY output signal.

4.6.1. SPI Interface Operation

The MI48Dx acts as an SPI slave. The SPI interface master must be operated in Mode 0. Therefore, the SPI_CLK idles at 0, and a clock cycle corresponds to a half cycle with the clock idle, followed by a half cycle with the clock asserted at 1. The leading and trailing edges of the clock are the rising and falling edges of SPI_CLK correspondingly. This is illustrated in Fig. 5.

The SPI Interface master should be configured to use 16-bit data width, with the most significant bit (MSB) transferred first. It does not matter if the SPI master (on the host system) releases the SPI_SS between reads of consecutive words of the same thermal data frame.

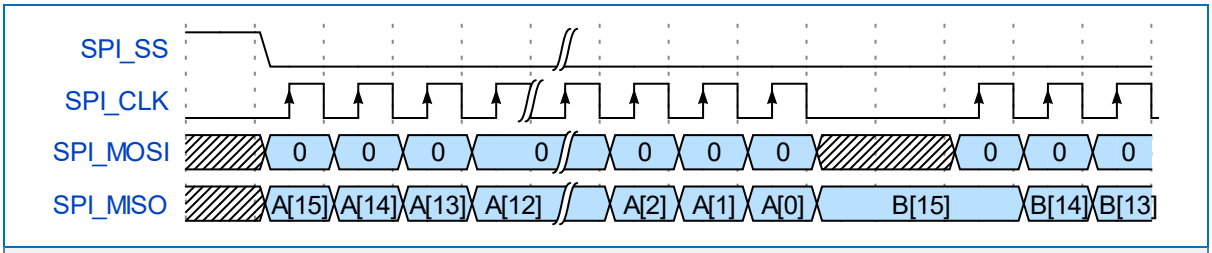


Fig. 4. Waveform diagram of the thermal data readout through the SPI Interface; A and B refer to the first and second 16-bit words of the data transfer. Vertical dotted lines delineate clock cycles.

Note that for every 2 bytes read from MI48Dx by the host controller over the SPI, the host must write two dummy bytes with the value 0x0000 over the MOSI pin in order to generate the clock for the SPI transfer.

4.6.2. Thermal Data Frame Format

The format of the Thermal Data Frame depends on the value of bit 5 – NO_HEADER of the FRAME_MODE register (0xB1). If NO_HEADER is set to 1, the Data Frame contains only the temperature data, and that is the only data transferred over the SPI interface. Alternatively, the data frame consists of a Frame Header, which is transferred first, followed by the temperature data. The data frame format in this case is shown in Table 23.

Table 24. THERMAL DATA FRAME FORMAT INCLUDING HEADER

Frame Header 80 words (MI08XX)	**Frame counter** 1 word	**SenXor VDD** 1 word	**SenXor die temperature** 1 word	**Time stamp** 2 words	**Max pixel value** 1 word	**Min pixel value** 1 word	**CRC** 1 word	**Reserved** 72 words (MI08XX)
Tempe-rature data	80 column * 62 row Pixel Data, i.e. 4960 words (MI0802 Camera Module)							

4.6.3. Thermal Data Frame Header Details

The header of the Thermal Data Frame consists of 80 words. Each word is composed of 16 bits, of which the most significant bit (MSB) is transferred first, and the least significant bit is transferred last. Only the first 8 words of the header are significant, as detailed in Table 24. Each word represents an unsigned integer.

Table 25. THERMAL DATA FRAME HEADER

Header Byte offset	Size, Bytes	Tag	Description
0	2	Frame counter	Number of frames taken from the since last power up. The value increments by 1 every time a frame is available for readout by the host.
2	2	SenXor VDD	Internal VDD sensed by the MI08XX Camera Module, in unit of 0.0001 V, i.e. 32945 equals 3.2945 V
4	2	SenXor die temperature	Internal die temperature of the connected MI08XX, in units of 0.01 K, i.e. 34001 = 340.01 K
6	4	Time stamp	Time elapsed since first frame was taken. Note that elapsed time is tracked using the external 12 MHz crystal oscillator, which is not as accurate as a standard 32kHz crystals for timing applications.
10	2	Max pixel value	Maximum pixel value of captured frame in units of 0.1 K, i.e. a decimal value of 3304 equals 330.4 K
12	2	Min pixel Value	Minimum pixel value of captured Frame in units of 0.1 K, i.e. a decimal value of 2735 equals 273.5 K
14	2	CRC	Check sum CRC-16/CCITT-FALSE calculated over the thermal data portion of the frame only. Note that the CCITT-FALSE variant of CRC-16 has the following parameters: width=16, poly=0x1021, **init=0xFFFF**, refin=False, refout=False, xorout=0x0000, check=0x29b1, residue=0x0000

4.6.4. Temperature Data

The temperature data consists of 4960 words. Each word is composed of 16 bits, and the most significant bit is transferred first. Every word represents the temperature of a pixel, as a 16-bit unsigned integer in units of 0.1 K.

For example, the transfer of the 16-bit word 0x0BC1, represents 3009 in decimal and the corresponding temperature is 300.9 K.

4.7. USB Interface Operation

The MI48Dx implements a USB interface that can be used as an alternative mode of communication to the host MCU. This mode of operation is select by pulling up the MODE pin (pin 31), which is sensed during reset. The host MCU must realise an interface protocol featuring command-acknowledge exchange of commands and data. The interface protocol is specified the document MI48xx-USB-Interface-Protocol by Meridian Innovation. The electrical signalling is compliant to the USB standard, which can be used as a reference, and the physical coupling can be done by USB-C a connector.

4.8. Thermal Data Acquisition

The MI48xx supports two data acquisition modes – Single Frame Capture, and Continuous Frame Capture. The capture mode depends on how the capture mode is initiated.

Single Frame Capture mode is triggered by setting to 1 GET_SINGLE_FRAME (bit 0) of MODE_REGISTER (0xB1) , and is appropriate when one needs to acquire thermal images at relatively large intervals from one another, e.g. once every 10 min. In such case, it is useful to also set the frame rate to a low value, e.g. by setting the FRAME_RATE_DIVIDER in the FRAME_RATE register at address 0xB4 to the value of 0x20. In this way one can benefit from the noise reduction within the MI48xx itself, so that the obtained thermal data requires minimal processing. GET_SINGLE_FRAME is automatically reset to 0.

Continuous Capture mode is initiated by setting to 1 CONTINUOUS_STREAM (bit 1) of MODE_REGISTER (0xB1). MI48xx obtains a continuous stream of thermal images from the attached camera module and delivers the processed thermal data frames to the Output Frame Buffer at the frame rate specified by the FRAME_RATE_DIVIDER in the FRAME_RATE register at address 0xB4. To stop the continuous data acquisition, one must reset CONTINUOUS_STREAM to 0.

4.9. Thermal Data Readout

4.9.1. General Considerations

The MI48xx supports Full-Frame readout mode, in which the host processor can read the entire Thermal Data Frame – including Frame Header and the Temperature Data of the entire SenXor™ pixel array. In the case of the MI48Dx being configured to communicate via SPI/I^2C interface this can happen upon the rise of the DATA_READY output signal from

the MI48xx. This is illustrated in Fig. 6, where the data transfer over the SPI interface is abstractly represented.

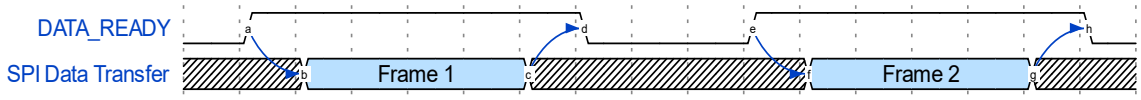


Fig. 5. Abstract timing relation between the DATA_READY timing and the readout of the thermal image data from MI48Dx.

Note that DATA_READY is lowered only after the host controller reads out the complete Thermal Data Frame.

In the case of the MI48Dx being configure to communicate via USB, the message containing the thermal data frame will be composed and sent out via the USB interface as soon as it is complete.

4.9.2. Low Power Considerations

In Continuous Capture Mode (bit 1, CONTINOUS_STREAM of the FRAME_MODE register 0xB1 set to 1), the actual rate of thermal data frame availability depends on two things: a) the value of the FRAME_RATE_DIVIDER in register 0xB4, and b) the values of the SLEEP_PERIOD in the SLEEP_MODE register 0xB5. Specifically, for the MI48Dx, the period between two assertions of DATA_READY equals the inverse FPS in milliseconds plus the power-down period in millisecond. An example is shown in Table 25. In the case of the USB communication interface, the period between two consecutive messages with data frames transferred via the USB interface is similarly elongated.

Table 26. DATA_READY PERIOD

Frame Rate [FPS]	SLEEP PERIOD [ms]	DATA_READY period [ms]
7.5	0	132
7.5	100	232

4.10. Low-level Thermal Data Processing

4.10.1. Per Pixel Calibration

Each SenXor™ module is factory-calibrated per pixel, so that accuracy and uniformity of temperature readout is achieved. The calibration data is accessed by the MI48xx, when connected to a camera module and used in the process of converting the output from the camera module into absolute temperature (in Kelvin).

4.10.2. Bad Pixel Correction

Each SenXor™ module is calibrated per pixel, and any bad pixel is identified during the calibration procedure. Within the MI48xx the readout value of the identified bad pixels is replaced by an appropriate estimate, based on the temperature of surrounding good pixels, automatically.

4.10.3. Camera Module Output to Temperature Conversion

The output of the camera module is readout by the MI48xx and converted into temperature after taking into account the calibration of the connected SenXor™, the emissivity value stored in the EMISSIVITY register at address 0xCA, and the emissivity correction factor stored in the EMISSIVITY_FACTOR register at address 0xC2.

4.10.4. Data Filtering

Data readout from each pixel of SenXor™ exhibit some fluctuations over time, particularly obvious at high frame rate. The MI48xx can smooth out these fluctuations to a different degree, depending on the application requirements for frame rate, readout stability and accuracy, and the anticipated dynamics of the scene to be observed by thermal imaging.

Image filtering can be performed in two distinct domains: in the time domain and in the spacial domain, as shown in the Fig. 7 below. The MI48 supports 2 different time-domain filters, Temporal Filter and Rolling Average Filter, as well as a Median Filter, for the spatial domain. Which one is turned on and off is dictated by the FILTER_CONTROL register at 0xD0. The operation of the filters is independent of each other and they can be ON at the same time.

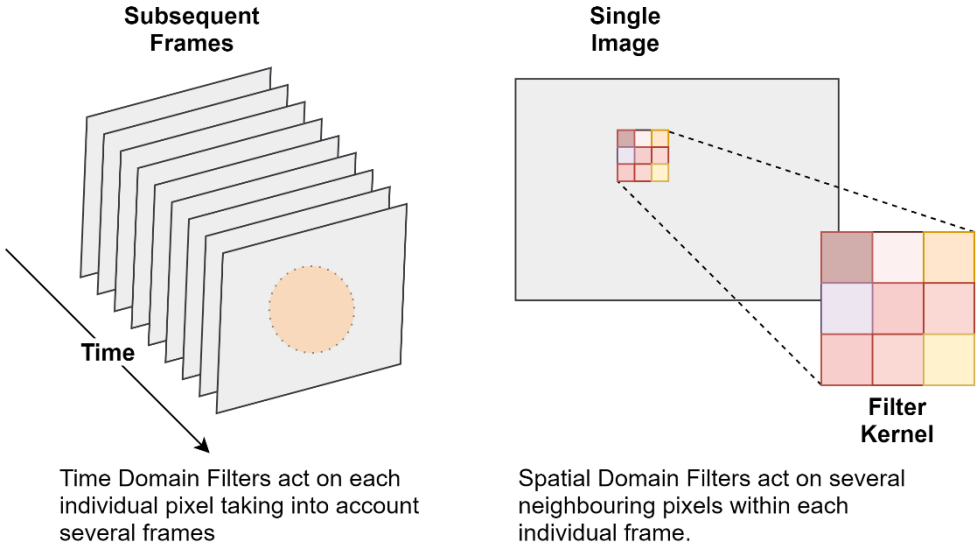


Fig. 6. Conceptual diagram of image denoising filters in the time-domain (left) and in the spatial domain (right).

Time-domain filters maintain the sharpness and features of the image because the denoising algorithm is applied on each pixel individually. However, time-domain filters

suffer from 'history' effects. That means that a sudden or fast change in the scene will result is a 'ghost'-like movement or change in the image over consecutive frames. The strength of the Temporal Filter and the depth of the Rolling Average Filter affect the amount of 'ghosting' and must be optimised for the specific application. This is done via the FILTER_SETTING_1 registers at address 0xD1 and 0xD2 (for the Temporal Filter), and via FILTER_SETTING_2 register at address 0xD3 (for the Rolling Average Filter). By default, the Rolling Average Filter is turned OFF, while the Temporal Filter is turned ON, and its default strength of 50 is optimal for a slowly changing scene at 9 FPS. Note that the Temporal Filter must be initialised whenever its strength is changed, via the 0xD0 register.

The median filter, which is OFF by default, is a spatial filter and does not introduce ghosting in the image, but potentially smooths out subtle features, particularly if the features in the scene are resolved in too few pixels. The Median Filter supports a kernel of 3 x 3 or 5 x 5 pixels, to avoid excessive smoothing. The selection of the kernel size is done by bit 5 of register 0xD0.

4.10.5. Self-Calibration

If the MI48Dx is connected to a SenXor module that is provided without an external flash memory to store calibration information, then the MI48Dx performs a self-calibration routine upon module power up, in order to minimize temperature offset between individual columns of the array. Additionally, the MI48Dx can use a generic calibration data for a given module type (related to the type of lens being used). For this to happen, the host MCU must initialize register MODULE_TYPE at address 0xBB with the correct module type (see Appendix I) and then activate the use of self-calibration by setting to 1 bit 4 of the SELF_CALIBRATION register at address 0xC5.

4.11. Module Gain Control

The module gain determines the range of scene temperatures that can be reported by the MI48Dx upon reading the data. The module gain is controlled via the MI48Dx, which supports two modes – manual and automatic gain control. By default, the chip is operating in manual gain control mode, with the gain that yields the highest sensitivity (lowest NETD) and best accuracy. This gain is normalized to a numerical value of 1. The user can reduce the gain to 0.5 (half-gain) or 0.25 (quarter gain) in order to expand the temperature range, via the MODULE_GAIN register at address 0xB9, according to the following table.

0xB9 - Auto / Manual Range				
Preset	Hex	Bit Value	Gain	Indicative Scene Temperature Range
OFF	0	0	1x (Default)	< 120
AUTO	1	1	1x - 0.25x	< 400
1	2	2	0.25x	200 - 400
2	3	3	0.5x	100 - 200
3	4	4	1x	< 120

Note that the temperature ranges below are only roughly indicative. In practice, the actual range depends on the type of lens used (e.g. module type) and the operational die temperature of the sensor.

Note also that after changing the gain manually, frame capture will stop for a few seconds.

In Automatic Gain Control Mode, the chip will perform a seamless transition between the temperature ranges. However, during the transition and for a few seconds after, the image quality and temperature accuracy may be compromised.

When Automatic Gain Control is ON, the value of the current gain can be obtained by reading register 0xC5.

Note that lowering the gain to 0.5 or 0.25 increases the NETD and reduces the accuracy of the temperature readout.

4.12. Accessing User Flash

The MI48 contains a 128-byte FLASH memory reserved for the user. This memory can be accessed byte-wise via the I2C interface. Its purpose is to store non-volatile data -- for example, end-product unit calibration data or identification codes. The byte addresses this flash memory enumerate from 0x00 to 0x7F, and is hereafter referred to as User Flash Address.

To access the User Flash for either read or write, the host must enable it by setting bit 0 of the USER_FLASH_CTRL register at address 0xD8. At that point, any attempt to access an address between 0x00 and 0x7F including will result in accessing the USER FLASH, i.e. any other MI48 registers that may be mapped to this address range will *not* be visible to the host. The memory map of the MI48 when User Flash access is enabled is shown in Fig. 8.

To resume access to all of the MI48 registers, the host must clear bit 0 of the USER_FLASH_CTRL register at address 0xD8, after completing the access (read or write) to the User Flash.

Note that making the User Flash accessible to the host via the I^2C interface implies a single byte access at a time, and the User Flash address and data are communicated just as any other access to the MI48 registers.

Specifically, for read access, the corresponding byte from the User Flash is placed in the I^2C data field.

For write access to the User Flash, the data from the I^2C command is written to the MI48 internal memory, and then it is actually written to the User Flash using a read-update-write sequence. The actual process of writing to the flash involves the copying of the original 128-byte content of the flash to the internal memory of the MI48, updating the relevant byte, then erasing the user flash memory, and finally writing the updated 128-byte contents from the MI48 internal RAM to the User Flash. This process is obviously rather time consuming and should not be performed during continuous frame acquisition.
In general, the usage of the User Flash should be avoided during data acquisition.
The intended usage is to store some parameters that are end-product specific, during test

and calibration of the unit. Then upon power up, the host should read these parameters if needed, before initiating data acquisition, and disable the User Flash thereafter.

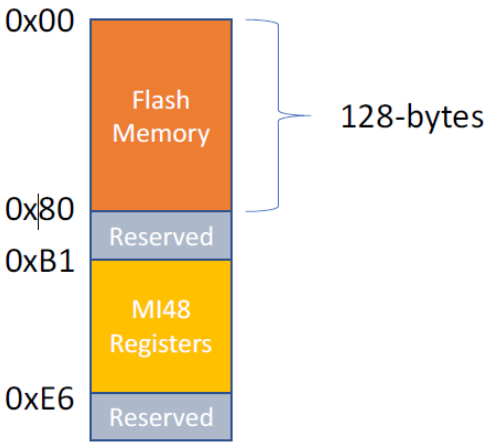


Fig. 7. Memory map of the MI48, showing the User Flash at address 0x00 – available only when bit 0 of the USER_FLASH_CTRL is set to 1.

5. ELECTRICAL AND THERMAL CHARACTERISTICS

5.1. Absolute Maximum Rating

Exceeding the values reported below at any time may lead to a performance deterioration, malfunction or destruction of the chip.

The values reported below are guaranteed by characterization results, not tested in production.

Table 27. VOLTAGE CHARACTERISTICS

Symbol	Parameter	MIN.	MAX.	Unit
V_{DD}-V_{SS}	DC Power Supply	-0.3	4	V
$\lvert V_{DDX}-V_{DD}\rvert$	Variation between different power pins		50	mV
V_{IN}	Input Voltage on any other pin		V_{DD}	V
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF + 47uF on V_{DD} and V_{SS} pins to induce a functional disturbance To be applied through 2.2uF on LDO_CAP and V_{SS} Condition: V_{DD} = 3.3V, T_A = 25°C		4.4	kV

Table 28. CURRENT CHARACTERISTICS [1)]

Symbol	Parameter	MIN.	MAX.	Unit
I_{DD}	Maximum Current into V_{DD}		200	mA
I_{SS}	Maximum Current out of V_{SS}		100	
I_{IO}	Maximum Current Sunk by a I/O pin		20	
	Maximum Current Sourced by a I/O pin		20	
	Maximum Current Sunk by total I/O pins		100	
	Maximum Current Sourced by total I/O pins		100	
LU	Static latch-up class (at T_A = 25°C)		400	mA

[1)] All interface-related pins are referred to as IO pins.

Table 29. THERMAL CHARACTERISTICS

Symbol	Parameter	MIN.	MAX.	Unit
T_A	Operating Temperature	-40	105	°C
T_J	Junction Temperature	-40	125	
T_{ST}	Storage Temperature	-65	150	

5.2. Nominal Operating Conditions

The values below assume V_{DD} – V_{SS} is in the range of 3.0 to 3.6 V, and T_A = 25°C, unless otherwise specified.

Table 30. VOLTAGE CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
V_{LDO}	LDO output voltage	C_{LDO} of 2.2 µF	1.08	1.2	1.32	
T_{VDD}	V_{DD} rise time rate		10			µs/V
	V_{DD} fall time rate		10			

Table 31. CURRENT CONSUMPTION [1)]

Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I_{DD}	Capture mode		60		mA
	Reduced clock speed		38		
	Sleep mode		4		

[1)] Measured at V_{DD} = 3.3 V and T_A = 25 °C.

6. DYNAMIC TIMING CHARACTERISTICS

6.1. MI48xx Clock

The MI48Dx timing is driven by a 12 MHz external oscillator. Internally, it generates all necessary timing for its operation and interfaces.

6.2. MI48xx Reset

The MI48xx is reset by asserting 0 to the nRESET pin 16 of the QFN33 package.

The nRESET pin must be held low (below 0.2 V_{DD}) for at least 32 µs in order to take effect. Similarly, nRESET is considered released after the pin is held high (above 0.7 V_{DD}) for at least 32 µs.

6.2.1. Normal power up

The time between de-asserting the nRESET pin and attempting to acquire the first image from the connected camera module is 1.5 seconds. For a more precise timing budget, one could poll bit 5 of STATUS register at 0xB6, i.e. check the value of bit 5 of 0xB6 – if it is set to 1, capture is still in progress and data is NOT available; if it is 0, then temperature is available and can be readout.

6.2.2. First time power-up

When MI48xx detects that a new camera module has been attached, the power up sequence will take 3 seconds before the first image can be acquired.

6.3. I²C Characteristics

Table 32. I²C TIMING PARAMETERS

Symbol	Parameter	MIN.	MAX.	Unit
t_{LOW}	I²C_SCL LOW period	4.7	-	µs
t_{HIGH}	I²C_SCL HIGH period	4	-	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	µs
$t_{HD;STA}$	START condition hold time	4	-	µs
$t_{SU;STO}$	STOP condition setup time	4	-	µs
t_{BUF}	Bus free time	4.7	-	µs
$t_{SU;DAT}$	Data setup time	250	-	ns
$t_{HD;DAT}$	Data hold time	0	3.45	µs
t_r	I²C_SCL/SDA rise time	-	1000	ns
t_f	I²C_SCL/SDA fall time	-	300	ns
C_b	Capacitive load for each bus line	-	400	pF

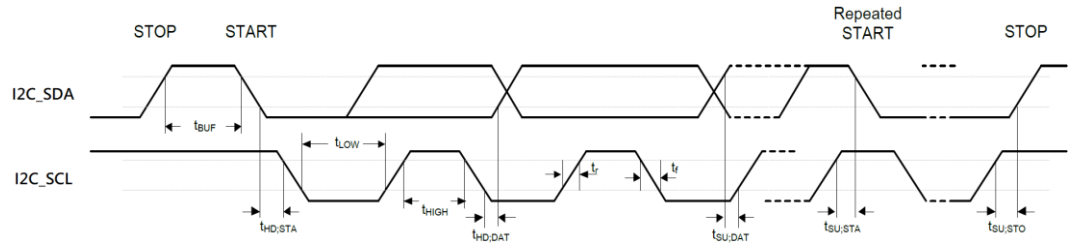


Fig. 8. Timing diagram of the I²C bus.

6.4. SPI Interface

Table 33. SPI TIMING PARAMETERS

Symbol	Parameter	MIN.	MAX.	UNIT
VDD=3.3V, 30pF Loading Capacitor				
f_{CLK}	Clock frequency	-	100	MHz
t_{CLKH}	Clock high time	-	T_{SPI_CLK} / 2	ns
t_{CLKL}	Clock low time	-	T_{SPI_CLK} / 2	
t_{SS}	Slave setup time	T_{SPI_CLK} + 2ns	-	
t_{SH}	Slave hold time	T_{SPI_CLK}	-	
t_{DS}	Data input setup time	0	-	
t_{DH}	Data input hold time	2	-	
t_V	Data output valid time	-	8	

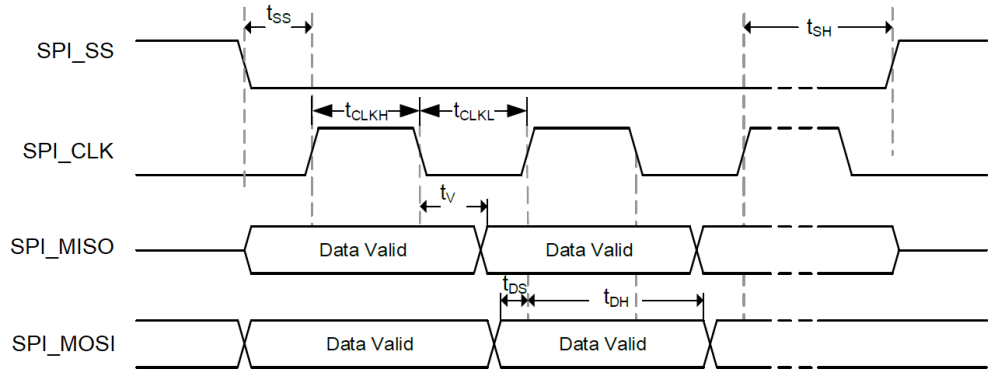
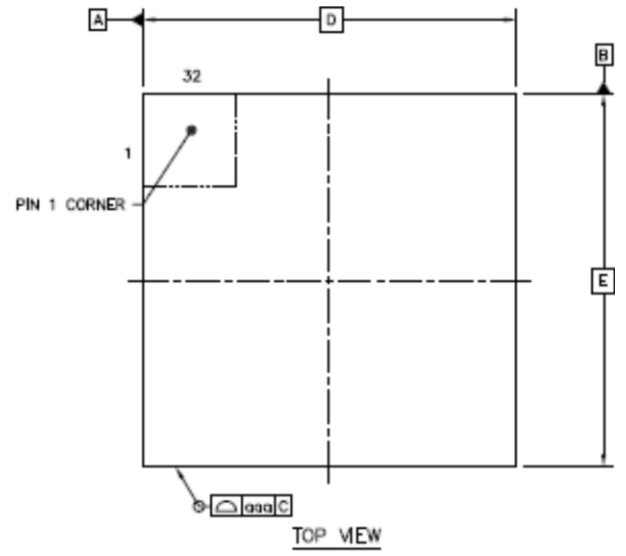


Fig. 9. SPI Interface timing diagram.

7. PACKAGE INFORMATION

7.1. Chip packaging



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Fig. 10. Dimension of the QFN33 package (5x5x0.8 mm^3, Pitch 0.5mm). All values are in [mm].

7.2. Shipping box

Chip Quantity per JEDEC tray	JEDEC trays per box	Chip quantity per box	Box dimensions L x W x H, mm	Gross weight, kg
490	8	3920	36.5 x 17.5 x 8	2.25

The above table reflects mass production quantities. For small quantities, the shipping box is decided on a per case basis.

8. REFERENCE DESIGN

8.1. Reference Circuit

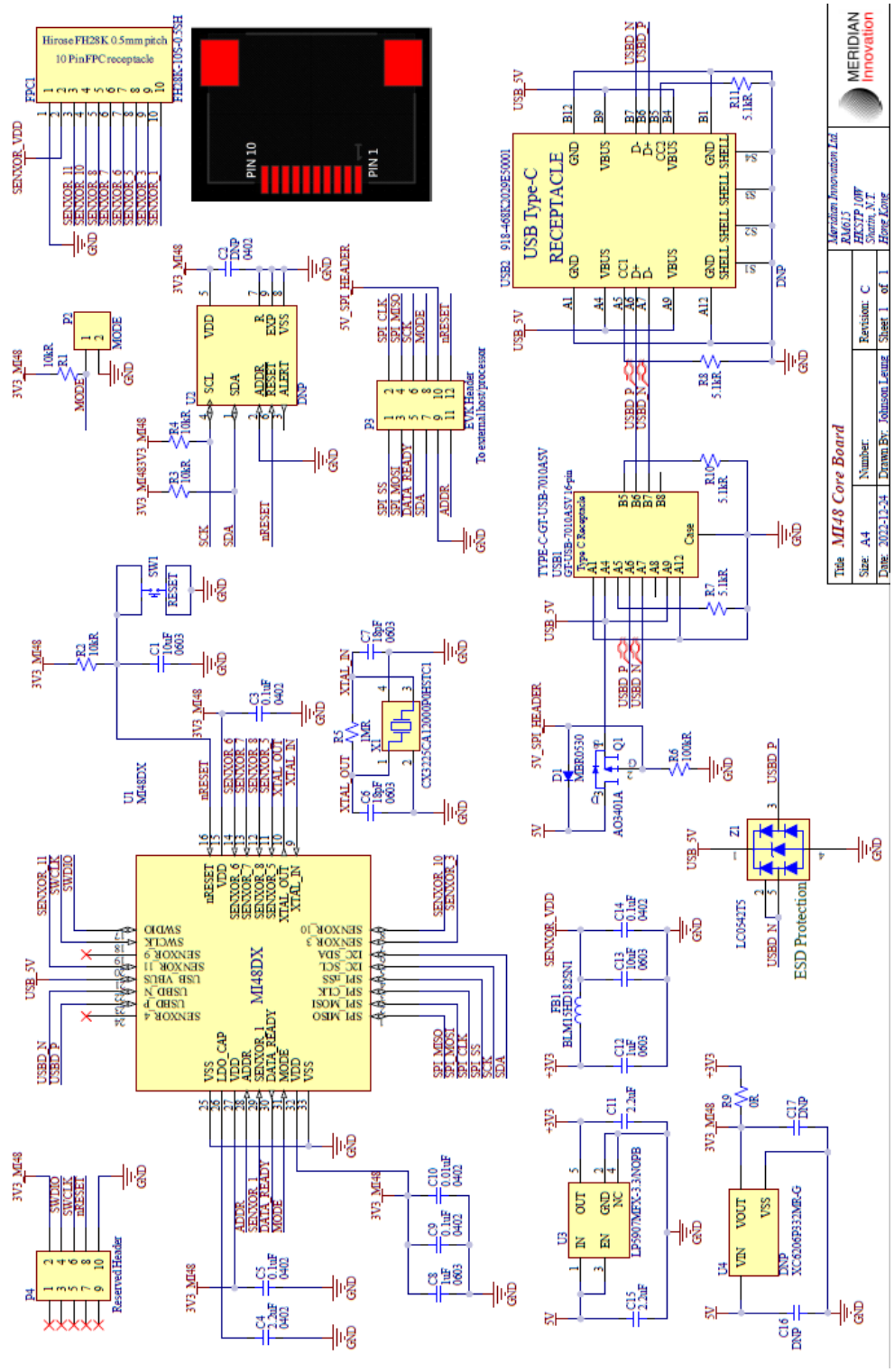


Fig. 11. Reference design circuit used for the MI0802Mxx module evaluation board.

Note that the reference circuit includes both options for communication to the host MCU, and the header P2 is used to define which mode – USB or SPI/I2C, is being select. In an end-user application only one of these interfaces will be needed.

It is suggested that the USB_N and USB_P pins are fanned out to a header or test pads, and that USB 5V (USB Vbus) and GND are connected to the MI48Dx USB_VBUS (pin 21) and GND correspondingly, even if the end system uses SPI/I^2C communication interface to the host MCU. This is to enable potential firmware updates to the MI48Dx via the USB interface. Such an update can be realised with the help of Meridian Innovation DFU (Device Firmware Update) software, which can be run on a Windows PC or an Android device with USB connection to the system hosting the MI48Dx. Note that the system must be able to boot up independently and be able to operate correctly. Therefore, the system must provide the MI48Dx with a stable 3.3 V VDD and drive correctly the reset and clock signals.

8.2. Bill of Materials

Table 34. BILL OF MATERIALS (MI48DX REFERENCE CIRCUIT)

Designator	Value / Vendor Part Number	Description	Vendor	Quantity
C1, C13	10uF	Capacitor SMD, XCAM-C0603, 20%, 6.3V, X5R		2
C3, C5, C9, C14	0.1uF	Capacitor SMD, XCAM-C0402, 10%, 6.3V, X5R		4
C4	2.2uF	Capacitor SMD, XCAM-C0402, 10%, 6.3V, X5R		1
C6, C7	18pF	Capacitor SMD, XCAM-C0603, 1%, 50V, C0G		2
C8, C12	1uF	Capacitor SMD, XCAM-C0603, 20%, 6.3V, X5R		2
C10	0.01uF	Capacitor SMD, XCAM-C0402, 10%, 6.3V, X5R		1
C11, C15	2.2uF	Capacitor SMD, XCAM-C0603, 20%, 10V, X5R		2
D1	MBR0530	Surface Mount Schottky Power Rectifier, SOD123	OnSemi	1
FB1	BLM15HD182SN1	Inductor SMD, XCAM-R0402	Murata	1
FPC1	FH28K-10S-0.5SH	Hirose 0.5 mm Pitch, FPC Receptacle, 10P	Hirose	1
Q1	AO3401A	30V 4.0A P-Channel MOSFET, SOT23	Alpha & Omega Semicon.	1
R1, R2, R3, R4	10kR	Resistor SMD, XCAM-R0402, 5%		4
R5	1MR	Resistor SMD, XCAM-R0402, 5%		1
R6	100kR	Resistor SMD, XCAM-R0402, 5%		1
R7, R8, R10, R11	5.1kR	Resistor SMD, XCAM-R0402, 5%		4
R9	0R	Resistor SMD, R0805		1
SW1	SKRPABE010	4-pin Tactile Switch, SKRP Series, TACT-SW-4P	Alps Alpine	1
U1	MI48DX	Thermal Image Processor for MI0802Mxx Thermal Imaging Modules, QFN33	Meridian Innovation	1

U3	LP5907MFX-3.3/NOPB	LP5907 250-mA, Ultra-Low-Noise LDO, SOT23-5 Package, LP5907 SOT-23	Texas Instruments	1
USB1	TYPE-C-GT-USB-7010ASV	5A 1 Surface Mount 16 Female -45℃~+85℃ Type-C SMD USB Connectors ROHS, GT-USB-7010ASV		1
X1	CX3225CA12000P0HSTC1	Passive 4-pin Oscillator, XTAL-4P, CX3225CA	KYOCERA	1
Z1	LC0542T5	Leiditech TVS Diode, TPD2E001DRLR, SOT553-TI	LEIDITECH	1

9. PCB Design Considerations

The recommended PCB layout of the solder pads for the MI48xx is shown in Fig. 14. Additionally, the standard design rules should be considered to minimize noise and interference:

- Trace length, including FPC cable length to the camera module should not exceed 30 cm.
- Power related traces to the camera module (e.g. from LDO) should be as short as possible and as wide as possible to avoid any drop in V_{DD} to which temperature accuracy is sensitive.
- Avoid ground loops, i.e. ground traces should form star connections only

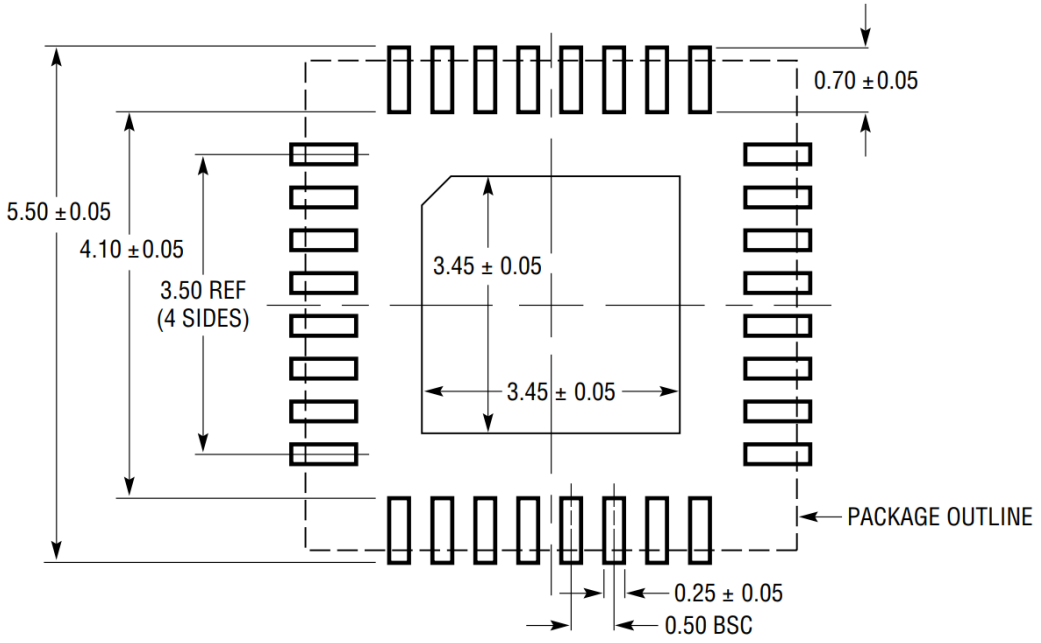


Fig. 12. Recommended PCB design pattern. All values are in [mm].

10. Revision History

Revision	*Date*	*Comment*
Draft	22/3/2019	Draft

0.B	9/4/2019	Formatting and changes for consistency (PSP) – no rev A
0.C	18/06/2019	Updating part number to MI48A0 Updating Pin configuration, reference circuit. Adding FPC layout reference.
1.0	5 Aug 2019	Merged a revised version of MI48A0 Interface Protocol (v0.D) Styling Overhaul Figures and tables update Major revision and expansion of text from original and merged document, numerical and unit's data.
1.0.1	11 Aug 2019	Updated as per FW 1.5.8 beta
1.0.2	3 Sept 2019	Updated with DISTANCE_CORR register and corrections of some inaccuracies in text.
1.0.3	8 Sept 2019	Minor iteration and errata: Inductor value in Reference Circuit, I^2C ADDR pin, SPI description, Package Info.
1.0.4	11 Sept 2019	Critical errata to SPI interface description (MSB mode of transfer). Errata to pinout (ADDR type). Minor clarifications, syntax and typing.
1.0.5	15 Sept 2019	Minor styling adjustments.
1.0.6	23 Sept 2019	Corrections to MODE_REGISTER, reset value of POWER_MODE_2, and Section 4.7. Added Reset info.
1.0.7.	30 Sept 2019	Chip marking in diagrams corrected.
1.0.8.	20 Oct 2019	Legal notice added; Tagged Confidential: Under NDA; Elaborated bit START_CAPTRE behaviour when re-written while in capture; Corrected FRAME_MODE reset value; Eliminated Distance Correction Register. Clarified the CRC-16/CCITT-FALSE implementation.
2.0.0	30 Jan 2020	Updates reflecting Filtering; Fixed address of DistanceCorrection register (0xC2). DATA_READY bit in STATUS register
2.0.1	10 Feb 2020	Added BOOTUP bit in Status Register. Added OFFSET_CORR register. Added description of Filtering in MI48.
2.0.2	28 Feb 2020	Updated reference circuit to include 12-pin header for connecting to host system (reflecting core development board); I2C bus pullups reduced to 4.7 kohm; revised table/figure references
2.0.3	6 Mar 2020	PCB design considerations added. Info on MI48Bx Added.
2.0.4	15 Mar 2020	Added programming pins/header to MI48A reference circuit
3.1.1	23 June 2022	Updated Register Map and section for User Flash, Median Filter, Power-related register naming, Filtering description.
3.1.2	27 June 2022	Updated Appendix and Reference Circuit diagrams
3.1.3	28 June 2022	Updated Product code with explicit reference/mapping to FW version, shipping box details, Appendix.
4.0.0	23 Dec 2022	Update for Cougar, including: Module type register, Self-calibration, Module gain control Access to module flash access
4.0.2	26 Dec 2022	Updated pinout information and reference design, BOM

4.0.3	28 Dec 2022	Updated register map. Added subsections on gain control and self-calibration. Updated comments regarding reference circuit and DFU update.
4.0.4	28 Dec 2022	Appendix I added to define correspondence between Module Type (Reg 0xBB) and Product Code
4.0.5	22 Feb 2022	Updated bootup timing and 50 ms delay upon wake up from sleep mode.

11. LEGAL INFORMATION

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13. APPENDIX I

Table 35. MODULE TYPE CODE AND PRODUCT CODE CORRESPONDENCE

Module Type	Product Code	Resolution	FOV (H/V/D)	Comment
19	MI0802M5S	80 x 62	45/35/56	
20	MI0802M6S	80 x 62	90/67/122	
21	MI0802M7G	80 x 62	105/79/134	