ES8389

High Performance Stereo Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM master or slave serial data port
- 256/384Fs and USB 12/24 MHz audio system clocks
- I^2C interface

Stereo ADC

- 24-bit, 8 to 192 kHz sampling frequency
- 103 dB signal to noise ratio, -90 dB THD+N
- Two pair of analog input with differential input option
- Low noise pre-amplifier
- Auto level control (ALC)
- Support analog and digital microphone

Stereo DAC

- 24-bit, 8 to 192 kHz sampling frequency
- 110 dB signal to noise ratio, -85 dB THD+N
- Two pair of analog output with headphone driver and differential output option
- Line in to line out mixing
- Pop and click noise suppression

Low Power

- 1.8V to 3.3V operation
- mW playback and record
- Low standby current

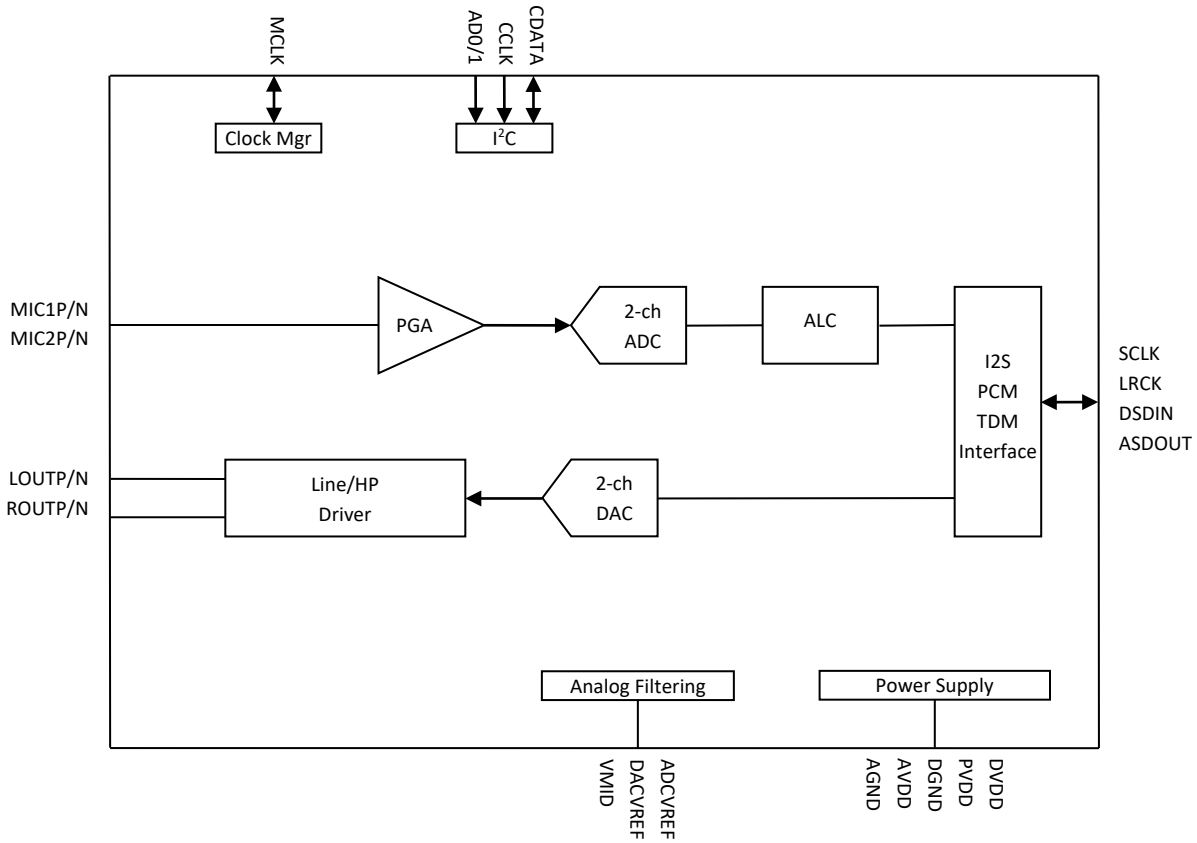
APPLICATIONS

- Automotive
- Surveillance
- General Purpose

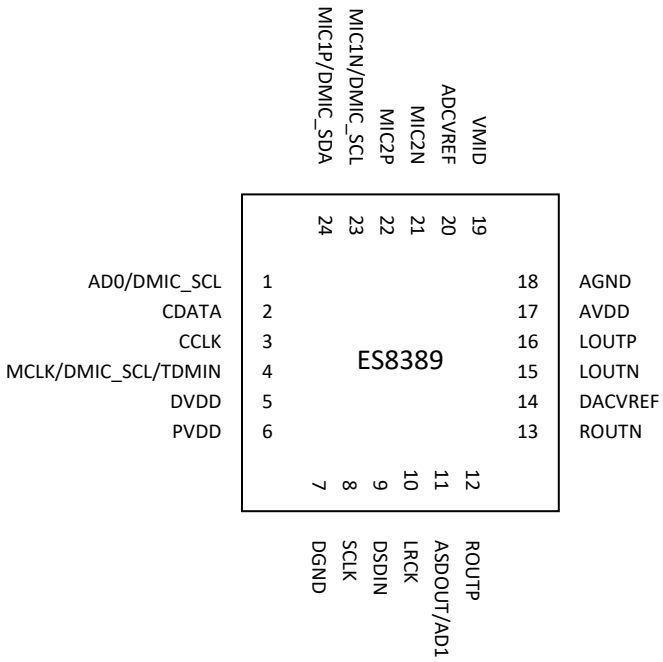
ORDERING INFORMATION

ES8389 -40°C ~ +125°C
3x3 QFN-24

1. BLOCK DIAGRAM

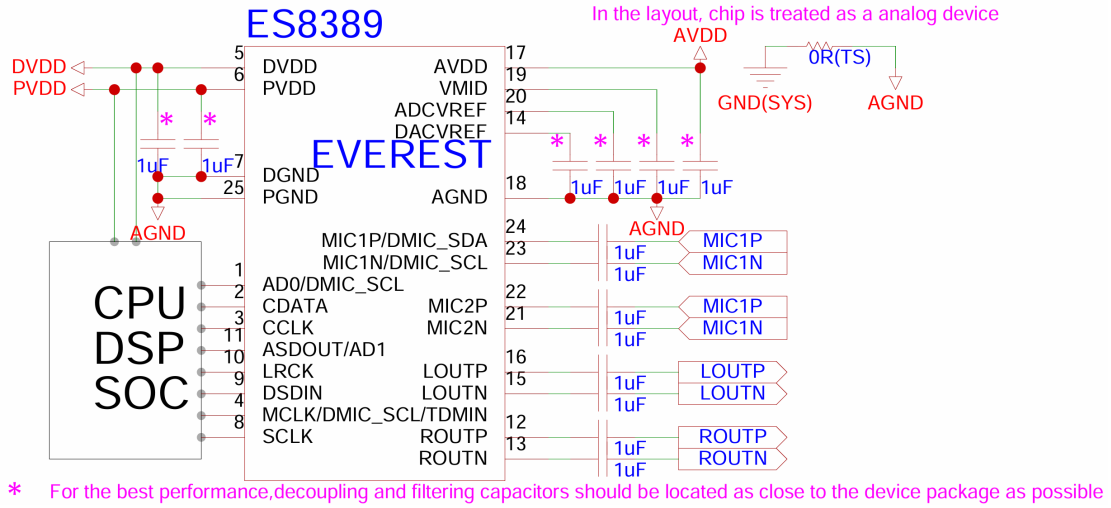


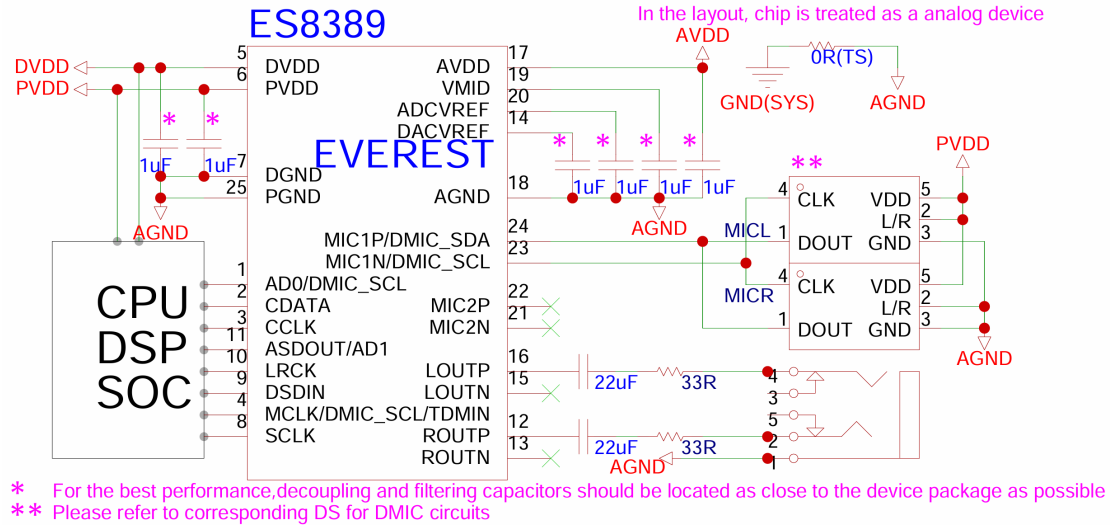
2. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA, AD0/DMIC_SCL	3, 2, 1	I, I/O, I/O	I^2C clock, data, address/DMIC clock
MCLK/DMIC_SCL/TDMIN	4	I/O	Master clock/DMIC clock/TDM in
SCLK	8	I/O	Serial data bit clock
LRCK	10	I/O	Serial data left and right channel frame clock
ASDOUT/AD1	11	O/I	ADC serial data output/I^2C address
DSDIN	9	I	DAC serial data input
MIC1P/N MIC2P/N	24, 23 22, 21	I/O	Mic or line input MIC1P/N can be used as DMIC data and clock
LOUTP/N ROUTP/N	16, 15 12, 13	O	Differential analog output
PVDD	6	Analog	Power supply for the digital input and output
DVDD, DGND	5, 7	Analog	Digital power supply
AVDD, AGND	17, 18	Analog	Analog power supply
VMID	19	Analog	Filtering capacitor connection
ADCVREF, DACVREF	20, 14	Analog	Filtering capacitor connection
PGND	25	Analog	Package bottom plate ground

3. TYPICAL APPLICATION CIRCUIT





4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (32Fs, 64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc.) and USB clocks (12/24 MHz).

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 00100x, where x equals AD1 AD0 (input pin: 1 being connected to supply and 0 being connected to ground). The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0010 0 AD1 AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

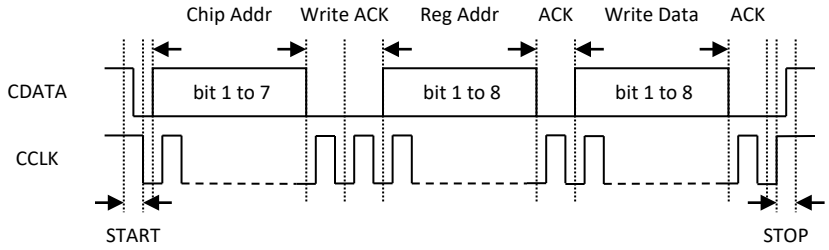


Figure 1a I²C Write Timing

Table 2 Read Data from Register in I²C Interface Mode

	Chip Address	R/W		Register Address		
Start	0010 0 AD1 AD0	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0010 0 AD1 AD0	1	ACK	Data	NACK	Stop

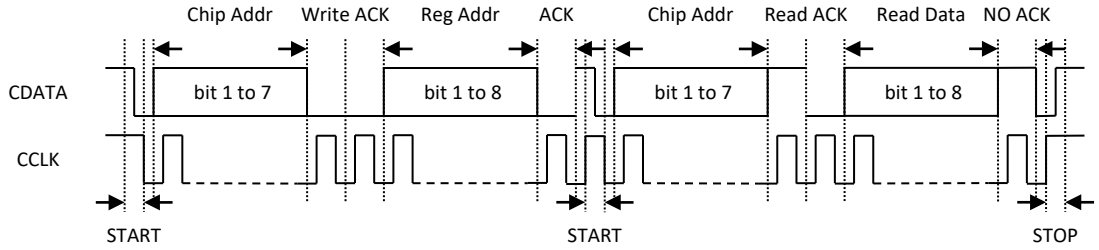


Figure 1b I²C Read Timing

Registers 0xF2, 0xF3 (bit 0, 2, 4 and 7), 0xFD and 0xFE use PVDD power supply, and the rest of registers use DVDD power supply. The registers in DVDD power supply can be accessed after writing 0x00 to register 0xF3.

6. I²S/PCM/TDM INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and SDIN or SDOUT pins. These formats are I²S, left justified, DSP/PCM and TDM. DAC input SDIN is sampled by the device on the rising edge of SCLK. ADC data is out at SDOUT on the falling edge of SCLK. The relationship of SDATA (SDIN/SDOUT), SCLK and LRCK with these formats are shown through Figure 2a to Figure 2h. Multiple ADC can be cascaded through TDMIN pin or on ADSOUT pin.

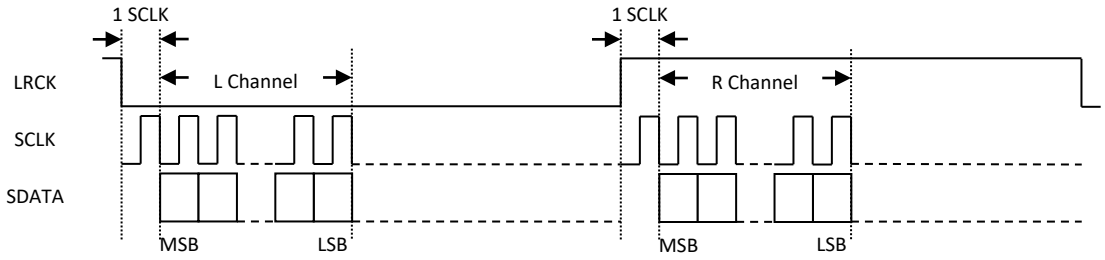


Figure 2a I²S Serial Audio Data Format

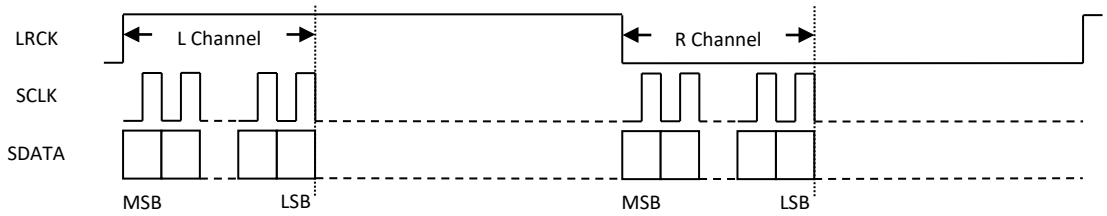


Figure 2b Left Justified Serial Audio Data Format

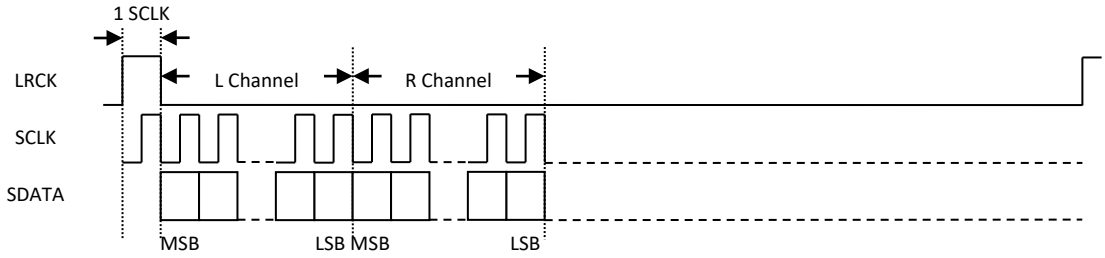


Figure 2c DSP/PCM Mode A Serial Audio Data Format

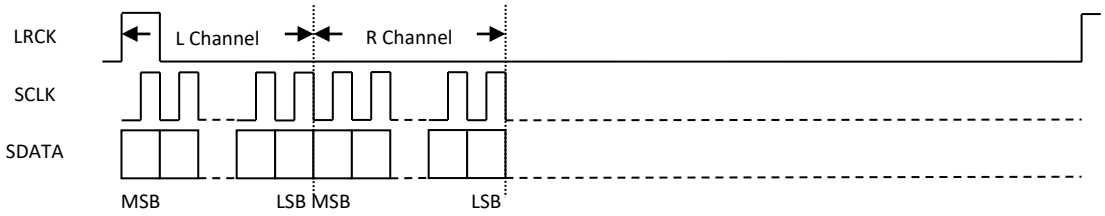


Figure 2d DSP/PCM Mode B Serial Audio Data Format

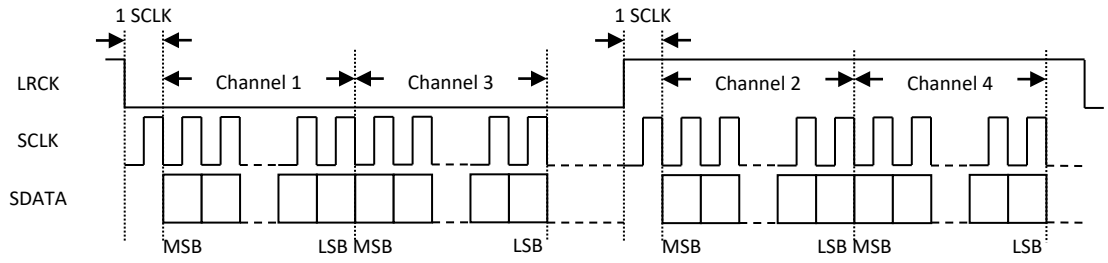


Figure 2e TDM I^{2}S Serial Audio Data Format

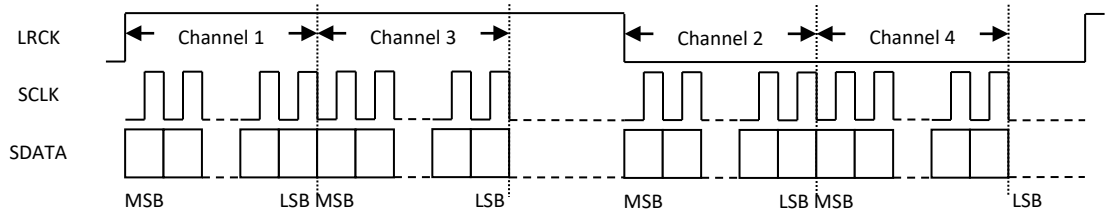


Figure 2f TDM Left Justified Serial Audio Data Format

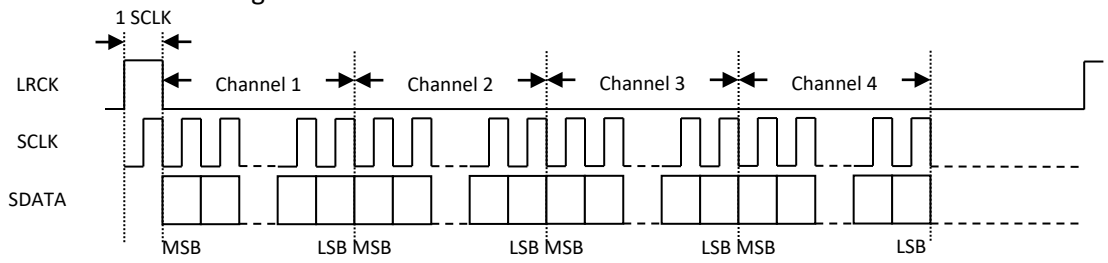


Figure 2g TDM DSP/PCM Mode A Serial Audio Data Format

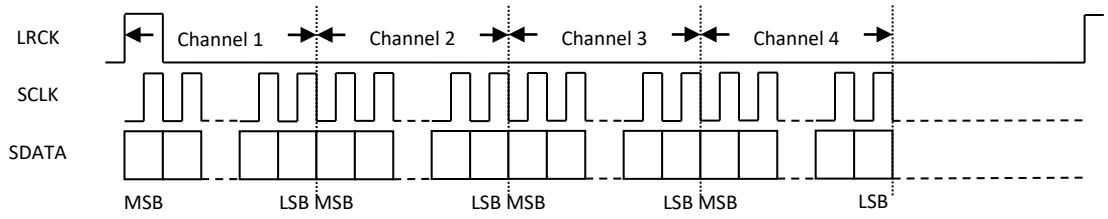


Figure 2h TDM DSP/PCM Mode B Serial Audio Data Format

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+125°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
DVDD (Note 1)	1.6	1.8/3.3	3.6	V
PVDD	1.6	1.8/3.3	3.6	V
AVDD	3.0	3.3	3.6	V

Note 1: for 192 kHz, DVDD must be 3.3V.

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	99	103	105	dB
THD+N	-93	-90	-87	dB
Channel Separation (1KHz)		114		dB
Interchannel Gain Mismatch		0.1	0.5	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input (differential P and N)		2.2*AVDD/3.3		Vrms
Input Impedance		16		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	105	110	112	dB
THD+N	-88	-85	-82	dB
Channel Separation (1KHz)		119		dB
Interchannel Gain Mismatch		0.1	0.5	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Analog Output				
Full Scale Output (differential P and N)		1.85*AVDD/3.3		Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V		60		mW
Power Down Mode (Note 2)				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V			0.1	uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

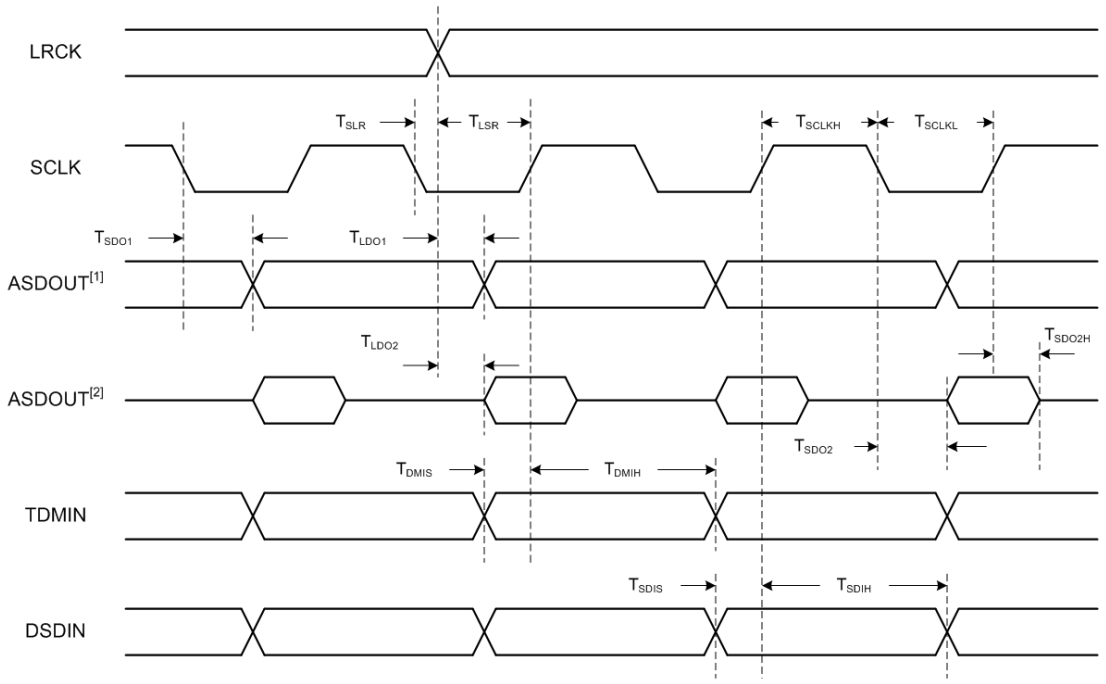
Note 2: recommend all power supply on, entering low power through control register setting, then stopping input clock.

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER		Symbol	MIN	MAX	UNIT
MCLK frequency				49.2	MHz
MCLK duty cycle			40	60	%
LRCK frequency				192	KHz
LRCK duty cycle (Note 3)			40	60	%
SCLK frequency	VDDD=1.8V VDDD=3.3V			13 26	MHz
SCLK pulse width low		T_{SCLKL}	16		ns
SCLK Pulse width high		T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)		T_{SLR}		5	ns
LRCK edge to SCLK rising (slave mode only)		T_{LSR}	10		ns
SCLK falling to ASDOUT valid	VDDD=1.8V VDDD=3.3V	T_{SDO1}		31.5 12	ns
LRCK edge to ASDOUT valid (Note 4)	VDDD=1.8V VDDD=3.3V	T_{LDO1}		26 10	ns
SCLK falling to ASDOUT valid (PTDM mode)	VDDD=1.8V VDDD=3.3V	T_{SDO2}		33 16	ns
LRCK edge to ASDOUT valid (PTDM mode)	VDDD=1.8V VDDD=3.3V	T_{LDO2}		26 10	ns
TDMIN valid to SCLK rising setup time		T_{DMIS}	10		ns
SCLK rising to TDMIN hold time		T_{DMIH}	10		ns
DSDIN valid to SCLK rising setup time		T_{SDIS}	10		ns
SCLK rising to DSDIN setup time		T_{SDIH}	10		ns

Note 3: one SCLK period of high time in DSP/PCM modes.

Note 4: only apply to MSB of Left Justified or DSP/PCM mode B.



Note: T_{SDO2H} equal to T_{SDO2} (PTDM mode)

Figure 3 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

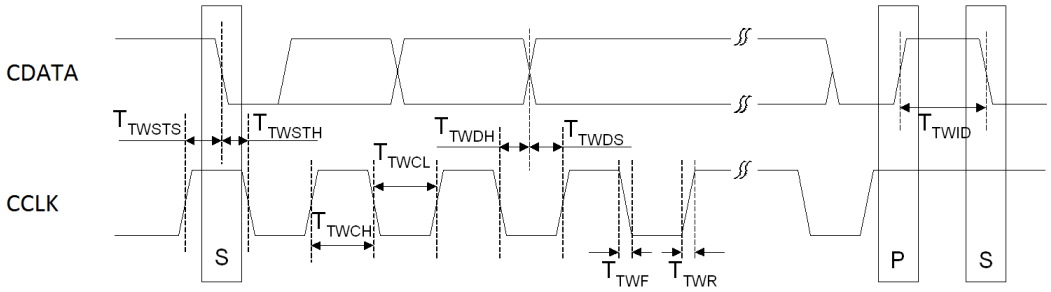


Figure 4 I²C Timing

8. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 – RESET CONTROL, DEFAULT 11111110

Bit Name	Bit	Description
RST_REGS	7	0 – normal 1 – reset control registers (except this bit)
RST_DIG	6	0 – normal 1 – reset digital (except control registers)
RST_XCLKGEN	5	0 – normal 1 – reset clock generate logic
RST_ADCCLK_GEN	4	0 – normal 1 – reset clock generate logic for adc
RST_DACCLK_GEN	3	0 – normal 1 – reset clock generate logic for dac
RST_ADC_DIG	2	0 – normal 1 – reset ADC function logic
RST_DAC_DIG	1	0 – normal 1 – reset DAC function logic
CSM_ON	0	Chip state machine stay power down 0–enable 1–disable

REGISTER 0X01 – MISC CONTROL, DEFAULT 11100000

Bit Name	Bit	Description
TRI_BCLK	7	0 – normal 1 – SCLK tri state
TRI_LRCK	6	0 – normal 1 – LRCK tri state
TRI_ADCDAT	5	0 – normal 1 – ASDOUT tri state
RST_MSTGEN	4	0 – normal 1 – reset master mode LRCK and SCLK
MST_CLK_ON	3	0 – turn off master mode SCLK and LRCK 1 – turn on master mode SCLK and LRCK
Reserved	2	Reserved
SEQ_DIS	1	Auto power sequence 0 – enable 1 – disable
MS_MODE	0	LRCK/SCLK clock mode 0 – slave mode 1 – master mode

REGISTER 0X02 – MASTER CLOCK CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
MAINCLK_SRCSEKL	7:6	Clock select for csm clock and the clock of filter logic module 00 – MCLK, MCLK 01 – SCLK, SCLK 10 – OSC output clock, MCLK 11 – OSC output clock, BCLK

MSTCLK_SRCSEL	5	0 – MCLK from pad 1 – MCLK from clock generator
DAC_DEMANA_CLKSEL	4	0 – from MSTCLK 1 – from OSC
DMICCLK_PADSEL	3:2	00 – select MIC1N as DMIC output clock 01 – select MCLK as DMIC output clock 10 – select AD0 as DMIC output clock 11 – select AD0 as DMIC output clock
MAINCLK_INVERT	1	0 – normal 1 – invert main clock
BCLK_INVERT	0	0 – normal 1 – invert SCLK clock

REGISTER 0X03 – CLOCK OFF 1, DEFAULT 00000000

Bit Name	Bit	Description
ADC_CLK_ON	7	0 – turn off ADC master clock 1 – turn on ADC master clock
DAC_CLK_ON	6	0 – turn off DAC master clock 1 – turn on DAC master clock
Reserved	5:2	Reserved
EXT_BCLKLRCK_ON	1	0 – turn off slave mode SCLK and LRCK internally 1 – turn on slave mode SCLK and LRCK internally
EXT_MCLK_ON	0	0 – turn off master clock 1 – turn on master clock

REGISTER 0X04 – MAIN CLOCK DIVIDER 1, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7	Reserved
XCLKGEN_DIV	6:0	MCLK divide 0 – no divide 1 – divide by 2 2 – divide by 3 .... 127 – divide by 128

REGISTER 0X05 – MASTER CLOCK MULTIPLICATION, DEFAULT 00000000

Bit Name	Bit	Description
ANACLK_DLYSEL	7:6	ADC analog clock delay index 00 – delay 1 01 – delay 2 10 – delay 3 11 – delay 4
DBL1_MODE	5	clock multiply 0 –multiply by 1 1 –multiply by 2
DBL2_MODE	4	clock multiply 0 – multiply by 1 1 – multiply by 2
MX1_MODE	3:2	clock multiply 00 – multiply by 1

		01 – multiply by 4 10 – multiply by 6 11 – multiply by 8
MX2_MODE	1:0	clock multiply 00 – multiply by 1 01 – multiply by 4 10 – multiply by 6 11 – multiply by 8

REGISTER 0X06 – MAIN CLOCK MUX 1, DEFAULT 00000000

Bit Name	Bit	Description
XCLKGEN_OUT1A_MUXSEL	7	0 – select path 1 1 – select path 2
XCLKGEN_OUT1D_MUXSEL	6:5	00 – select path 1 01 – select path 2 10 – select path 3 11 – select path 4
Reserved	4	Reserved
XCLKGEN_OUT3_MUXSEL	3:2	00 – select path 1 01 – select path 2 10 – select path 3 11 – select path 4
XCLKGEN_OUT2_MUXSEL	1:0	00 – select path 1 01 – select path 2 10 – select path 3 11 – select path 4

REGISTER 0X07 – MAIN CLOCK MUX 2, DEFAULT 00000000

Bit Name	Bit	Description
ADC_OUT2DIV_SYNC_ON	7	0 – sync off 1 – sync on
ADC_OUT3DIV_SYNC_ON	6	0 – sync off 1 – sync on
ADC_DSP_MUXSEL	5	0 – select path 1 1 – select path 2
ADC_ANA_MUXSEL	4	0 – select path 1 1 – select path 2
ADC_CF_MUXSEL	3	0 – select path 1 1 – select path 2
ADC_OUT2_CLKDIV	2:0	clock divide 000 – divide by 1 001 – divide by 2 .... 111 – divide by 8

REGISTER 0X08 – ADC CLOCK CONTROL, DEFAULT 01000000

Bit Name	Bit	Description
ADC_DELAY_SEL	7:6	ADC clock delay 00 – no delay 01 – delay 1 10 – delay 2

		11 – delay 3
Reserved	5	Reserved
ADC_DMIC_HALFCLK	4	0 – normal 1 – half dmic clock frequency
ADC_CF_HALFCLK	3	0 – normal 1 – half comb clock frequency
ADC_OUT3_CLKDIV	2:0	clock divide 000 – divide by 1 001 – divide by 2 .... 111 – divide by 8

REGISTER 0X09 – DAC CLOCK CONTROL 1, DEFAULT 00000000

Bit Name	Bit	Description
DAC_DSMDIV_SYNC_ON	7	0 – sync off 1 – sync on
DAC_DSPDIV_SYNC_ON	6	0 – sync off 1 – sync on
ADC_DSP_MUXSEL	5	0 – select path 1 1 – select path 2
ADC_ANA_MUXSEL	4	0 – select path 1 1 – select path 2
STOPCLK_SRCSEL	3	0 – select MCLK/SCLK 1 – select internal generate clock
Reserved	2	Reserved
DAC_DSM_MUXSEL	1:0	00 – select path 1 01 – select path 2 10 – select path 3 11 – select path 4

REGISTER 0X0A – DAC CLOCK CONCTROL 2, DEFAULT 00000000

Bit Name	Bit	Description
DAC_CLKOFF_AUTOSW_EN	7	0 – not auto-switch 1 – DAC's analog clock auto-switch to OSC clock
DAC_DSP_CLKDIV	6:4	clock divide 000 – divide by 1 001 – divide by 2 .... 111 – divide by 8
Reserved	3	Reserved
DAC_DSM_CLKDIV	2:0	clock divide 000 – divide by 1 001 – divide by 2 .... 111 – divide by 8

REGISTER 0X0B – MASTER SCLK DIVIDER, DEFAULT 00000100

Bit Name	Bit	Description
Reserved	7	Reserved
MST_BCLK_DIV	6:0	SCLK divide (use with MSTCLK_SRCSEL)

		0/1 – no divide 2 – divide by 2 .... 127 – divide by 127

REGISTER 0X0C – MASTER LRCK DIVIDER 1, DEFAULT 00000001

Bit Name	Bit	Description
MST_SP_PTL	7:6	00 – I^2S 01 – Left Justified 10 – DSP mode 11 – DSP mode
MST_SP_LRP	5	I^2S/Left Justified: 0 – L/R normal polarity Left/Right=High/Low (Left Justified) Left/Right=Low/High (I^2S) 1 – L/R invert polarity Left/Right=Low/High (Left Justified) Left/Right=High/Low (I^2S) DSP/PCM mode: 0 – mode A 1 – mode B
Reserved	4	Reserved
MST_LRCK_DIVH	3:0	MST_LRCK_DIV[11:8]

REGISTER 0X0D – MASTER LRCK DIVIDER 2, DEFAULT 00000000

Bit Name	Bit	Description
MST_LRCK_DIVL	7:0	MST_LRCK_DIV[7:0]

REGISTER 0X0E – CLOCK OFF 2, DEFAULT 00000000

Bit Name	Bit	Description
ADC1_DEMCLK_OFF	7	0 – normal 1 – ADC1's dem clock off
ADC2_DEMCLK_OFF	6	0 – normal 1 – ADC2's dem clock off
ADC1_CFINTCLK_OFF	5	0 – normal 1 – ADC1's comb integrator clock off
ADC2_CFINTCLK_OFF	4	0 – normal 1 – ADC2' s comb integrator clock off
DAC1_DEMCLK_OFF	3	0 – normal 1 – DAC1's dem clock off
DAC2_DEMCLK_OFF	2	0 – normal 1 – DAC2's dem clock off
ADC_ANACLK_OFFLVL	1	fix ADC's analog clock level 0 – low level 1 – high level
DAC_ANACLK_OFFLVL	0	fix DAC's analog clock level 0 – low level 1 – high level

REGISTER 0X0F – OSC CLOCK CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
DETCLK_DIVSEL	7:6	input clock divide for clock detect 00 – divide by 1 01 – divide by 2 10 – divide by 4 11 – divide by 8
OSC_CLKDIV	5:3	OSC clock divide 000 – divide by 1 001 – divide by 2 .... 111 – divide by 8
OSC_CNT_BITSEL	2:0	clock number select for MCLK stop 000 – 256 divide clock 001 – 128 divide clock .... 111 – 2 divide clock

REGISTER 0X10 – CSM JUMP CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
OSCLK_SOFT_ON	7	0 – close internal OSC 1 – open internal OSC
LRCK_DET_ON	6	0 – close LRCK detect 1 – open LRCK detect
STDBY2NRML	5	0 – normal 1 – enable jump from Standby to Normal
NRML2STDBY	4	0 – normal 1 – enable jump from Normal to Standby
STDBY2PWDN	3	0 – normal 1 – enable jump from Standby to Powerdown
MCLKOFF_AUTO_LPEN	2	0 – normal 1 – auto from Normal to Standby when MCLK stop
Reserved	1:0	Reserved

REGISTER 0X11 – MAIN CLOCK DIVIDER 2, DEFAULT 00000000

Bit Name	Bit	Description
MX1_LF	7	0 – high frequency mode 1 – low frequency mode
MX2_LF	6	0 – high frequency mode 1 – low frequency mode
Reserved	5:3	Reserved
XCLKGEN_OUT3_DIV	2:0	OUT3 clock divide 000 – divide by 1 001 – divide by 2 .... 111 – divide by 8

REGISTER 0X12 TO 0X1C – RESERVED

REGISTER 0X20 – ADC SP CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC_SP_WL	7:5	000 – 24-bit 001 – 20-bit 010 – 18-bit 011 – 16-bit 100 – 32-bit
ADC_SP_LRP	4	I^2S/Left Justified: 0 – L/R normal polarity Left/Right=High/Low (Left Justified) Left/Right=Low/High (I^2S) 1 – L/R invert polarity Left/Right=Low/High (Left Justified) Left/Right=High/Low (I^2S) DSP/PCM mode: 0 – mode A 1 – mode B
ADC_SP_PTL	3:2	00 – I^2S 01 – Left Justified 10 – DSP mode 11 – DSP mode
ADC1_P2S_SWMUTE	1	0 – normal 1 – mute ADC1 output to 0
ADC2_P2S_SWMUTE	0	0 – normal 1 – mute ADC2 output to 0

REGISTER 0X21 – ADC OSR CONTROL, DEFAULT 00011111

Bit Name	Bit	Description
ADC_FS_MODE	7	0 – Single speed mode 1 – Double speed mode
Reserved	6	Reserved
ADC_CF_OSR	5:0	ADC decimation ratio

REGISTER 0X22 – ADC DSP COUNTER CONTROL, DEFAULT 01111111

Bit Name	Bit	Description
ADC_DSP_OSR	7:0	ADC dsp counter parameter

REGISTER 0X23 – ADC MODE CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC_STDM_ON	7	0 – serial TDM off 1 – serial TDM on
ADC_PTDM_ON	6	0 – parallel TDM off 1 – parallel TDM on
ADC1_CF_SRCSEL	5	0 – normal 1 – ADC2 channel to ADC1 channel
ADC2_CF_SRCSEL	4	0 – normal 1 – ADC1 channel to ADC2 channel
Reserved	3	Reserved

ADC_DMIC_LRP	2	0 – ADC1 at posedge, ADC2 at negedge 1 – ADC2 at posedge, ADC1 at negedge
ADC_DMIC1_ON	1	0 – DMIC1 off 1 – DMIC1 on
ADC_DMIC2_ON	0	0 – DMIC2 off 1 – DMIC2 on

REGISTER 0X24 – ADC HPF CONTROL 1, DEFAULT 01100110

Bit Name	Bit	Description
ADC_SWE_VOL2E1	7	0 – normal 1 – ADC2's volume use ADC1's volume
ADC1_HPF_MODE	6	0 – HPF's offset close update 1 – HPF's offset always update
ADC2_HPF_MODE	5	0 – HPF's offset close update 1 – HPF's offset always update
ADC1_HPF_COEF1	4:0	HPF filter coefficient 1 5'b00110 – fast setting 5'b01101 – slow setting

REGISTER 0X25 – ADC HPF CONTROL 2, DEFAULT 00000110

Bit Name	Bit	Description
ADC_RAMCLR	7	0 – normal 1 – clear DSP ram
ADC1_180C	6	0 – normal 1 – output invert
ADC2_180C	5	0 – normal 1 – output invert
ADC1_HPF_COEF2	4:0	HPF filter coefficient 2 5'b00110 – fast setting 5'b01101 – slow setting

REGISTER 0X26 – ADC OSR VOLUME CONTROL, DEFAULT 10111111

Bit Name	Bit	Description
ADC_OSR_VOLUME	7:0	ADC OSR volume 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X27 – ADC1 VOLUME CONTROL, DEFAULT 10111111

Bit Name	Bit	Description
ADC1_SW_VOLUME	7:0	ADC1 software volume 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X28 – ADC2 VOLUME CONTROL, DEFAULT 10111111

Bit Name	Bit	Description
ADC2_SW_VOLUME	7:0	ADC2 software volume 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X29 – ALC CONTROL 1, DEFAULT 00000000

Bit Name	Bit	Description
ADC_VC_RAMPRATE	7:4	0 – VC: disable ramp ALC: 0.125dB/1LRCK 1 – 0.125dB/4LRCK 2 – 0.125dB/8LRCK ..... 15 – 0.125dB/2^(15+1)LRCK
ADC_ALC_WINSIZE	3:0	0 – 2LRCK 1 – 4LRCK 2 – 8LRCK ..... 15 – 2^(15+1)LRCK

REGISTER 0X2A – ADC PTDM CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC_ALC_CLKOFF	7	0 – normal 1 – ADC alc clock off
ADC_PTDM_SLOTSEL	6:4	0 – slot 0 1 – slot 1 ..... 7 – slot 7
Reserved	3:0	Reserved

REGISTER 0X2B – ALC CONTROL 2, DEFAULT 00000000

Bit Name	Bit	Description
ADC_ALC_ON	7:6	00 – disable ALC 01 – only ADC2 alc 10 – only ADC1 alc 11 – ADC1/ADC2 alc
ADC_ALC_MAXGAIN	5:0	Max gain dB = (ADC_ALC_MAXGAIN-31)dB

REGISTER 0X2C – ALC CONTROL 3, DEFAULT 11000000

Bit Name	Bit	Description
ADC_AM_WS	7:5	ADC automute window size 0 – 128 1 – 256 ..... 7 – 128x2^(ADC_AM_WS)
ADC_ALC_TARGET_LEVEL	4:0	ADC alc target level

0 – -32dB	8 – -19dB	16 – -11dB	24 – -4.5dB
1 – -30dB	9 – -18dB	17 – -10dB	25 – -4dB
2 – -28dB	10 – -17dB	18 – -9dB	26 – -3.5dB
3 – -26dB	11 – -16dB	19 – -8dB	27 – -3dB
4 – -24dB	12 – -15dB	20 – -7dB	28 – -2.5dB
5 – -22dB	13 – -14dB	21 – -6dB	29 – -2dB
6 – -21dB	14 – -13dB	22 – -5.5dB	30 – -1.5dB
7 – -20dB	15 – -12dB	23 – -5dB	31 – -1dB

REGISTER 0X2D – ALC CONTROL 4, DEFAULT 00000000

Bit Name	Bit	Description
ADC_AM_NG	7:5	ADC automute noise gate 0 – -96dB 1 – -90dB ..... 7 – -96+6x(7)dB
ADC_ALC_MAX_LEVEL	4:0	ADC alc max level

0 – -30dB	8 – -18dB	16 – -10dB	24 – -4dB
1 – -28dB	9 – -17dB	17 – -9dB	25 – -3.5dB
2 – -26dB	10 – -16dB	18 – -8dB	26 – -3dB
3 – -24dB	11 – -15dB	19 – -7dB	27 – -2.5dB
4 – -22dB	12 – -14dB	20 – -6dB	28 – -2dB
5 – -21dB	13 – -14dB	21 – -5.5dB	29 – -1.5dB
6 – -20dB	14 – -12dB	22 – -5dB	30 – -1dB
7 – -19dB	15 – -11dB	23 – -4.5dB	31 – -0.5dB

REGISTER 0X2E – RESERVED

REGISTER 0X2F – ADC LRCK SYNC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC1_OSR_VC_ON	7	0 – ADC1 OSR volume off 1 – ADC1 OSR volume on
ADC2_OSR_VC_ON	6	0 – ADC2 OSR volume off 1 – ADC2 OSR volume on
ADC1_DEMOUT_SWMUTE	5	0 – normal 1 – mute ADC1 dem out
ADC2_DEMOUT_SWMUTE	4	0 – normal 1 – mute ADC2 dem out
ADC_ILRCK_DLYSEL	3:2	ADC iLRCK delay index 00 – no delay 01 – delay 1 10 – delay 2

		11 – delay 3
ADC_ILRCK_SYNC_ON	1	0 – ADC iLRCK sync off 1 – ADC iLRCK sync on
ADC_CFDSP_CLKSAME	0	0 – ADC Comb & DSP sync mode0 1 – ADC Comb & DSP sync mode1

REGISTER 0X30 – RESERVED

REGISTER 0X31 – ADC RESET CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
DAC1ADC1_MIX_ON	7	mix DAC1 and ADC1 to ADC1 0 – off 1 – on
DAC2ADC2_MIX_ON	6	mix DAC2 and ADC2 to ADC2 0 – off 1 – on
Reserved	5:3	Reserved
RST_ADC_CFDSP	2	0 – not reset ADC Comb&DSP 1 – reset ADC Comb&DSP
RST_ADC_ALC	1	0 – not reset ADC ALC 1 – reset ADC ALC
RST_ADC_P2S	0	0 – not reset ADC P2S 1 – reset ADC P2S

REGISTER 0X40 – DAC SERIAL PORT CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
DAC_SP_WL	7:5	000 – 24-bit 001 – 20-bit 010 – 18-bit 011 – 16-bit 100 – 32-bit
DAC_SP_LRP	4	I^2S/Left Justified: 0 – L/R normal polarity Left/Right=High/Low (Left Justified) Left/Right=Low/High (I^2S) 1 – L/R invert polarity Left/Right=Low/High (Left Justified) Left/Right=High/Low (I^2S) DSP/PCM mode: 0 – mode A 1 – mode B
DAC_SP_PTL	3:2	00 – I^2S 01 – Left Justified 10 – DSP mode 11 – reserved
DAC1_S2P_SWMUTE	1	0 – normal 1 – mute DAC1 input to 0
DAC2_S2P_SWMUTE	0	0 – normal 1 – mute DAC2 input to 0

REGISTER 0X41 – DAC DSM COUNTER CONTROL, DEFAULT 01111111

Bit Name	Bit	Description
DAC_DSM_OSR	7:0	DAC's over-sampling parameter, lower 8 bits

REGISTER 0X42 – DAC DSP COUNTER CONTROL, DEFAULT 01111111

Bit Name	Bit	Description
DAC_DSP_OSR	7:0	DAC DSP's counter parameter

REGISTER 0X43 – DAC MISC CONTROL 1, DEFAULT 00000000

Bit Name	Bit	Description
DAC_FS_MODE	7	0 – Single speed mode 1 – Double speed mode
DAC_SW_VOL2E1	6	0 – normal 1 – DAC2's volume use DAC1's volume
DAC_DITHER_OFF	5	0 – dither on 1 – dither off
DAC_DSM_CLIPEN	4	0 – normal 1 – clip DAC DSP's output
Reserved	3	Reserved
DAC_ILRCK_SYNC_ON	2	0 – DAC iLRCK sync off 1 – DAC iLRCK sync on
DAC_DSPDSM_CLKSAME	1	0 – DAC filter sync mode0 1 – DAC filter sync mode1
DAC_DSM_OSR_MSB	0	DAC_DSM_OSR most significant bit

REGISTER 0X44 – DAC MIX CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
DAC_ILRCK_DLYSEL	7:6	DAC iLRCK delay index 00 – no delay 01 – delay 1 10 – delay 2 11 – delay 3
DAC1_DEM_SRCSEL	5	0 – normal 1 – DAC2 channel to DAC1 channel
DAC2_DEM_SRCSEL	4	0 – normal 1 – DAC1 channel to DAC2 channel
DAC12_MIX2DAC1_ON	3	Mix DAC1 and DAC2 to DAC1 0 – off 1 – on
DAC12_MIX2DAC2_ON	2	Mix DAC1 and DAC2 to DAC2 0 – off 1 – on
ADC1DAC1_MIX_ON	1	Mix ADC1 and DAC1 to DAC1 0 – off 1 – on
ADC2DAC2_MIX_ON	0	Mix ADC2 and DAC2 to DAC2 0 – off 1 – on

REGISTER 0X45 – DAC MISC CONTROL 2, DEFAULT 00000000

Bit Name	Bit	Description
DAC_RAMCLR	7	0 – normal 1 – clear DSP ram
DAC1_180C	6	0 – normal 1 – output invert
DAC2_180C	5	0 – normal 1 – output invert
Reserved	4	Reserved
DAC_VPPSCALE	3:0	0 – -0.005dB; 4 – -0.2dB; 8 – 0.005dB; 12 – 0.2dB 1 – -0.01dB; 5 – -0.3dB; 9 – 0.01dB; 13 – 0.3dB 2 – -0.05dB; 6 – -0.4dB; 10 – 0.05dB; 14 – 0.4dB 3 – -0.1dB; 7 – -0.5dB; 11 – 0.1dB; 15 – 0.5dB

REGISTER 0X46 – DAC1 VOLUME CONTROL, DEFAULT 10111111

Bit Name	Bit	Description
DAC1_SW_VOLUME	7:0	DAC1 software volume 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X47 – DAC2 VOLUME CONTROL, DEFAULT 10111111

Bit Name	Bit	Description
DAC2_SW_VOLUME	7:0	DAC2 software volume 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X48 – MIX VOLUME CONTROL, DEFAULT 10111110

Bit Name	Bit	Description
ADC2DAC_MIX_VOLUME	7:1	mix volume between ADC and DAC 00h – -95dB 01h – -94dB …… 5Fh – 0dB …… 7Fh – +32dB
Reserved	0	Reserved

REGISTER 0X49 – DAC VC RAMP CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7	Reserved

DAC_S2P_SLOTSEL	6:4	0 – slot 0 1 – slot 1 ..... 7 – slot 7
DAC_VC_RAMPRATE	3:0	0 – 0.125dB/1LRCK 1 – 0.125dB/2LRCK ..... 14 – 0.125dB/2^14LRCK 15 – disable vc ramp

REGISTER 0X4A TO 4C– RESERVED

REGISTER 0X4D – DAC RESET CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:4	Reserved
RST_DAC_S2P	3	0 – normal 1 – reset DAC's S2P
RST_DAC_DSP	2	0 – normal 1 – reset DAC's DSP
RST_DAC_DSM	1	0 – normal 1 – reset DAC's DSM
RST_DAC_DEM	0	0 – normal 1 – reset DAC's DEM

REGISTER 0X60 – VMID CONTROL, DEFAULT 00100111

Bit Name	Bit	Description
VMIDSEL1	7:6	00 –default 01 – fast 10 – slow 11 – NA
Reserved	5:4	Reserved
Reserved	3:2	Reserved
Reserved	1:0	Reserved

REGISTER 0X61 – ANALOG ENABLE CONTROL 1, DEFAULT 00001000

Bit Name	Bit	Description
EN_ANA	7	0 – power down analog circuits 1 – enable analog circuits
EN_IBIASGEN	6	0 – power down analog bias 1 – enable analog bias
EN_DACVREFGEN	5	0 – power down analog DAC reference circuits 1 – enable analog DAC reference circuits
Reserved	4	Reserved
IBIAS_SW	3:2	0 – bias setting level0 1 – bias setting level1 2 – bias setting level2 3 – bias setting level3
VMIDLVL	1:0	0 – VMID=AVDD/2 1 – VMID lvl1 2 – VMID lvl2

		3 – VMID lvl3

REGISTER 0X62 – ANALOG SYSTEM CONTROL1, DEFAULT 10001100

Bit Name	Bit	Description
VSEL	7:4	0100 – setting 4 (lowest) 0101 – setting 5 0110 – setting 6 0111 – setting 7 1000 – setting 8 1001 – setting 9 1010 – setting 10 1011 – setting 11 1100 – setting 12 1101 – setting 13 1110 – setting 14 1111 – setting 15 (highest) Others – not allowed
	3:0	0100 – setting 4 (lowest) 0101 – setting 5 0110 – setting 6 0111 – setting 7 1000 – setting 8 1001 – setting 9 1010 – setting 10 1011 – setting 11 1100 – setting 12 1101 – setting 13 1110 – setting 14 1111 – setting 15 (highest) Others – not allowed

REGISTER 0X63 – ANALOG SYSTEM CONTROL2, DEFAULT 00001000

Bit Name	Bit	Description
Reserved	7	Reserved
Reserved	6	Reserved
Reserved	5	Reserved
DAC_IBIAS_SEL	4	Select bias low 1 - low bias 0 - normal
Reserved	3:0	Reserved

REGISTER 0X64 – ADC ANALOG ENABLE CONTROL , DEFAULT 00110000

Bit Name	Bit	Description
EN_ADCVREFGEN	7	0 – power down MIC1/2 reference circuits 1 – enable MIC1/2 reference circuits
Reserved	6	Reserved
MOD1_RST	5	0 – normal 1 – reset ADC1 to power down state
MOD2_RST	4	0 – normal 1 – reset ADC2 to power down state

EN_MOD1	3	0 – ADC1 power down 1 – ADC1 power up
EN_MOD2	2	0 – ADC2 power down 1 – ADC2 power up
EN_PGA1	1	0 – PGA1 power down 1 – PGA1 power up
EN_PGA2	0	0 – PGA2 power down 1 – PGA2 power up

REGISTER 0X65 TO 0X68 – RESERVED

REGISTER 0X69 – DAC ANALOG CONTROL, DEFAULT 10100000

Bit Name	Bit	Description
SPD_DOWN2	7	0 – normal MODE 1 – power down SEL2
SPD_DOWN1	6	0 – normal MODE 1 – power down SEL1
Reserved	5	Reserved
Reserved	4:2	Reserved
HPRSW	1	0 – lineout 1 – enable HPdriver for headphone output
HPLSW	0	0 – lineout 1 – enable HPdriver for headphone output

REGISTER 0X6A – RESERVED

REGISTER 0X6B – ANALOG LOW POWER CONTROL 1, DEFAULT 00000000

Bit Name	Bit	Description
LP_VREF	7	0 – normal mode 1 – low power mode
LP_DACREF	6	0 – normal mode 1 – low power mode
LP_DAC	5	0 – normal mode 1 – low power mode
LP_ADCREF	4	0 – normal mode 1 – low power
LP_MOD2	3	0 – normal 1 – low power
LP_MOD1	2	0 – normal 1 – low power
Reserved	1:0	Reserved

REGISTER 0X6C – ANALOG LOW POWER CONTROL 2, DEFAULT 00000000

Bit Name	Bit	Description
LP_PGA1	7	0 – normal 1 – low power
LP_PGA2	6	0 – normal 1 – low power
LP_VMOD	5	0 – normal 1 – low power

LP_VPGA	4	0 – normal 1 – low power
LP_PGA11	3	0 – normal 1 – low power
LP_PGA12	2	0 – normal 1 – low power
LP_PGA21	1	0 – normal 1 – low power
LP_PGA22	0	0 – normal 1 – low power

REGISTER 0X6D – ADC ANALOG CONTROL1, DEFAULT 00101000

Bit Name	Bit	Description
DMIC_MIC1P_ON	7	0 – off 1 – on
DMIC_MIC1N_ON	6	0 – off 1 – on
ADCBIAS_SW	5:4	Select bias 00 - 25% 01 - 50% 10 - 75% 11 – 100%
MODF_SW	3:0	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9 1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed

REGISTER 0X6E – PGA1 ANALOG CONTROL, DEFAULT 10001000

Bit Name	Bit	Description
PGA1_SW	7:4	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9 1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed

PGA2_SW	3:0	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9 1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed

REGISTER 0X6F – ADC ANALOG CONTROL2, DEFAULT 10000110

Bit Name	Bit	Description
MOD1 _SW	7:4	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9 1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed
MOD2_SW	3:0	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9 1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed

REGISTER 0X70 – ADC ANALOG CONTROL3, DEFAULT 01100110

Bit Name	Bit	Description
MODS _SW	7:4	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9

		1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed
MODC_SW	3:0	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9 1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed

REGISTER 0X71 – ADC ANALOG CONTROL4, DEFAULT 01000100

Bit Name	Bit	Description
MODREF_SW	7:4	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9 1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed
MODVM_SW	3:0	0100 - setting level4 (lowest) 0101 - setting level5 0110 - setting level6 0111 - setting level7 1000 - setting level8 1001 - setting level9 1010 - setting level10 1011 - setting level11 1100 - setting level12 1101 - setting level13 1110 - setting level14 1111 - setting level15 (highest) Others –not allowed

REGISTER 0X72 – PGA1 GAIN CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7	Reserved
LINSEL	6:4	001 – MIC1P – MIC1N 101 – MIC1P 110 – MIC2P Others – not allowed
MIC1GAIN_SETTING	3:0	0000 – 0dB 0001 – 3.5dB 0010 – 6.5dB 0011 – 9.5dB 0110 – 12.5dB 0111 – 15.5dB 1000 – 18.5dB 1001 – 21.5dB 1010 – 24.5dB 1011 – 27.5dB 1100 – 30.5dB 1101 – 33.5dB 1110 – 36.5dB Others – not allowed

REGISTER 0X73 – PGA2 GAIN CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reversed	7	Reserved
RINSEL	6:4	001 – MIC2N – MIC2P 101 – MIC2P 110 – MIC1P Others – not allowed
MIC2GAIN_SETTING	3:0	0000 – 0dB 0001 – 3.5dB 0010 – 6.5dB 0011 – 9.5dB 0110 – 12.5dB 0111 – 15.5dB 1000 – 18.5dB 1001 – 21.5dB 1010 – 24.5dB 1011 – 27.5dB 1100 – 30.5dB 1101 – 33.5dB 1110 – 36.5dB Others –not allowed

REGISTER 0XF0 – CHIP MISC CONTROL, DEFAULT 00010000

Bit Name	Bit	Description
EXT_LRCK_EXTEND	7	0 – normal internal LRCK pulse width 1 – larger internal LRCK pulse width
CLKDBL_SEL	6:4	clock doubler duty cycle index 000 – level 0

		001 – level 1 010 – level 2 011 – level 3 100 – level 4 101 – level 5 110 – level 6 111 – level 7
STDM TDMIN_SEL	3	0 – MCLK pin as TDMIN 1 – DSDIN pin as TDMIN
ADCDAT2DACDAT_ON	2	select ADC's serial output as DAC's input 0 – off 1 – on
IBCLKLRCK_SEL	1	0 – according to M/S mode 1 – master mode's LRCK/SCLK as internal LRCK/SCLK before normal operation
CSM_LRCKSEL	0	0 – normal 1 – use master mode SCLK/LRCK to csm

REGISTER 0XF1 – CSM STATE REPORT, DEFAULT 00000000

Bit Name	Bit	Description
LRCKCNT_FSEL	7:6	state time unit 00 – 8LRCK(short state),64LRCK(long state) 01 – 2LRCK(short state),16LRCK(long state) 10 – 1LRCK(short state),8LRCK(long state) 11 – 16LRCK(short state),128LRCK(long state)
Reserved	5	Reserved
CSM_STATE	4:0	chip state machine 00000 – power down 00111 – Standby 01101 – Normal others – reserved

REGISTER 0XF2 – PULL DOWN CONTROL, DEFAULT 01111111

Bit Name	Bit	Description
Reserved	7	Reserved
MIC1P_PULLDWN	6	MIC1P pin internal pull down resister 1 – on 0 – off
CAD_PULLDWN	5	AD0 pin internal pull down resister 1 – on 0 – off
ADCDAT_PULLDWN	4	ASDOUT pin internal pull down resister 1 – on 0 – off
DACDAT_PULLDWN	3	DSDIN pin internal pull down resister 1 – on 0 – off
LRCK_PULLDWN	2	LRCK pin internal pull down resister 1 – on 0 – off
BCLK_PULLDWN	1	SCLK pin internal pull down resister

		1 – on 0 – off
MCLK_PULLDWN	0	MCLK pin internal pull down resister 1 – on 0 – off

REGISTER 0XF3 – ISOLATION CONTROL, DEFAULT 11000111

Bit Name	Bit	Description
D2B_ISO_EN	7	Force signals from VDDD to VDDB to fixed level(0 or 1) 0 – normal 1 – on
A2D_ISO_EN	6	Force signals from VDDA to VDDD to fixed level(0 or 1) 0 – normal 1 – on
D2A_DET_EN	5	power detect enable from VDDD to VDDA 0 – detect off 1 – detect on
D2B_DET_EN	4	power detect enable from VDDD to VDDB 0 – detect off 1 – detect on
A2D_DET_EN	3	power detect enable from VDDA to VDDD 0 – detect off 1 – detect on
D2B_DET_ISOB	2	power-detection's isolate valid flag from VDDD to VDDB when D2B_DET_EN enable 0 – isolation flag valid 1 – normal
A2D_ISO_ISOB	1	power-detection's isolate valid flag from VDDA to VDDD when A2D_DET_EN enable 0 – isolation flag valid 1 – normal
DVDD_RST_ON	0	reset DVDD power domain 0 – normal 1 – reset logic in DVDD power domain

REGISTER 0XF4 – CSM STATE CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
MCLK_OFF_FLAG	7	MCLK stop flag 0 – normal 1 – MCLK stop detected
LRCK_OFF_FLAG	6	LRCK stop flag 0 – normal 1 – LRCK stop detected
Reserved	5	Reserved
FORCE_CSM_STATE	4:0	Force chip state machine 10000 – force to power down 00111 – force to Standby 01101 – force to Normal others – reserved

REGISTER 0XFD – CHIP ID1, DEFAULT 10000011

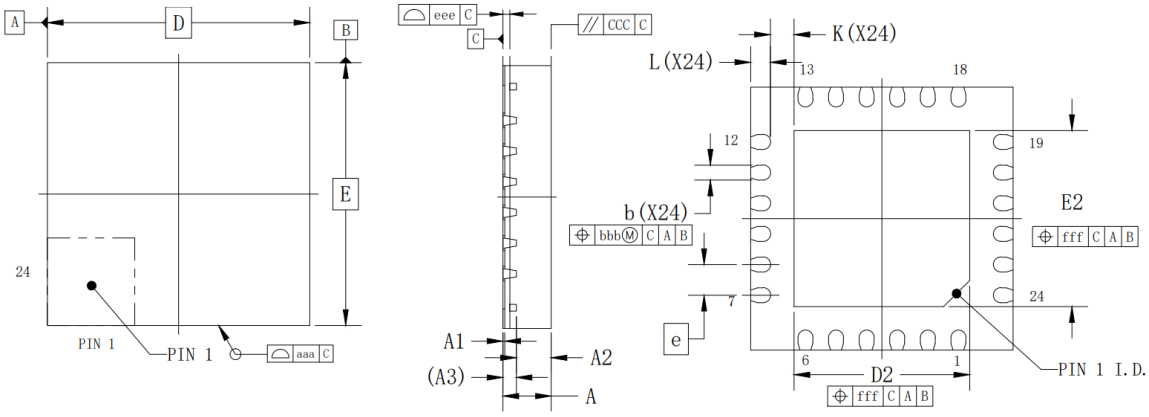
Bit Name	Bit	Description
DEVICE_ID1	7:0	Chip ID

REGISTER 0XFE – CHIP ID0, DEFAULT 10001001

Bit Name	Bit	Description
DEVICE_ID0	7:4	Chip ID

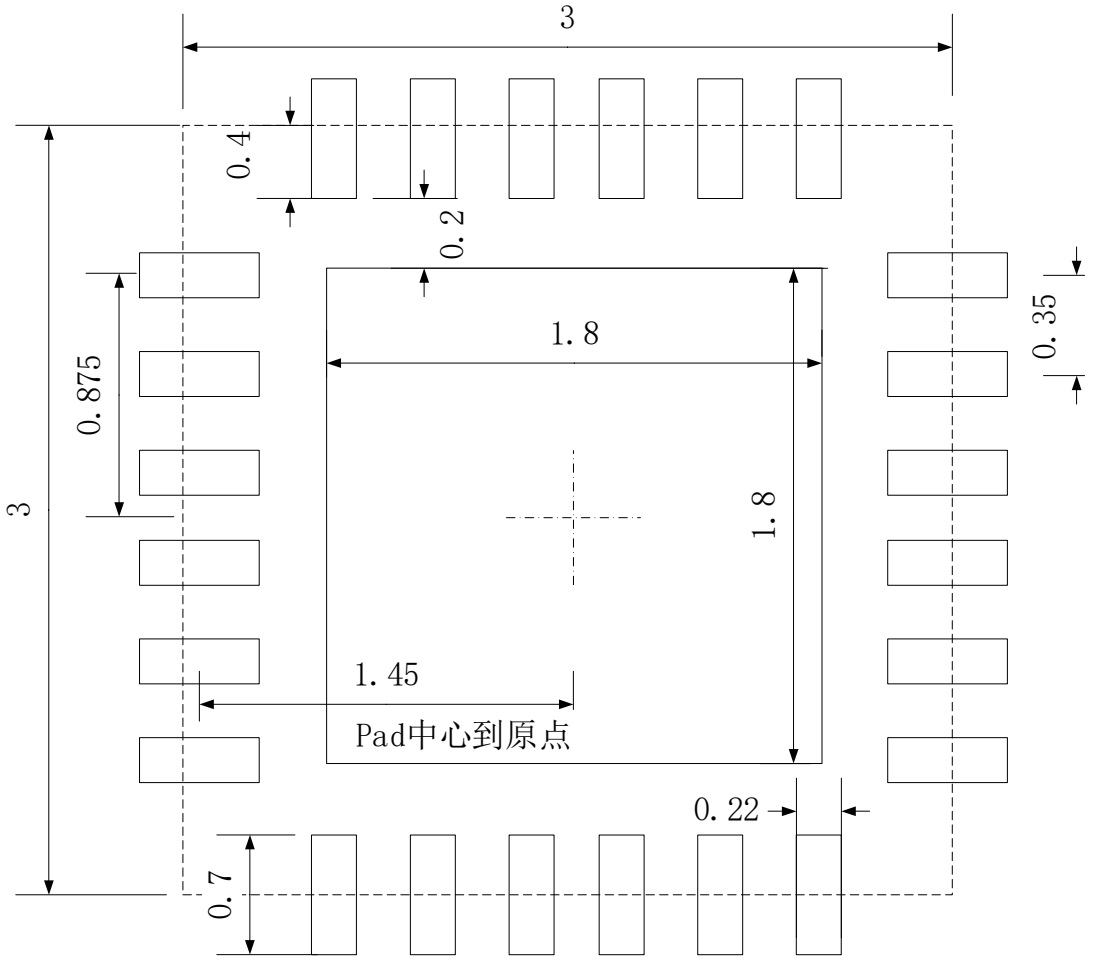
9. PACKAGE (UNIT: MM)

QFN-24L-3X3(P0.35T0.55) Package Outline Drawing



TOP VIEW SIDE VIEW BOTTOM VIEW

Item	Symbol	Minimum	Normal	Maximum
Total Thickness	A	0.50	0.55	0.60
Stand Off	A1	0	0.02	0.05
Molding Thickness	A2	---	0.40	---
LF Thickness	A3		0.152 REF	
Lead Width	b	0.12	0.17	0.22
Body Size	D		3 BSC	
	E		3 BSC	
Lead Pitch	e		0.35 BSC	
Exposed Pad Size	D2	1.60	1.70	1.80
	E2	1.60	1.70	1.80
Lead Length	L	0.20	0.30	0.40
Lead tip to Exposed Pad	K		0.35 REF	
Package Edge Tolerance	aaa		0.10	
Molding Flatness	ccc		0.10	
Coplanarity	eee		0.08	
Lead Offset	bbb		0.07	
Exposed Pad Offset	fff		0.10	


3
0.4
0.2
0.875
3
1.8
1.8
0.35
1.45
Pad中心到原点
0.22
0.7

10.CORPORATE INFORMATION

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