DATA SHEET

FocalTech

# FT3168

## Self-Capacitance Touch Controller

***Preliminary***

Jun.18th, 2021

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## INTRODUCTION

The FT3168is a single-chip capacitance touch panel controller IC with a built-in 16-bitenhancedMicro-controller unit (MCU). It adopts the self-capacitance technology, which supports multi-touch. In conjunction with a self-capacitance touch panel, The FT3168implementthe user-friendly input function and is widely used in various industry application and other touch application.

## FEATURES

- Self-Capacitive Sensing Techniques support single point touch and gesture or two-point touch.
- Absolute X and Y coordinates or gesture
- 1 point and gestures / 2 points supported
- Supports up to 16 channels of sensors
- Auto-Calibration: Insensitive to background capacitance and environmental variations
- High immunity to RF and Power interferences
- Excellent waterproof performance
- Support single film material TP and triangle pattern without additional shield
- Fast Report Rate: up to 100Hz
- Serial interfaces: $I^2C$slave, up to 400Kbps
- Built-in 16-bit enhanced MCU
- Built-in 1.4V and 1.8V LDO Regulators
- Built-in 30MHz and 35KHz Oscillator
- Internal accuracy ADC and smooth filters
- Power Supply Mode
  - Power Supply:2.8V-3.6V
  - independent IOVCC:1.8V-3.6V
- High efficient power management with 3 Operating Modes
  - Active Mode
  - Monitor Mode
  - Sleep Mode
- Operating Temperature Range: -40°C to +85°C
- Package:
  - QFN3*3*0.55mm 0.35mm/pitch

# 1.OVERVIEW

## 1.1. TYPICAL APPLICATIONS

FT3168 accommodates a wide range of applications with a set of buttons up to a 2D touch sensing device, their typical applications are listed below.

- Mobile phones, smart phones
- Smart watch
- Wrist Band
- GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras
- MIDs

FT3168 support up to 1.4-inch Touch Panel; users may find out their target IC from the specs listed in the following table:

| Model Name | Panel | Package | | | Touch Panel Size |
|---|---|---|---|---|---|
| | Channel | Type | Pin | Size | |
| FT3168 | 16 | QFN3X3 | 25 | 3mm×3mm | ≤2 inch |

# 2.FUNCTIONAL BLOCK DESCRIPTION

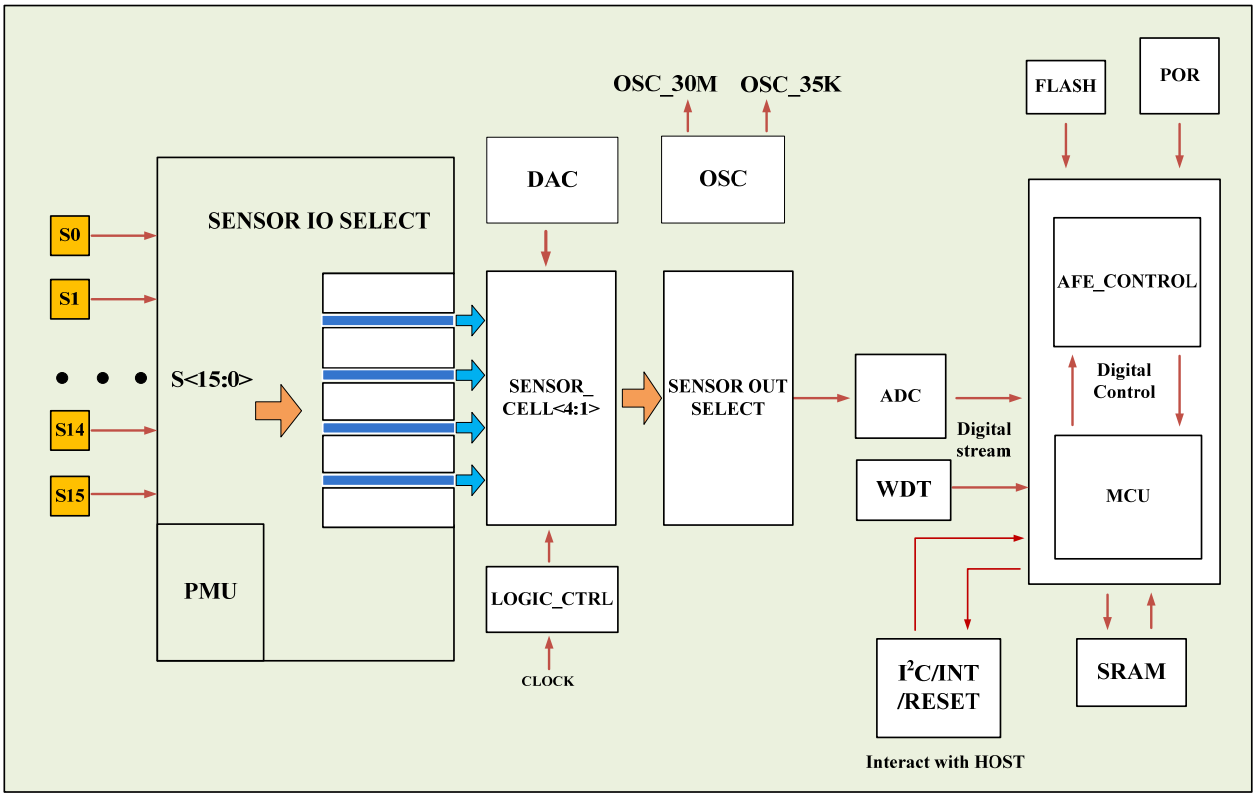



**Figure 2-1FunctionBlock Diagram of FT3168**

## 2.1. Architecture Overview

### 2.1.1 AFE and AFE Controller

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So it supports both driver and Sensor functions.Key parameters to configure this circuit can be sent via serial interfaces.

### 2.1.2 MCU

For MCU, larger program and data memories are supported. Furthermore, a Flash Memory is implemented to store programs and some key parameters.Complex signal processing algorithms are implemented by MCU to detect the touches reliablyand efficiently. Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

### 2.1.3 Operation Modes

- SDA/SCL:$I^2C$ Interface for data exchange with host.
- INT: Interrupt signal to inform the host processor that touch data is ready for read.
- RESETB: External Hardware reset for FT3168; low is active.

### 2.1.4 Watchdog Timer

Watchdog timer is implemented to ensure the robustness of the chip.

### 2.1.5 PMU

PMU is power manage unit, to generate voltage power / reference for internal circuit.

## 2.2. Operating Mode

FT3168 operates in the following three modes:

### 2.2.1. Active Mode

In this mode, FT3168 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT3168to speed up or to slow down.

### 2.2.2. Monitor Mode

- In this mode, the FT3168 is scanning the touch sensor at a lower scan rate, which is user programmable. The purpose of this mode is to detect whether there is a touch on the screen. If a touch is detected, the FT3168 will switch to active mode immediately. In the case of mobile phone applications, the display is typically “on” in this mode.
- In Monitor mode, the FT3168 does not perform full touch tracking. It only looks for a valid touch. No coordinates or sensor image are calculated or reported.

### 2.2.3. Sleep Mode

FT3168 is not scanning the touch sensor. The analog circuits are turned off and the MCU stopped. The FT3168will wake up and respond to“RESETB” or“Wakeup”signal from host processor. The display is typically off in this mode.

### 2.3. Host Interface

FT3168 communicates to the host through the I²C interface and follows the I²C protocol. I²C bus utilize the SCL and SDA, a two-wire synchronous communication interface and can operate at a maximum bit rate of 400kbps. FT3168 can be part of a single-slave or a multi-slave environment.

When FT3168 is in Monitor mode or Sleep mode, host will not be able to communicate with the touch IC via I²Cafter accessing any other slave device on the same bus. In order to maintain I²C communication during Monitor/Sleep mode between host and touch IC in them multi-slave environment, the FT3168 firmware will clear I²C state machine periodically. Wake up status via a touch event could also change FT3168 from Monitor/Sleep mode to Active mode and clear the I²C state machine, hence ensuring the touch FT3168's I²C function properly.

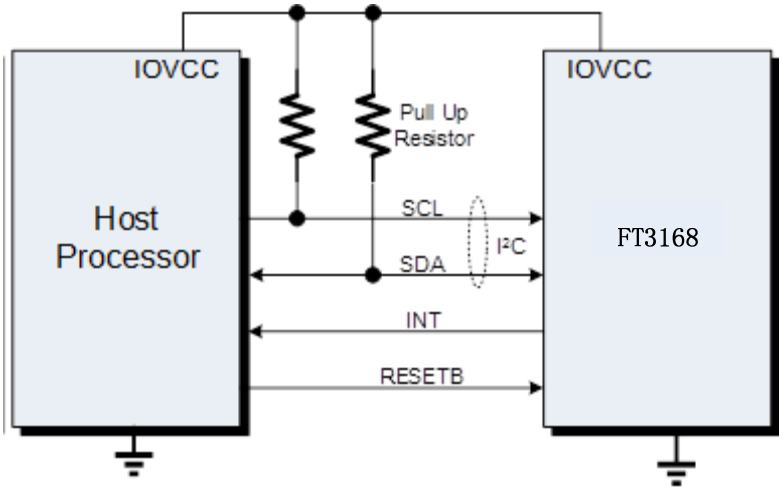



**Figure 2-2 HOST Interface of FT3168**

#### 2.3.1. I²C Interface Timing

The I²C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-3**

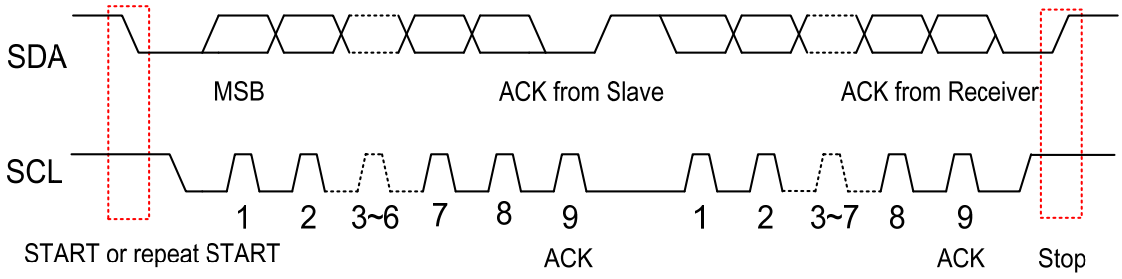



**Figure 2-3I²C Serial Data Transfer Format**

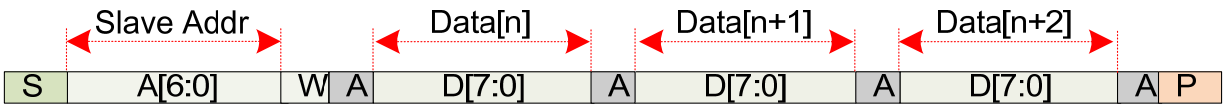



**Figure 2-4I²C Master Write, Slave Read**

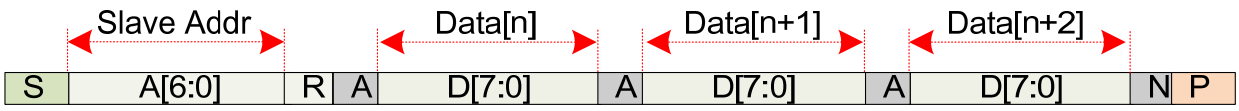



**Figure 2-5I²C Master Read, Slave Write**

Table 2-1 lists the meanings of the mnemonics used in the above figures.

**Table 2-1 Mnemonics Description**

| Mnemonics | Description |
|---|---|
| S | I²C Start or I²C Restart |
| A[6:0] | Slave address |
| R/W | READ/WRITE bit, '1' for read, '0'for write |
| A(N) | ACK(NACK) |
| P | STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet) |

I²C Interface Timing Characteristics is shown in Table 2-2.

**Table 2-2 I²C Timing Characteristics**

| Parameter | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| SCL frequency (fast mode support) | 0 | 100 | 0 | 400 | KHz |
| Clock low period | 4.7 | - | 1.3 | - | us |
| Clock high period | 4.0 | - | 0.6 | - | us |
| Bus free time between a STOP and START condition | 4.7 | - | 1.3 | - | us |
| Hold time (repeated) START condition | 4.0 | - | 0.6 | - | us |
| Data setup time | 250 | - | 100 | - | ns |
| Setup time for a repeated START condition | 4.7 | - | 0.6 | - | us |
| Setup Time for STOP condition | 4.0 | - | 0.6 | - | us |

## 3.ELECTRICAL SPECIFICATIONS

### 3.1. Absolute Maximum Ratings

**Table 3-1 Absolute Maximum Ratings**

| Item | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Power Supply Voltage | AVDD - AVSS | -0.3 ~ +3.6 | V | 1, 2 |

| | | | | |
|---|---|---|---|---|
| I/O Communication Voltage | IOVCC<br>(Internal generated when external IOVCC power is not existed) | 1.75~1.85 | V | 1 |
| | IOVCC<br>(Internal LDO IOVCC is turned off when external IOVCC power is existed) | 1.6~3.6 | V | 1 |
| Operating Temperature | Topr | -40 ~ +85 | ℃ | 1 |
| Storage Temperature | Tstg | -55 ~ +150 | ℃ | 1 |

**Notes**

1. If used beyond the absolute maximum ratings, FT3168 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure AVDD (high) ≥AVSS (low).

### 3.2. DC Characteristics

**Table 3-2 DC Characteristics (Ta=-40~105℃)**

| Item | Symbol | Test Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Input high-level voltage | VIH | | 0.7 × IOVCC | - | IOVCC | V | |
| Input low -level voltage | VIL | | -0.3 | - | 0.3 × IOVCC | V | |
| Output high -level voltage | VOH | IOH=－0.1mA | 0.7 × IOVCC | - | - | V | |
| Output low -level voltage | VOL | IOH=0.1mA | - | - | 0.3 × IOVCC | V | |
| I/O leakage current | ILI | Vin=0~AVDD | -1 | - | 1 | μA | |
| Current consumption （Normal operation mode） | Iopr | AVDD=2.8V<br>Ta=25℃ MCLK=15MHz | - | 1.5 | - | mA | |
| Current consumption （Monitor mode） | Imon | AVDD=2.8V<br>Ta=25℃ MCLK=15MHz | - | 30 | - | μA | |
| Current consumption （Sleep mode） | Islp | AVDD=2.8V<br>Ta=25℃ | - | 10 | - | μA | |
| Power Supply voltage | AVDD | | 2.8 | - | 3.6 | V | |

### 3.3. AC Characteristics

**Table 3-3 AC Characteristics of Oscillators**

| Item | Symbol | Test Condition | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| OSC clock | fosc1 | AVDD= 2.8V；Ta=25℃ | -1% | 30 | +1% | MHz | |

**Table 3-4 AC Characteristics of sensor**

| Item | Symbol | Test Condition | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Sensor acceptable clock | ftx | AVDD= 2.8V；Ta=25℃ | 0 | 100 | 300 | KHz | |
| Sensor output rise time | Ttxr | AVDD= 2.8V；Ta=25℃ | - | 100 | - | nS | |
| Sensor output fall time | Ttxf | AVDD= 2.8V；Ta=25℃ | - | 80 | - | nS | |

### 3.4. Power ON and Reset Sequence

The GPIO such as INT and I2C are advised to be low before powering on. Reset should be pulled down to be low before powering on. INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If power down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

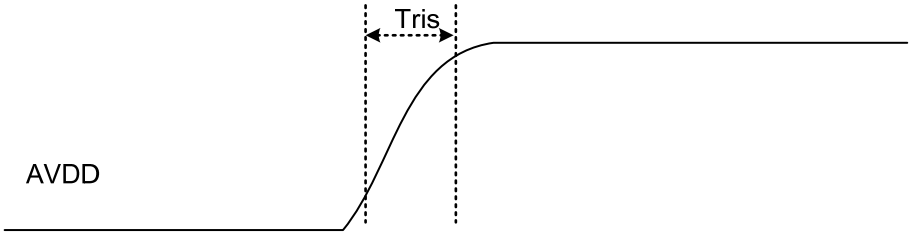



**Figure 3-1 Power on time**

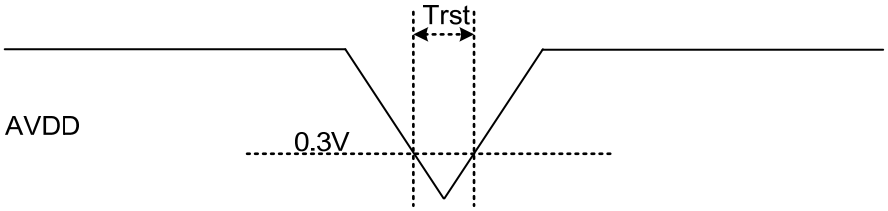



**Figure 3-2 Power down requirement**

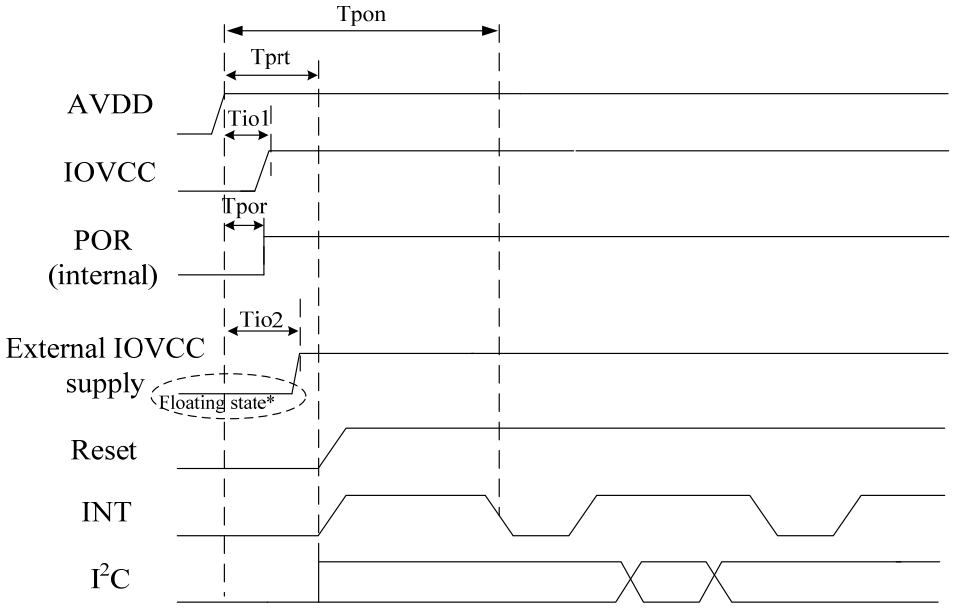



**Figure 3-3Power on Sequence (for external IOVCC supply exist)**

Notes*: external IOVCC supply should be in a floating state when it is not on to avoid unexpected leakage.

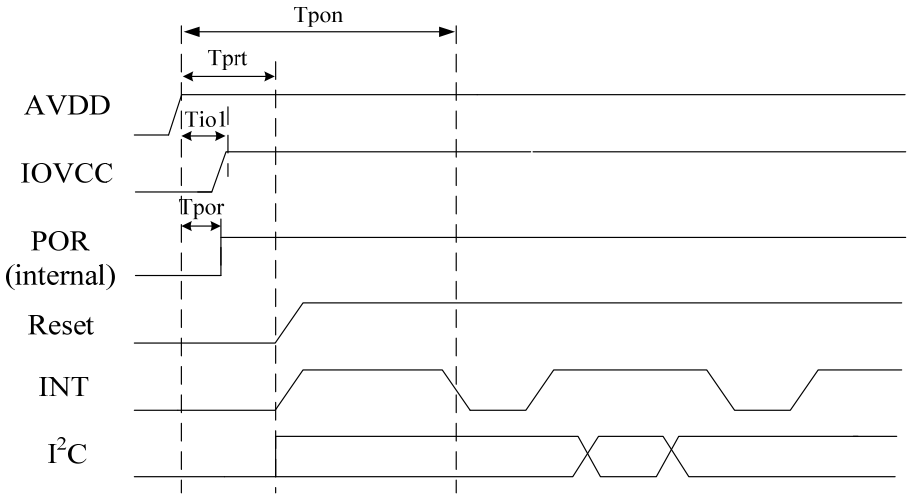



**Figure 3-4Power on Sequence (for external IOVCC supply not exist)**

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

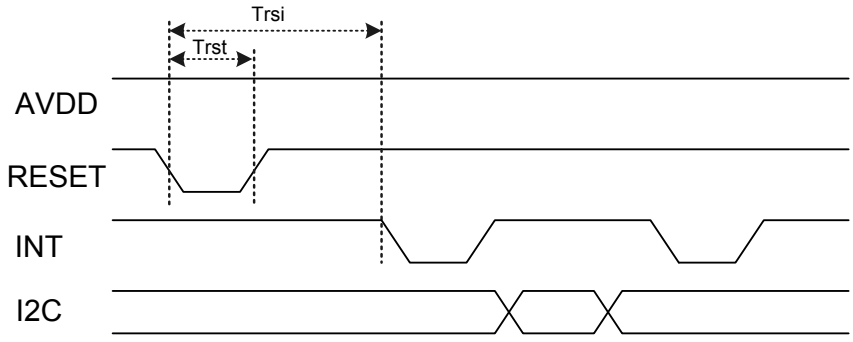



**Figure 3-5 Reset Sequence**

The following is the power down sequence.

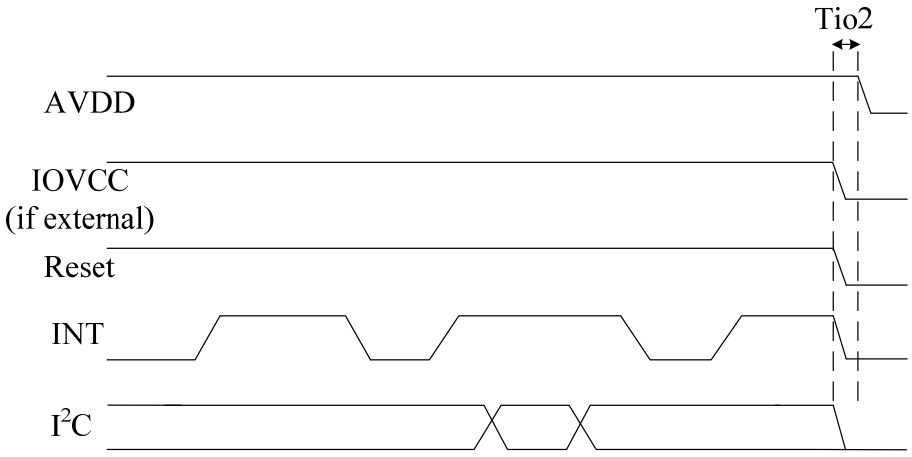



**Figure 3-6 Power down Sequence (for external IOVCC)**

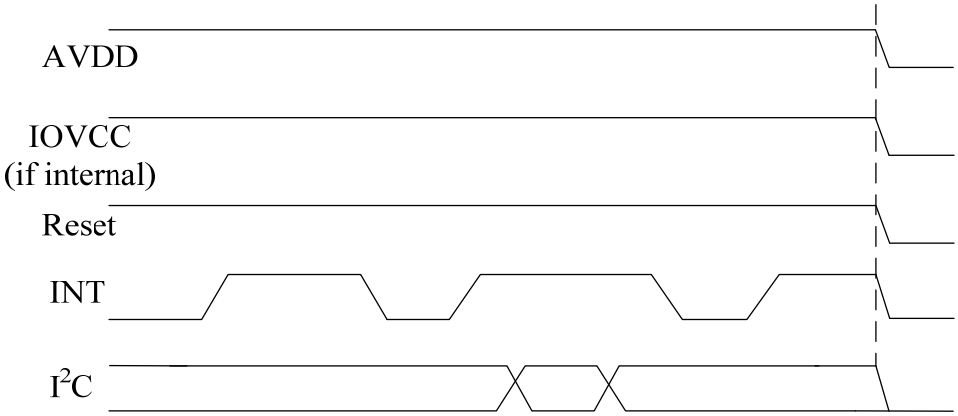


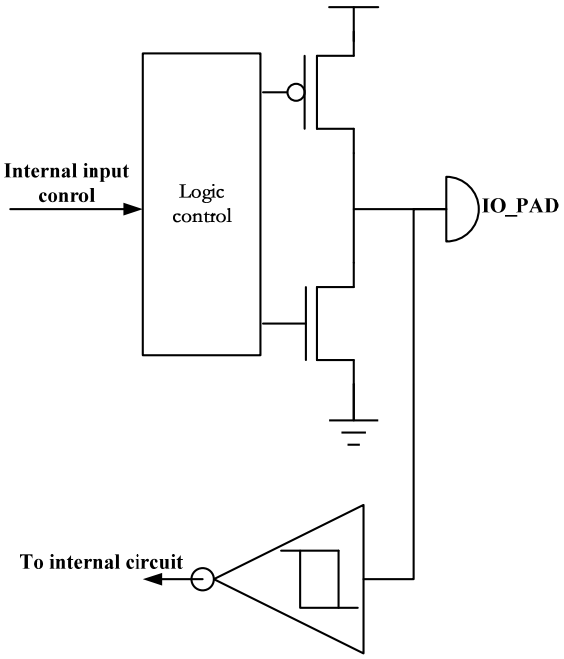

**Figure 3-7 Power down Sequence (for internal IOVCC)**

**Table 3-5Power on/Reset/Wake Sequence Parameters**

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| Tris | Rise time from 0.1VDD to 0.9VDD | - | 3 | ms |
| Tpor | Time of internal POR ready after AVDD power on | 1 | - | ms |
| Tio1 | Time of IOVCC rising after AVDD power on | 1 | - | ms |
| Tio2 | Time of external IOVCC supply after AVDD power on or time of external IOVCC supply before AVDD power down | 1 | - | ms |
| Tpon | Time of starting to report point after powering on | 70 | - | ms |
| Tprt* | Time of RESETB being low after power on | 3 | - | ms |
| Trsi | Time of starting to report point after resetting | 70 | - | ms |
| Trst* | Reset time | 5 | - | ms |

Notes*: reset time should not to be too long, because when reset is low, all the control logic would be fixed to be the default value, and the system state is fixed to be a default state.

### 3.5. IO PORT CIRCUIT



## 4.PIN CONFIGURATION

**Table 4-1 Pin Definition of FT3168**

| Name | Pin No. | Type | Description |
|---|---|---|---|
| S0 | 1 | I/O | Capacitance sensor |
| S1 | 2 | I/O | Capacitance sensor |
| S2 | 3 | I/O | Capacitance sensor |
| S3 | 4 | I/O | Capacitance sensor |
| S4 | 5 | I/O | Capacitance sensor |
| S5 | 6 | I/O | Capacitance sensor |
| S6 | 7 | I/O | Capacitance sensor |
| S7 | 8 | I/O | Capacitance sensor |
| S8 | 9 | I/O | Capacitance sensor |
| S9 | 10 | I/O | Capacitance sensor |
| S10 | 11 | I/O | Capacitance sensor |
| S11 | 12 | I/O | Capacitance sensor |
| S12 | 13 | I/O | Capacitance sensor |
| S13 | 14 | I/O | Capacitance sensor |
| S14 | 15 | I/O | Capacitance sensor |
| S15 | 16 | I/O | Capacitance sensor |
| VREF | 17 | PWR | Generated internal reference voltage. A 1μF ceramic capacitor to ground is required. |
| AVDD | 18 | PWR | Analog power supply, A 1μF ceramic capacitor toground is required |
| IOVCC | 19 | PWR | I/O power supply |
| SCL | 20 | I/O | I2C clock input |
| SDA | 21 | I/O | I2C data input and output |
| INT | 22 | I/O | External interrupt to the host |
| RSTN | 23 | I | External Reset, Low is active |
| DVDD | 24 | PWR | Digital power supply. A 1μF ceramic capacitor toground is required. |
| GND | 25 | PWR | Power ground. The pin that needs to be connected to the ground is exposed die attach pad. |

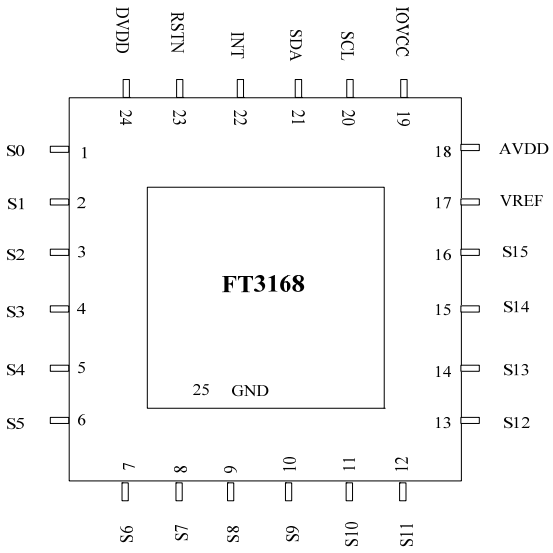
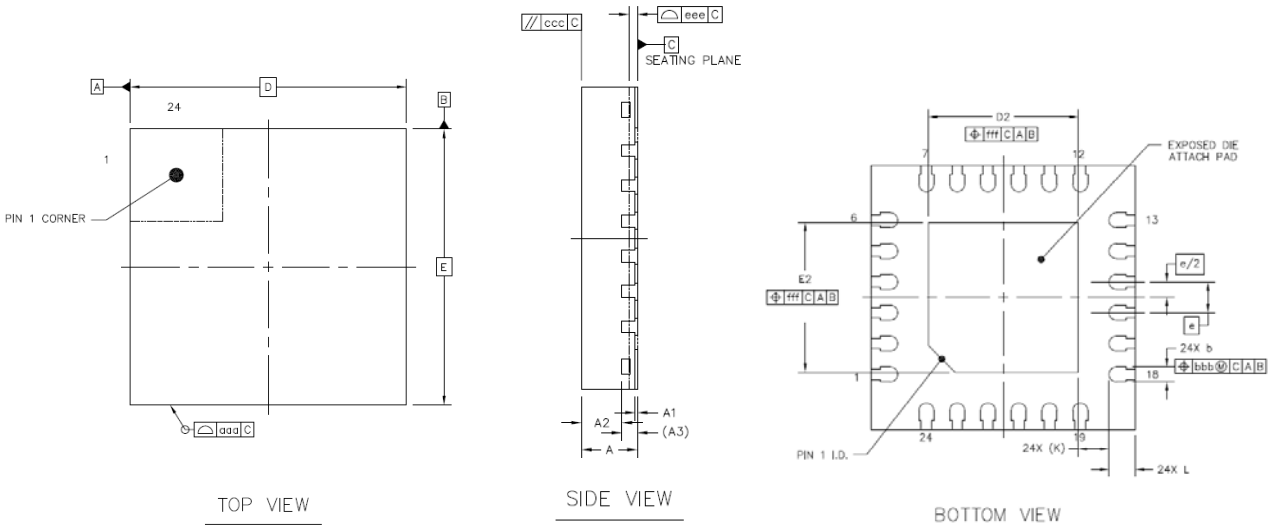



**Figure 4-1 FT3168 Package Diagram**

## 5.ACKAGE INFORMATION

### 5.1. Package Information of QFN3X3_24L Package




TOP VIEW SIDE VIEW BOTTOM VIEW

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.5 | 0.55 | 0.6 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.4 | --- |
| L/F THICKNESS | | A3 | 0.152 REF | | |
| LEAD WIDTH | | b | 0.12 | 0.17 | 0.22 |
| BODY SIZE | X | D | 3 BSC | | |
| | Y | E | 3 BSC | | |
| LEAD PITCH | | e | 0.35 BSC | | |
| EP SIZE | X | D2 | 1.6 | 1.7 | 1.8 |
| | Y | E2 | 1.6 | 1.7 | 1.8 |
| LEAD LENGTH | | L | 0.2 | 0.3 | 0.4 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | 0.35 REF | | |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | ccc | 0.1 | | |
| COPLANARITY | | eee | 0.08 | | |
| LEAD OFFSET | | bbb | 0.07 | | |
| EXPOSED PAD OFFSET | | fff | 0.1 | | |
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## 6.REVISION HISTORY

| Date | Revision # | Description | Page | Auditor |
|---|---|---|---|---|
| Jan. 23th,2019 | 0.1 | Original. | All | Jack.huang, 张金磊，李瑞兴，杜洪洋，李华 |
| Aug.20th,2019 | 0.2 | Update sleep mode current consumption | 11 | 李华 |
| Otc.18th,2019 | 0.3 | Modify Figure 3-2, Figure 3-4, Figure 3-5.<br>Update Tpon and Trsi parameters minimum value.<br>Add Figure 4-1 Package Diagram | 12,13,15 | 李华、李瑞兴 |
| Nov.22th,2019 | 0.4 | Update OSC frequency<br>And modify Table2-2 | 4,5,10<br>9 | 李瑞兴<br>李华 |
| Jul.03th,2020 | 0.5 | Modify IC support touch panel size<br>Modify IIC interface description<br>Update Power on sequence diagram<br>Update Power on/Reset/Wake Sequence Parameters | 5,7,11,12 | 李华，张金磊，黄飚 |
| Jun.18th,2021 | 0.6 | Update power down sequence | 12、13 | 李瑞兴 |