Meridian Innovation MI1602 Thermal Camera Module

Data sheet (preliminary)

Revision 1.0.2 – December 2024

Contents

1. Overview

Meridian Innovation's MI1602 is a long-wave infrared (LWIR) thermal imaging camera module, powered by SenXor™ technology and featuring 19,200 pixels arranged in a 160 by 120 pixel focal point array (FPA).

SenXor™ technology is Meridian Innovation's patented CMOS-compatible thermal sensor array. Its hybrid architecture yields the synergy of microbolometer and thermopile pixel technology. The sensor array is wafer-level vacuum-packaged (WLVP). WLVP refers to a microchip that is made of two CMOS wafers bonded together with a vacuum cavity in between. The base wafer – referred to as the *active wafer* -- contains the thermal sensor array and the readout circuit. The top wafer – referred to as the *cap wafer* – transmits LWIR radiation while keeping the pixels of the array in vacuum for optimal operation.

The WLVP chip is attached and wire-bonded to a reinforced flexible PCB substrate and its housing includes a lens assembly designed to transmit LWIR radiation and focus it on the thermal sensor array, as shown in Fig. 1. The flexible PCBA has an extension for interfacing an FPC-connector on the host system.

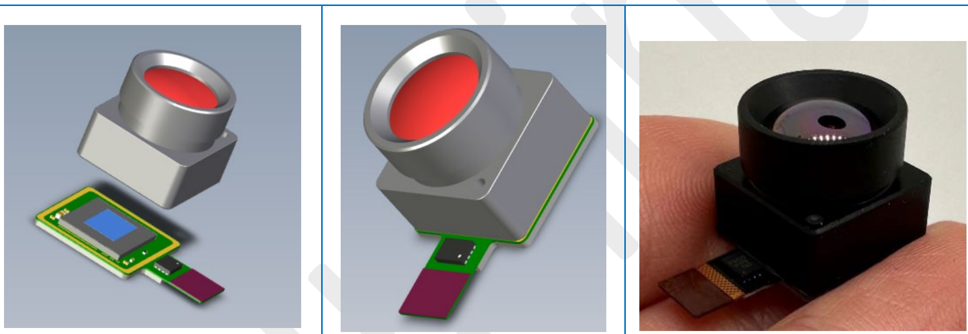


Fig. 1. Schematic diagram of the MI1602M5S camera module and a picture of the actual module with a dual-element Si lens MI1602M5S.

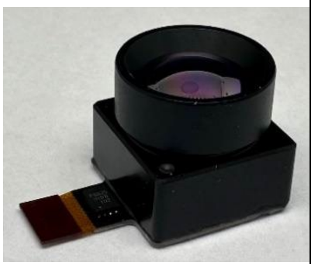
2. Key Features

- 19,200 pixels arranged in a 160 (H) by 120 (V) pixel array, rendering sufficient complexity in the thermal image to enable thermal data analytics and inference
- Radiometric output, i.e. per pixel temperature output
- Factory calibration per pixel, resulting in high uniformity and accuracy of the temperature readout
- Continuous operation and thermal video stream due to shutterless design
- Intrinsic sensor protection due to WLVP
- Multiple lens options offering different field of view

3. ORDER INFORMATION

The MI1602 ordering code includes a three-symbol encoding of the specific lens and packaging, as per the Table 1.

Table 1. ORDERING INFORMATION

Product Code & Resolution (HxV)	Image	Package HxWxH, mm	Lens	FoV (H/V/D), °	Minimum Quantity
MI1602M5S 160 x 120		13.0 x 13.0 x 12.6	2-element, chalcogenide, fixed mount, F# 1.0	45/34/56	1000
MI1602M6C 160 x 120		13.0 x 13.0 x 13.2	1-element, carbo-hydrate , fixed mount, F# 1.0	88/66/110	1000

Note: FoV figures are subject to up to $\pm$ 5% tolerance.

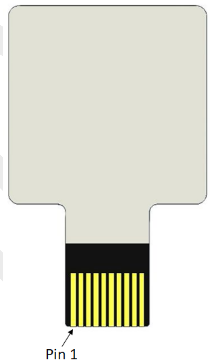
Package dimension are subject to $\pm$ 50um tolerance.

4. Pin Information

4.1. PCBA Package with FPC Extension

The MI1602 interfaces to a host system via the integral FPC extension through a 10-pin FPC-connector with 0.5 mm pitch. The pin information is shown in Table 2.

Table 2. FPC Connector Pin Description

Pin No	Pin Name	Type	Description
1	VSS	P	Ground *(left-most when looked at from the back)* 
2	VDD	P	3.3 V Power supply
3	DATA_AV	O	Data Available signal
4	SSFLASHN	I	SPI Slave Select, Flash Memory on the MI1602 PCBA (active low)
5	SCK	I	SPI Bus Clock
6	MISO	O	Master Input Slave Output of the SPI Bus
7	MOSI	I	Master Output Slave Input of the SPI Bus
8	SSN	I	SPI Slave Select (active low)
9	RSTN	I	System Reset (active low)
10	SYSCLK	I	System Clock

5. Recommended System Setup

The recommended usage of MI1602 camera module is in combination with its companion integrated circuit MI48xx as seen in Fig. 2.

The MI48xx plays the role of a low-level thermal imaging processor, and handles the exact control signalling necessary to capture raw sensor data from the thermal imaging array of the MI1602. It also provides standard interfaces for communication with a host controller. In the case of the MI48xx for example, these interfaces are the Inter-Integrated Circuit (I^2C) bus – for conveying commands and obtaining status, and the serial peripheral interface (SPI) – for the readout of thermal data obtained by the MI48xx. In addition to the I^2C and SPI interfaces, the MI48xx provides a digital signal to alert the host controller that new thermal image data is available, as shown in Fig. 2.

The MI48xx also performs low-level processing of the data read out from the camera modules. Specifically, it handles the per-pixel calibration, performs bad pixel correction (BPC), and converts the raw camera data to temperature, and in this way greatly facilitates the development of applications embedding the MI1602 camera module.

To ensure the best accuracy and stability of the temperature readout, a dedicated voltage regulator for the camera module is also recommended.

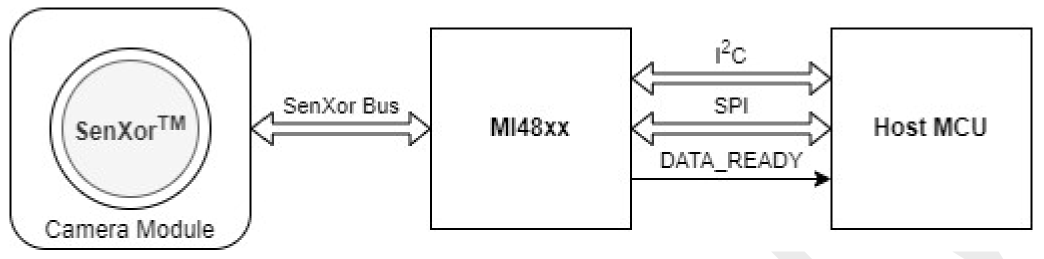


Fig. 2. Recommended system architecture embedding the camera module MI1602, the thermal imaging processor MI48xx, and a host MCU.

6. FUNCTIONAL DESCRIPTION

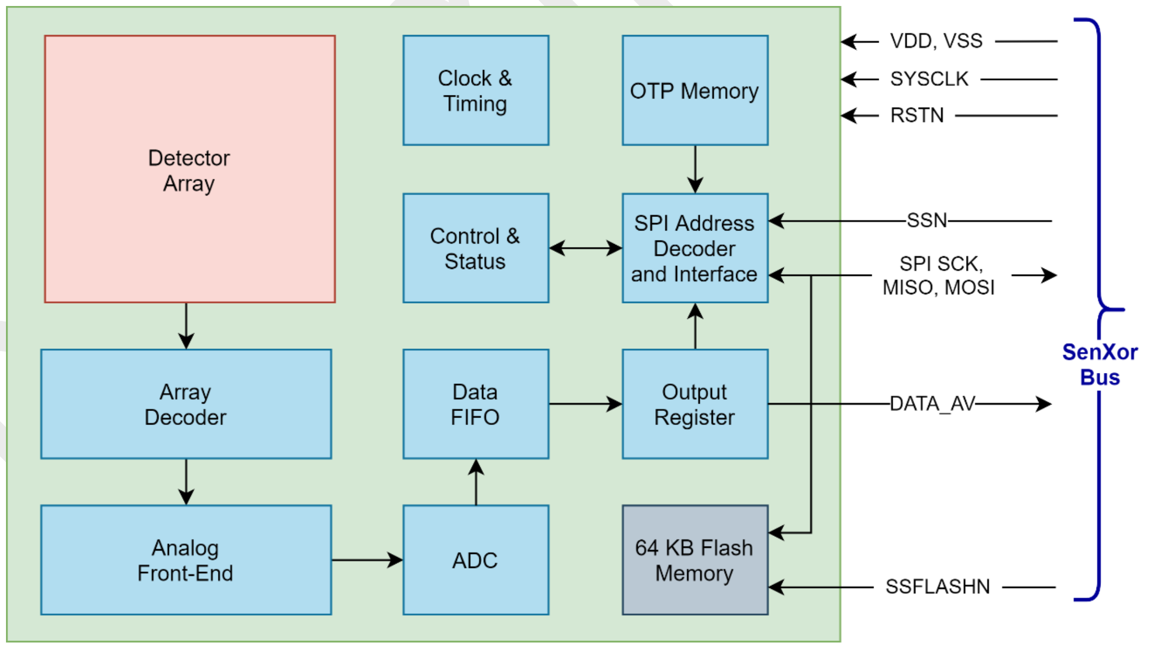


Fig. 3. Block diagram of the MI1602 camera module, showing major elements of the SenXor chip, the on-board flash memory and the SenXor Bus digital interface signals.

Table 3. Functional Blocks Description

Detector Array	An array of 160 x 120 LWIR detectors, each of which produces a voltage of magnitude that is dependent on the difference in temperature between the objects in the field of view and the die temperature.
Clocking and Timing Logic	System clock related circuitry, responsible for all timing and reset signalling supplied to the Array Decode Logic.
SPI Address Decoder	Address decoder for selecting the correct SPI slave device and registers of the MI1602 Camera Module. Two SPI select pins are supported. SSN enables access to the internal registers for control and status information, as well as to the output register through which the ADC data corresponding to each detector is acquired. SSFLASHN enables access to the 64 KB flash memory that is located on the PCB assembly.
Array Decode Logic	Row and column decode logic for the FPA, responsible for accessing each detector in sequence and routing its output via the Analogue Front End to the ADC.
Analogue Front End	Amplification and filtering the signals from the individual detectors so they are suitable for digitization by the ADC. This stage includes gain control for conditioning the analogue signal for digitization based on the scene temperature and frame rate.
ADC	Analogue to Digital Converter of the voltage signal from the Analogue Front End. Its output is buffered in the Output Register.
Data FIFO	The MI1602 implements a First-In-First-Out (FIFO) memory buffer so as to ease the timing on the readout of the output data from ADC.
Output Register	The output register stores the ADC data that can be read by the MI48xx chip or the host MCU through the SPI interface.
OTP Memory	Embedded OTP ROM of factory programmed unique device ID.
Flash Memory	Factory programmed FLASH memory storing the per-pixel calibration look-up tables that are necessary for temperature conversion and radiometric output by the host system.

7. Technical Specification

7.1. Thermal Imaging Sensor Characteristics

7.1.1. General

The thermal sensor array operates in the long-wave infrared range (LWIR) of the electromagnetic spectrum. Table 4 lists the essential characteristics of the sensor. Fig. 4

shows the spectral response of an individual detector within the array, including the characteristics of the lens of the camera module.

Table 4. THERMAL IMAGING SENSOR CHARACTERISTICS

Parameter	Value			Unit
Wavelength detection range	8 – 14			µm
Focal point array shape	160 (H) x 120 (V)			Number of detectors
Total number of detectors	19,200			Number of detectors
Non-functional detectors	200 pixels			
Detector pitch	35 (H) x 35 (V)			µm
Noise-equivalent temperature difference (NETD)	TBD (MI1602M5S) [1),] TBD (MI1602M6C) [2)]			mK
Indicative Scene Temperature (at ambient operational temperature)	Module Gain factor [3)]			
	1.0 (default)	0.5	0.25	
MI1602M6C	20 to 300°C	TBD	TBD	°C
MI1602M5S	20 to 250°C	TBD	TBD	°C
Operating temperature range	-20 to 85°C			°C
Storage temperature range	TBD			°C
Frame rate (maximum)	25			Frames per second
Power consumption (mean)	76			mW

Notes:

1) Defined at 1 FPS with the default denoising filter in the firmware of the companion thermal imaging processor by Meridian Innovation, see MI48xx specification.
2) Module gain is controlled via the companion thermal imaging processor MI48xx.

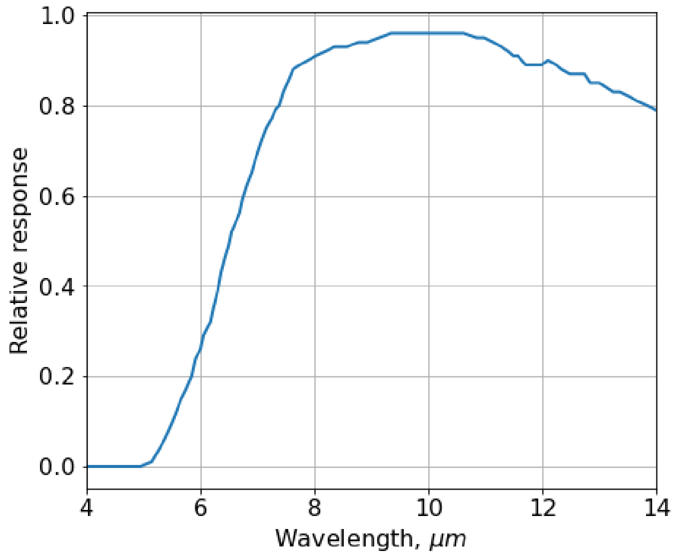
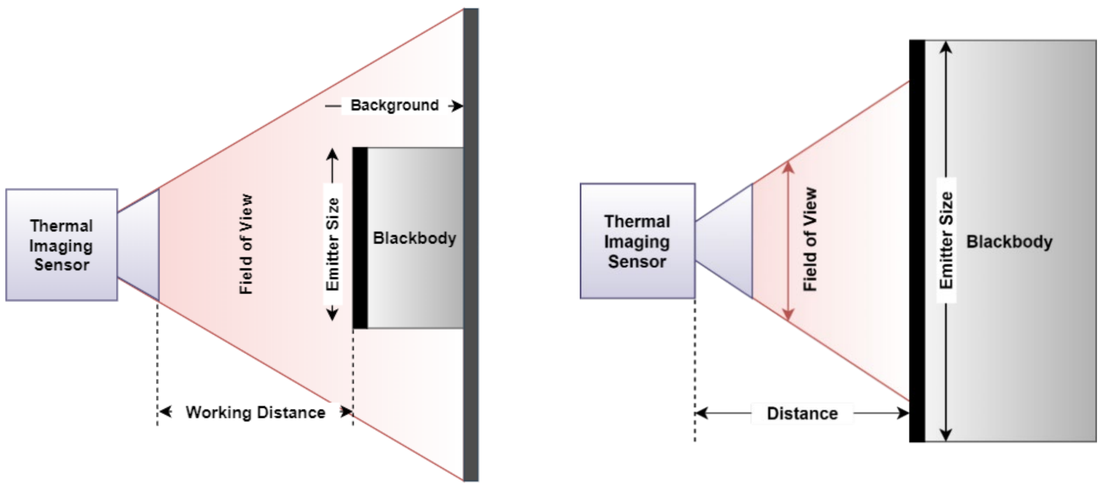


Fig. 4. Spectral response of MI1602M5S.

7.1.2. Accuracy

Accuracy is defined as the uncertainty of the mean value obtained from the center of a sufficiently large reference heat source under isothermal conditions for module and ambience, power supply voltage $V_{DD} = 3.3 \pm 0.01\ V$, relative humidity below 95 %, and no condensing vapor or moisture on the lens. The area of the reference heat source must cover a significant fraction of the FOV of the module, as shown in Fig. 5 a). Non-uniformity is defined as deviation of an individual pixel from the mean value of all pixels when the working distance is such that the emitter size exceeds the FOV of the module as in Fig 5 b).



a) b)

Fig. 5. Setup for module accuracy verification (a) and for module non-uniformity verification (b).

Table 5. ACCURACY SPECIFICATION FOR MI1602M5S

	Operational chip temperature [1], ℃	Scene temperature, ℃	Uncertainty, ℃
Frame Accuracy [2]	30	0 – 100	± 3.5 ℃**
	30	> 100	the bigger of ±5.0 or 5%**
	30	< 0	TBD
Non-uniformity [3]	30	0 – 100	±1℃**

Table 6. ACCURACY SPECIFICATION FOR MI1602M6C

	Operational chip temperature [1], ℃	Scene temperature, ℃	Uncertainty, ℃
Frame Accuracy [2]	30	0 – 100	± 3.5 ℃**
	30	< 0	the bigger of ±5.0 or 5%**
	30	> 100	TBD
Non-uniformity [3]	30	0 to +100	±1℃**

Notes:

1. SenXor chip temperature, measured internally by the chip itself.
2. Frame Accuracy is defined as the noise-free value obtained from the centre of a stationary uniform circular heat source of 12.5 cm diameter, placed 50cm away from the lens and occupying the center of the field of view.
3. Frame Accuracy is based on the center of the array, 60x60 pixel area for NFOV lens, 30x30 pixel area for WFOV lens
4. Pixel-to-pixel variation is defined as the deviation from the mean value obtained from irradiance by a uniform blackbody exceeding the FOV of the sensor.

7.2. Electrical Characteristics

7.2.1. Absolute Maximum Rating

Exceeding the values reported below at any time may lead to a performance deterioration, malfunction or destruction of the chip.

The values reported below are guaranteed by characterization results, not tested in production.

All interface-related pins are referred to as I/O.

Table 7. ABSOLUTE VOLTAGE RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}-V_{SS}	DC Power Supply	−0.3	3.6	V
V_{IN}	I/O voltage	−0.3	3.6	V
ESD(HBM)	ESD(HBM)		2	kV

ESD(CDM)	ESD(CDM)		0.5	kV

Table 8. ABSOLUTE CURRENT RATINGS

Symbol	Parameter	Min	Max	Unit
I_{DD}	Maximum Current into V_{DD}		200	mA
I_{SS}	Maximum Current out of V_{SS}		100	
I_{IO}	Maximum Current Sunk by a I/O pin		20	
	Maximum Current Sourced by a I/O pin		20	
	Maximum Current Sunk by total I/O pins		100	
	Maximum Current Sourced by total I/O pins		100	
LU	Static latch-up class (at T_A = 25°C)		200	

Table 9. ABSOLUTE ENVIRONMENTAL RATINGS

Symbol	Parameter	Min	Max	Unit
T_A	Ambient (Operating) Temperature	−20	85	°C
T_{ST}	Storage Temperature	−20	95	°C
P_A	Ambient Pressure		110	kPa
R_H	Relative Humidity		95	%
G_{SH}	Mechanical Shock		1	G

7.2.2. Nominal Operating DC Characteristics

Table 10. VOLTAGE CHARACTERISTICS

Symbol	Parameter	Min	Typical	Max	Unit
V_{DD}	Power Supply	3.2	3.3	3.4	V
V_{IO}	IO logic levels	3.0	3.3	3.6	V

Table 11. CURRENT CONSUMPTION 1)

Symbol	Parameter	Min	Typical	Max	Unit
I_{DD_A}	Active (thermal image acquisition)		23		mA
I_{DD_S}	Stand-by		2.5		mA

1) Measured at V_{DD} = 3.3 V and T_A = 25 °C.

7.3. Dynamic Timing Characteristics

7.3.1. System Clock

The MI1602 timing is driven by an external oscillator of 3 MHz, with a tolerance not exceeding 30 ppm. Internally, it generates all necessary timing for its operation and interfaces. Typically, SYSCLK will be generated by the companion chip MI48XX, which interfaces directly to the MI1602 via the SenXor bus.

7.3.2. System Reset

The MI1602 is reset by asserting 0 to the RSTN.

RSTN pin must be held low (below 0.2 V_{DD}) for at least 10 SYSCLK cycles in order to take effect, as shown in Fig. 10. When RSTN is asserted, there is no access to the SPI interface.

RSTN is considered released after the pin is held high (above 0.7 V_{DD}) for at least 10 SYSCLK µs. Thereafter, the SPI interface is accessible.

Immediately after power up the host MCU must assert and hold RST_N pin low for a minimum of 10 SYSCLK cycles. During this time the SYSCLK must be enabled and running. After this time the pin may be de-asserted, i.e. brought high for at least 10 SYSCLK cycles.

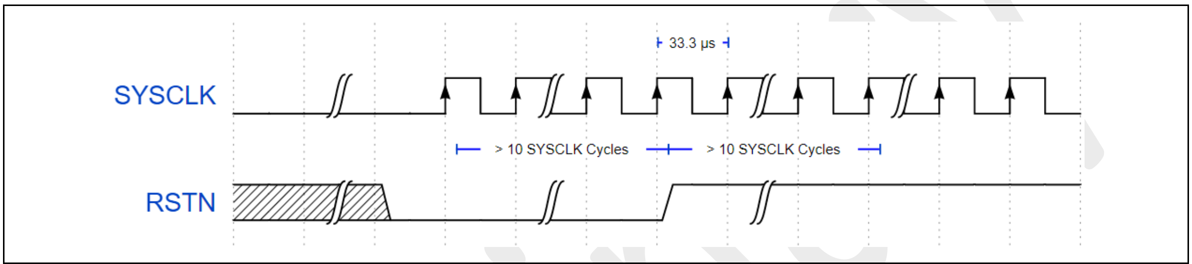


Fig. 6. Power-ON reset timing diagram and time before SPI interface access.

7.3.3. SPI Interface Timing for Register Access

ADC output data for each detector, as well as the control and status registers are accessed through the SPI interface as shown in the timing diagram in Fig. 7.

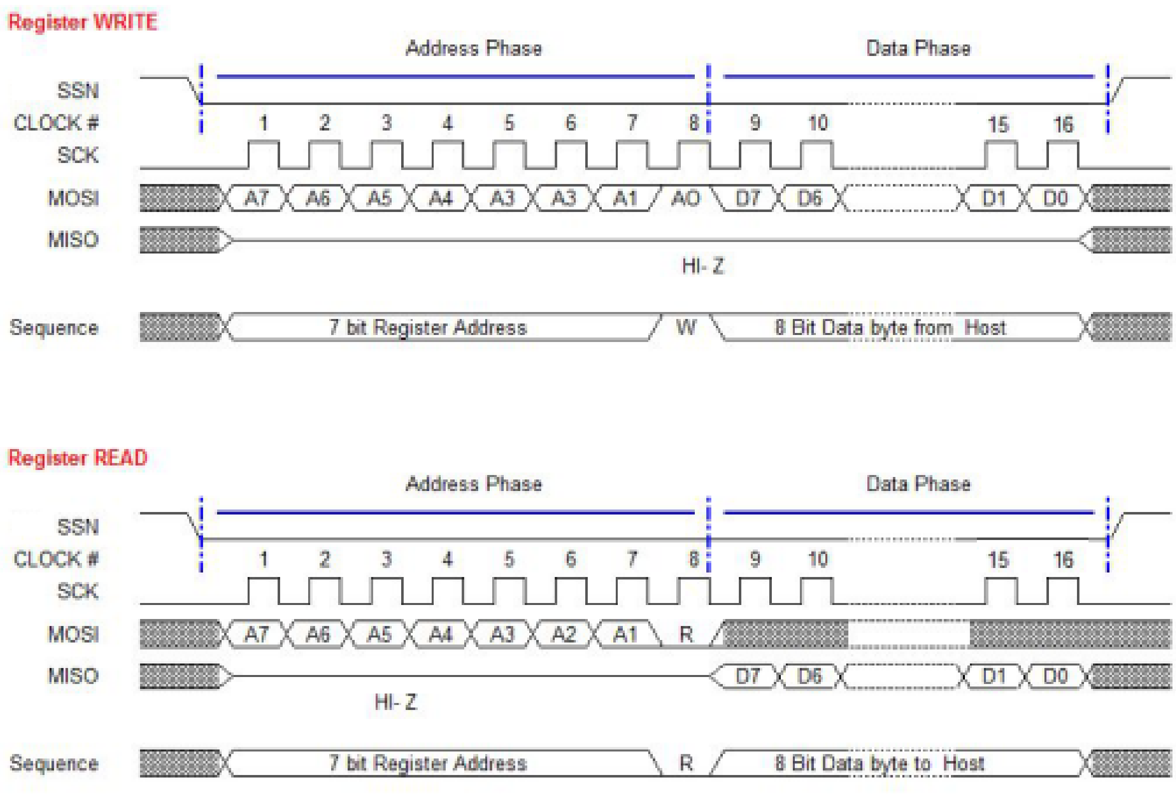


Fig. 7. SPI Timing diagram for write and read access.

7.3.4. Timing Characteristics

Table 12. TIMING PARAMETERS

Symbol	Parameter	Min	Typical	Max	Unit
F_{SYSCLK}	System clock frequency		3		MHz
F_{SCK}	SPI clock frequency	10	14	20	MHz
$Duty_{SCK}$	SPI clock duty cycle		50		%
T_{DS}	SPI data setup time	2			ns
T_{DH}	SPI data hold time	5			ns

8. PACKAGE INFORMATION

Fig. 8. shows the dimension details of the dimension of the MI1602M5S camera module.
Fig. 9 shows the dimension details of the dimension of the MI1602M6C camera module.
The weight of the entire assembly is less than 5 g.

The base of the MI1602Mxx is a reinforced flexible PCB with an integral extension for interfacing to an FPC connector with a pitch of 0.5 mm. A typical connector part number is HiRose FH28-10S-0.5SH from Hirose Electric. Further details of the correspondence between pin 1 on the MI1602Mxx and pin 1 on the FPC connector on the host system are given in Appendix A.

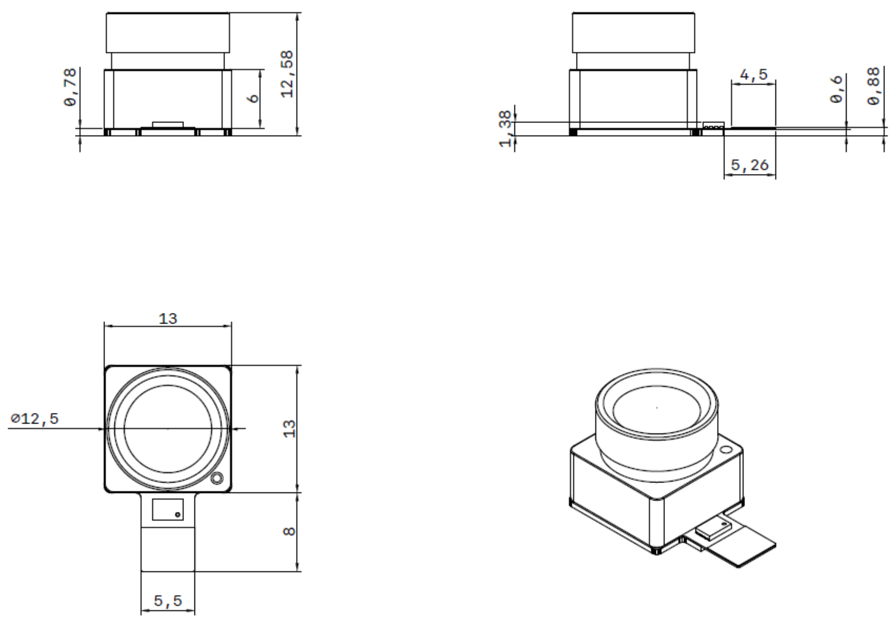


Fig. 8. Dimension of MI1602M5S. All dimensions are in mm, unless specified otherwise.

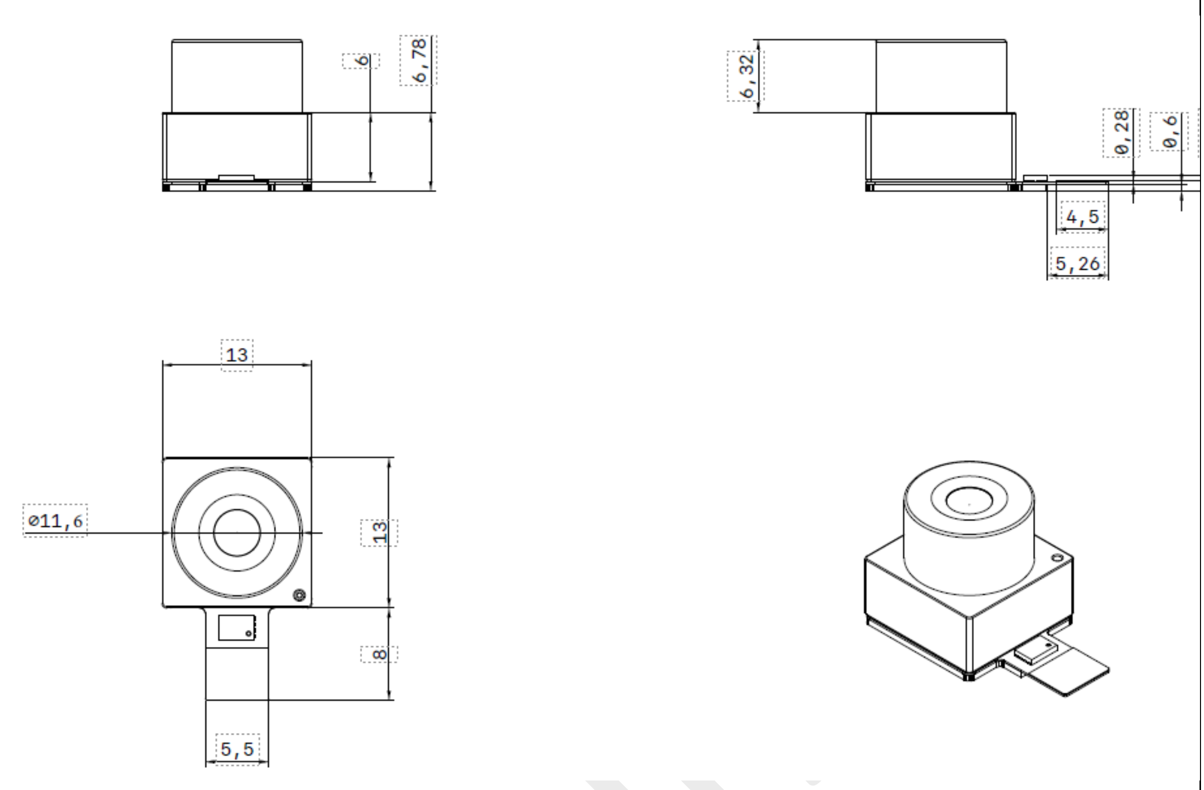


Fig. 9. Dimension of MI1602M6C. All dimensions are in mm, unless specified otherwise.

9. REVISION HISTORY

Revision	Date	Comment
1.0.1	18 Oct 2024	Template with preliminary information
1.0.2	20 Dec 2024	Add more information to document

10. Legal Information

This document is for informational purposes only

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11. Contacts Information

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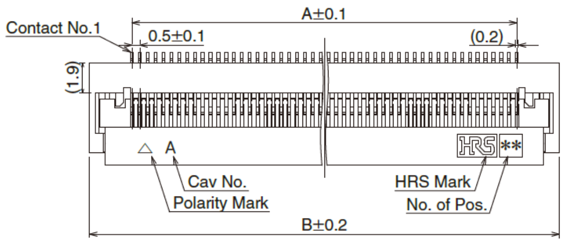
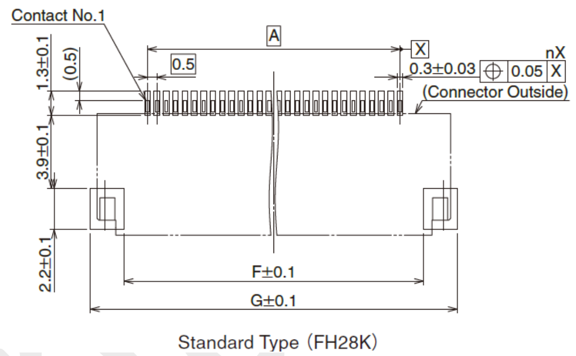
Company Registration Number: 201611173R

12. Appendix A – Interfacing to FPC Connector on the Host System

Figure 10-a) shows the schematic of the recommended HiRose FH28-10S-0.5SH FPC connector with 0.5 mm pitch. Note the polarisation mark, which indicates Pin 1 of the connector. This Pin 1 corresponds to Pin 1 of the FPC extension of the MI1602. Accordingly, the recommended PCB layout of the connector is shown Fig. 10-b).



a)



b)

Fig. 10. Polarisation mark and Pin 1 indicator on the recommended FPC connector for interfacing the MI1602Mxx, and example layout of the soldering pads for the FPC connector on the host system.

13. Appendix B – Array Orientation and Detector Enumeration

The MI1602 module outputs the data of each detector of the focal point array in a serial fashion. It is important to note the correct enumeration of the detectors, when constructing a two-dimensional image from the serial stream of data.

The MI1602 contains 19,200 detectors or pixels, arranged in 120 rows and 160 columns as shown in Fig. 11, assuming that you are facing the lens of the module. The value of pixel 1 is output first, and the value of pixel 19,200 is output last, in a row-by-row fashion.

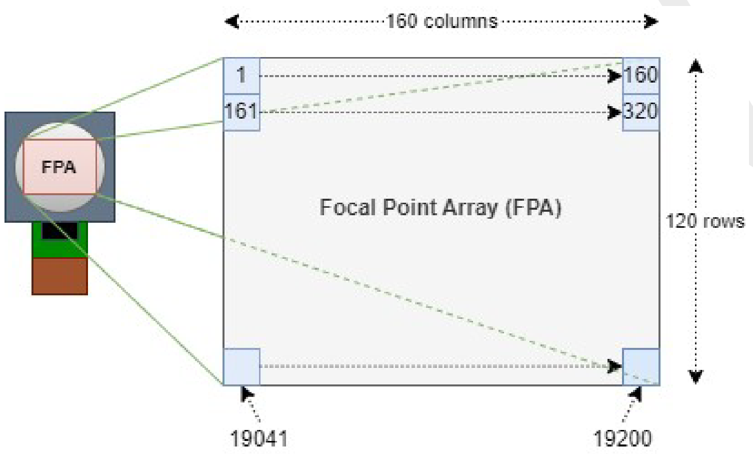


Fig. 11. When facing the lens of the MI1602 module, the individual detectors of the focal point array are enumerated as shown in the rectangular frame, from 1 to 19,200. The temperature values are output serially, starting from that of detector 1, ending with that of detector 19,200.