

# **SSD2677**

## ***Advanced information***

**960 Source x 680 Gate  
Active Matrix EPD Display Driver with Controller  
for color application**

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

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**SSD2677**

Rev 1.0

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**Appendix: Revision history**

<b>Version</b>	<b>Change Items</b>	<b>Effective Date</b>
Advance Information 1.0	Initial Release <ul style="list-style-type: none"><li>• Revised DC characteristics</li></ul>	28-Mar-2024

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## 1 General Description

The SSD2677 is an all-in-one AMEPD driver IC with Controller which can support EPD color application.

It consists of 960 source outputs, 680 gate outputs, 1 VCOM & 1 VBD which can support a maximum display resolution 960 x 680.

SSD2677 supports cascade function which can expand the panel resolution to maximum 1920 x 680. It also embeds oscillator, booster & regulators and selectable Serial Peripheral Interface (3-wire/4-wire) to communicate with general MCU.

## 2 Features

- Design for dot matrix type active matrix EPD display, support Black/White/Color.
- Power supply:
  - VDD: 2.3V to 3.6V
  - VDDIO: Connect to VDD
- On chip display RAM.
  - 2bit outputs per pixel to support Black/White/Color.
- Resolution: 680 gate outputs, 960 source outputs, 1VBD (for border) and 1 VCOM.
  - 680 output gate drivers:
    - 2-level outputs (VGH, VGL), Max 40Vp-p.
    - Gate driving output voltage (VGH/VGL): +/-20V, +/-17V, +/-15V.
    - Up and Down shift capability.
  - 960 output source drivers with 4 levels output for Black/White/Color per pixel:
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame):
      - Mode 0: 0V & VSH1 (+15V) & VSL (-15V) & VSH2 (+3V to +15V)
      - Mode 1: 0V & VSH1 (+3V to +15V) & VSL (-3V to -15V) & VSH2 (+3V to +15V)
    - Source driving output voltage (Voltage step: 200mV)
    - Left and Right shift capability.
  - 1 VBD for border level.
    - Same function as the programmable source driver with selected LUT.
    - 4 levels output (DCVCOM, VSH1, VSL and VSH2)
  - 1 VCOM for Common electrode level.
    - DCVCOM: -0.2V to -4V (Voltage step: 200mV)
    - ACVCOM: 4 levels output (DCVCOM, VSH1+DCVCOM, VSL+DCVCOM and floating)
    - Built in VCOM sensing.
- On-chip oscillator.
- Programmable output Waveform Settings.
- Support frame rate: 85Hz (max).
- External or internal generated voltage for burning OTP.
- Embedded 6k Bytes OTP to store the waveform settings and parameters.
- Support low voltage detect for supply voltage.
- Internal Temperature Sensor of +/-2degC accuracy from -25degC to 50degC, 7-bit status.
- MCU interface: Serial peripheral (3-wire/4-wire), Maximum SPI write speed 20MHz.
- Available in COG package.

### 3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD2677ZB	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 12um
SSD2677ZC	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um

### 4 Block Diagram

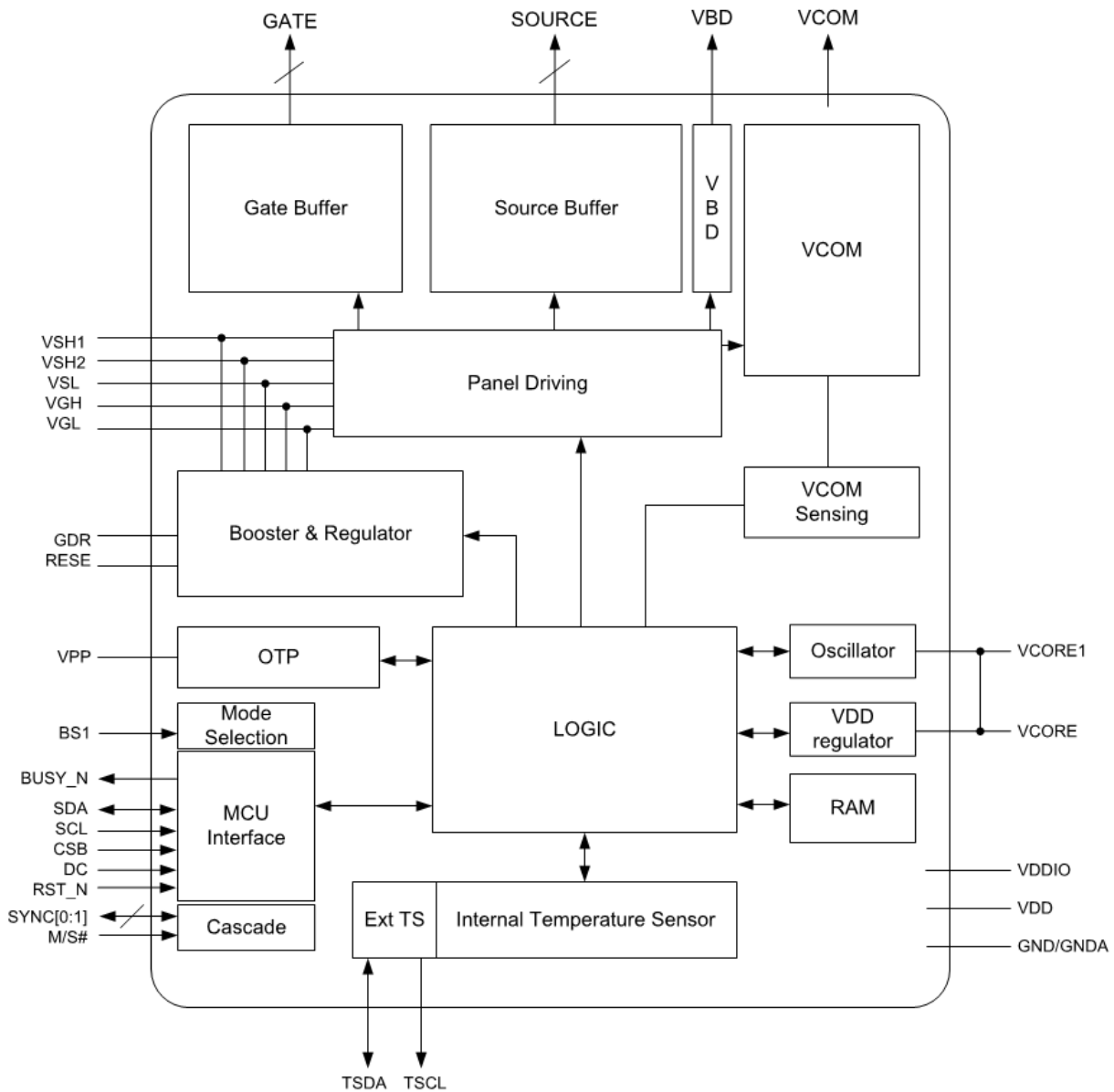


Figure 4-1 : SSD2677 Block Diagram

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## 5 PIN DESCRIPTION

**Key:** I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin  
 NC = Not Connected, Pull L =connect to GND, Pull H = connect to V<sub>DDIO</sub>

**Table 5-1: Power Supply Pins**

Name	Type	Connect to	Function	Description	When not in use
VDD	P	Power Supply	Power Supply	Power input pin for the chip.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the interface. - Connect to VDD in the application circuit.	-
VCORE	C	Capacitor	Logic Power	Core logic power pin. VCORE is regulated internally from VDD.	-
VCORE1	C	Capacitor	Logic Power	Core logic power pin1. - connect to VCORE in the application circuit.	-
GND	P	GND	GND	Ground	-
GND A	P	GND	GND	Ground - Connect to GND in the application circuit	-
VPP	P	Reserved	Reserved	Reserved Keep it floating.	-

**Table 5-2: Interface Logic Pins**

Name	Type	Connect to	Function	Description	When not in use						
BS1	I	VDDIO/GND	MCU Interface Mode Selection	This pin is for selecting 3-wire or 4-wire SPI bus. <table border="1" style="margin-left: 20px;"> <tr> <td>BS1</td> <td>MCU Interface</td> </tr> <tr> <td>0</td> <td>4-wire SPI</td> </tr> <tr> <td>1</td> <td>3-wire SPI(9 bits SPI)</td> </tr> </table>	BS1	MCU Interface	0	4-wire SPI	1	3-wire SPI(9 bits SPI)	-
BS1	MCU Interface										
0	4-wire SPI										
1	3-wire SPI(9 bits SPI)										
SCL	I	MPU	Data Bus	Serial clock pin for interface	-						
SDA	I/O	MPU	Data Bus	Serial data pin for interface	VDDIO or GND						
CSB	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU.	VDDIO or GND						
DC	I	MPU	Logic Control	This pin is Data/Command control pin connecting to the MCU.	VDDIO or GND						
RST_N	I	MPU	System Reset	This pin is reset signal input. Active Low.	-						
BUSY_N	O	MPU	Device Busy Signal	This pin indicates the driver status. L: Driver is busy H: non-busy. Host side can send command/data to driver.  In the cascade mode, the BUSY_N pin of the slave chip should be left open.	Open						

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Name	Type	Connect to	Function	Description	When not in use
M/S#	I	VDDIO/GND	Cascade Mode Selection	This pin is Master and Slave selection pin. - For the single chip application, the M/S# pin should be connected to VDDIO. - In the cascade mode: <ul style="list-style-type: none"> <li>For Master Chip, the M/S# pin should be connected to VDDIO.</li> <li>For Slave Chip, the M/S# pin should be connected to GND. The corresponding pins including TSDA, TSCL, SYNC[0:1], VCORE, VGH, VGL, VSH1, VSL, VSH2 VCOM must be connected to the master chip.</li> </ul>	-
SYNC[0:1]	I/O	Open	Cascading connection	Reserved for cascade application.	Open
TSDA	I/O	Temperature sensor SDA	Interface to Digital Temp. Sensor	This pin is I <sup>2</sup> C Interface to digital temperature sensor Data pin. External pull up resistor is required when connecting to I <sup>2</sup> C slave.	VSS
TSCL	O	Temperature sensor SCL	Interface to Digital Temp. Sensor	This pin is I <sup>2</sup> C Interface to digital temperature sensor Clock pin. External pull up resistor is required when connecting to I <sup>2</sup> C slave.	VSS

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**Table 5-3: Analog Pins**

Name	Type	Connect to	Function	Description	When not in use
GDR	O	MOSFET Driver	VGH, VGL Generation	This pin is N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		This pin is Current sense input pin for the control Loop.	-
VGH	C	Stabilizing capacitor		This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and GND in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and GND in the application circuit.	-
VSH1	C	Stabilizing capacitor	VSH1, VSH2, VSL Generation	This pin is Positive Source driving voltage, VSH1. Connect a stabilizing capacitor between VSH1 and GND in the application circuit.	-
VSH2	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH2. Connect a stabilizing capacitor between VSH2 and GND in the application circuit.	
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage, VSL. Connect a stabilizing capacitor between VSL and GND in the application circuit.	
VCOM	C	Panel & Stabilizing capacitor	VCOM driving signal	This pin is VCOM driving voltage, VCOM. Connect a stabilizing capacitor between VCOM and GND in the application circuit.	-

**Table 5-4: Driver Output Pins**

Name	Type	Connect to	Function	Description	When not in use
S [959:0]	O	Panel	Source driving signal	Source output pin.	Open
G [679:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	Border output pin.	Open

**Table 5-5: Other Pins**

Name	Type	Connect to	Function	Description	When not in use
TIN	I	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
TPE	O	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
CL	I/O	Open	Reserved	Reserved	Open
RSV	NC	NC	Reserved	This is a reserved pin and should be kept open.	Open
TPA, TPB, TPC, TPD, TPF, FB	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Do not connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPE, TPF, TIN and FB.	Open

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## 6 Functional Block Description

### 6.1 MCU Interface

#### 6.1.1 MCU Interface selection

The SSD2677 can support 3-wire/4-wire serial peripheral. In the SSD2677, the MCU interface is pin selectable by BS1 shown in Table 6-1.

Table 6-1 : Interface pins assignment under different MCU interface

MCU Interface	BS1	RST_N	CSB	DC	SCL	SDA
4-wire serial peripheral interface (SPI)	L	Required	CSB	DC	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	CSB	L	SCL	SDA

#### Note

(1) L is connected to GND and H is connected to  $V_{DDIO}$

#### 6.1.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C and CSB. The control pins status in 4-wire SPI in reading/writing command/data is shown in

Table 6-2. The read/write procedure of 4-wire SPI is shown in Figure 6-1.

Table 6-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	L	L
Read/Write data	↑	Data bit	H	L

#### Note:

- (1) L is connected to GND and H is connected to  $V_{DDIO}$
- (2) ↑ stands for rising edge of signal
- (3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C pin.

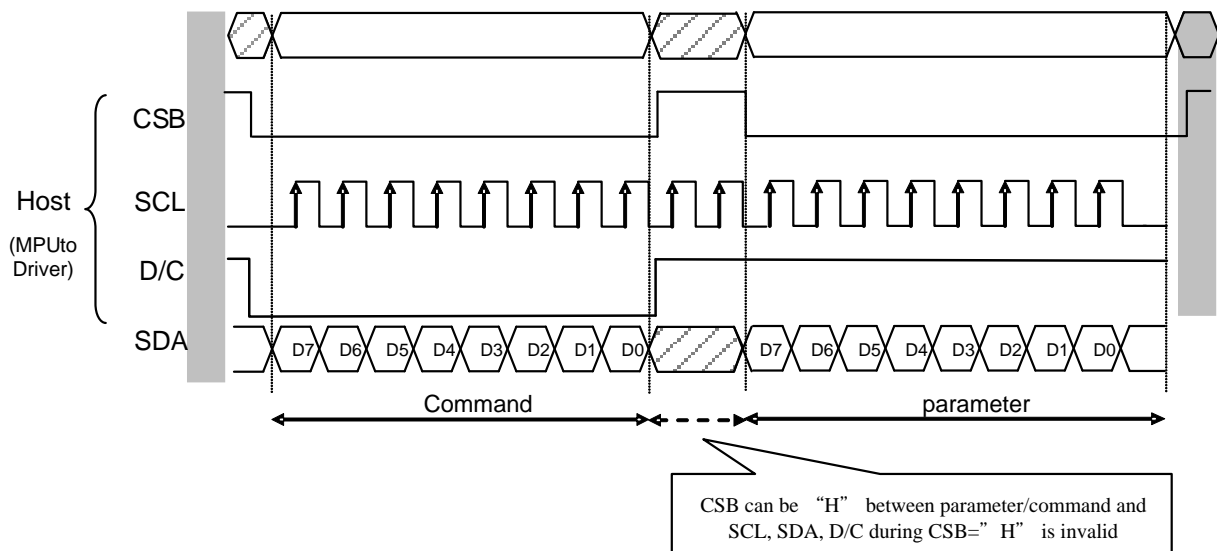


Figure 6-1 : Read/Write procedure in 4-wire SPI mode

### 6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CSB. The operation is similar to 4-wire SPI while D/C pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3. The read/write procedure of 3-wire SPI is shown in Figure 6-3.

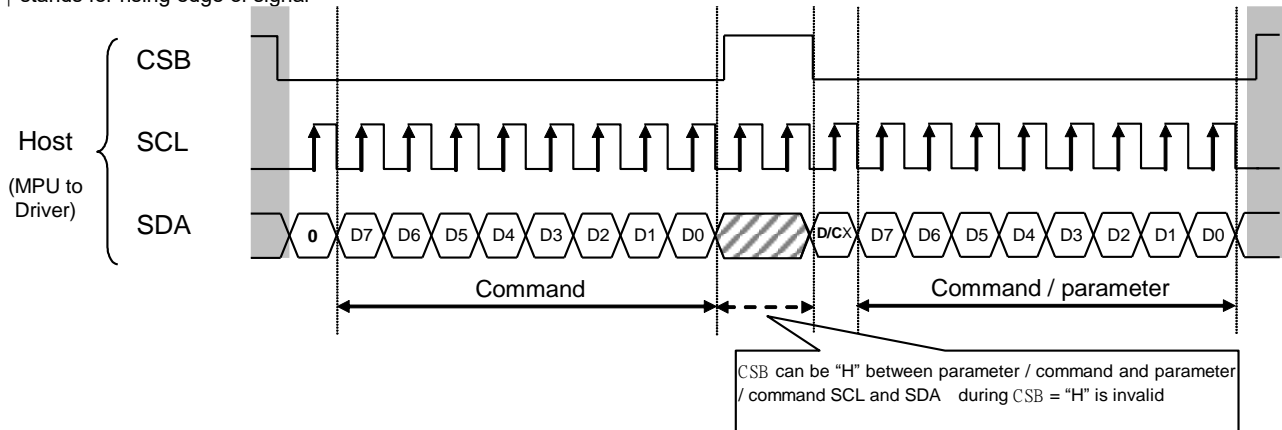
In the read/write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C bit, D7 bit, D6 bit to D0 bit. The first bit is D/C bit which determines the following byte is command or data. When D/C bit is 0, the following byte is command. When D/C bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

**Table 6-3 : Control pins status of 3-wire SPI**

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Read/Write data	↑	Data bit	Tie LOW	L

**Note:**

- (1) L is connected to GND and H is connected to V<sub>DDIO</sub>
- (2) ↑ stands for rising edge of signal



**Figure 6-2 : Read/Write procedure in 3-wire SPI mode**

### 6.2 RAM

The On-chip display RAM is holding the image data. 2bpp for 960x680 resolution

### 6.3 Internal Temperature Sensor

The internal temperature sensor can be selected by command register. The accuracy of it is ±2degC from -25degC to 50degC.

### 6.4 Oscillator

The oscillator module generates the clock reference for waveform timing and analog operations.

### 6.5 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH1, VSH2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.

### 6.6 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into OTP. It required PON with DCVCOM mode for analog voltage ready.

The typical flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Source are GND.
- VCOM pin is used for sensing.
- During Sensing period, BUSY\_N is kept flagged.
- After Sensing, Active Gate return to non-select stage.

## 6.7 External Temperature Sensor I2C Single Master Interface

The chip provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing.

TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor.

- 1) If the Temperature value MSB bit D7 = 0, then the temperature is positive and value (DegC) = + (Temperature value)
- 2) If the Temperature value MSB bit D7 = 1, then the temperature is negative and value (DegC) = - (2's complement of Temperature value)

Hex value	Binary value	2's complement	Temperature (DegC)
0xE7	1110 0111	-(0011001)	-25
...	...	...	...
0xFD	1111 1101	-(000 0011)	-3
0xFE	1111 1110	-(000 0010)	-2
0xFF	1111 1111	-(000 0001)	-1
0x00	0000 0000	0000 0000	0
0x01	0000 0001	0000 0001	1
0x02	0000 0010	0000 0010	2
0x03	0000 0011	0000 0011	3
...	...	...	...
0x19	0001 1001	0001 1001	25
0x32	0011 0010	0011 0010	50

## 6.8 Cascade Mode

The SSD2677 has a cascade mode that can cascade 2 chips to achieve the higher display resolution. The pin M/S# is used to configure the chip. When M/S# is connected to VDDIO, the chip is configured as a master chip. When M/S# is connected to GND, the chip is configured as a slave chip.

When the chip is configured as a master chip, it will be the same as a single chip application, ie, all circuit blocks will be worked as usual. When the chip is configured as a slave chip, its booster and regulator circuit will be disabled. The booster voltages will come from the master chip. Therefore, the corresponding pins including TSDA, TSCL, SYNC[0:1], VCORE, VGH, VGL, VSH1, VSL, VSH2 and VCOM must be connected to the master chip.

# 7 COMMAND TABLE

## 7.1 User Command Table

Table 7-1: Summary of user command table

R/W#	DC	Code	Command	D7	D6	D5	D4	D3	D2	D1	D0	POR	
W	0	00h	PSR Panel Setting Register	0	0	0	0	0	0	0	0		
W	1			RES[1:0]		B mode		0	UD	SHL	SHD N	RST N	2Fh
W	1			LUT_EN	FOPT[1:0]		VCMZ	TS_AUTO	TIEG	NORG	VC.LUTZ		09h
W	0	01h	PWR Power setting Register	0	0	0	0	0	VSC_EN	VS_EN	VG_EN	07h	
W	1			1	1	1	1	0	VGPN[1:0]			F0h	
W	1			VSP[6:0]									00h
W	1			VSNL[6:0]									00h
W	1			VSP2[6:0]									00h
W	1			VSNL2[6:0]									00h
W	0			02h	POF Power OFF Command Register	0	0	0	0	0	0	1	0
W	1	03h	POFS Power off Sequence Setting	00h				0	0	1	1		-
W	0			T_VDPG_OFF[1:0]	0	T_VDS_OFF[1:0]						00h	
W	0	04h	PON Power ON Command Register	0	0	0	0	0	1	0	0		
W	1			0	0	0	0	1	1	0			
W	0	06h	BTST Booster Soft Start Setting Register	0		VGHSSC_ONT[2:0]		T_VGHSSA[1:0]		T_VGHSSB[1:0]		0Fh	
W	1			1	VGHSSA_DRV[2:0]		VGHSSA_OFFT[3:0]					8Bh	
W	1			1	VGHSSB_DRV[2:0]		VGHSSB_OFFT[3:0]					93h	
W	1			1	VGHSSC_DRV[2:0]		VGHSSC_OFFT[3:0]					A3h	
W	0	07h	DSLIP Deep Sleep Register	0	0	0	0	0	1	1	1		
W	1			A5h									-
W	0			0	0	0	1	0	0	0	0		
W	1	10h	DTM Data Start transmission Register	KPixel1[1:0]		KPixel2[1:0]		KPixel3[1:0]		KPixel4[1:0]		-	
W	1			Kpixel(4M-3)[1:0]		Kpixel(4M-2)[1:0]		Kpixel(4M-1)[1:0]		Kpixel(4M)[1:0]		-	
W	1			0		0		1		0		1	0
W	0			00h									-
W	0	12h	DRF Display Refresh Command Register	00h									
W	1			A5h or A7h									
W	0	17h	AUTO Auto Sequence Register	0	0	0	1	0	1	1	1		
W	1			0	0	0	0	0	0	0	0	0	
W	0			0	1	0	0	0	0	0	0	0	
W	0	30h	PLL Frame Rate Control register	0	0	1	1	0	0	0	0		
W	1			0	0	0	0	0	0	FR[2:0]		02h	
W	0			0	1	0	0	0	0	0	0	0	
R	1	40h	TSE Temperature Sensor Command Register	TS[7:0]									
W	0			0	1	0	0	0	0	0	0	1	
W	1	41h	TSE Temperature Sensor Enable Register	TSE	0	0	0	TO[3:1]				0	
W	0			0	1	0	0	0	0	1	0		
W	1			WATTR[7:0]									00h
W	1	42h	TSW Temperature Sensor Write Register	WMSB[7:0]									00h
W	1			WLSB[7:0]									00h
W	0			0	1	0	0	0	0	0	1	1	
R	1	43h	TSR Temperature Sensor Read Register	RMSB[7:0]									
W	0			0	1	0	1	0	0	0	0	0	
W	1	50h	VCOM and DATA interval setting Register	VBD[2:0]		DDX		CDI[3:0]				97h	
W	0			0	1	0	0	0	0	0	0	1	
R	1	51h	LPD Lower Power Detection Register	0	0	0	0	0	0	0	LPDstatus		
W	0			0	1	1	0	0	0	0	1		
W	1			0	0	0	0	0	0	HRES[9]	HRES[8]		03h
W	1	61h	TRES Resolution setting Register	HRES[7:0]									C0h
W	1			0	0	0	0	0	0	VRES[9]	VRES[8]		02h
W	1			VRES[7:0]									A8h
W	0			0	1	1	0	0	0	1	0	1	
W	1	65h	GSST Gate/Source Start Setting Register	0	0	0	0	0	0	S_start[9]	S_start[8]		00h
W	1			S_start[7:0]									00h
W	1			0	0	0	0	0	0	G_start[9]	G_start[8]		00h
W	1			G_start[7:0]									00h

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R/W#	DC	Code	Command	D7	D6	D5	D4	D3	D2	D1	D0	POR		
W	0	70h	REV Chip Revision Register	0	1	1	1	0	0	0	0			
R	1			A[7:0]								07h		
R	1			B[7:0]								01h		
R	1			C[7:0]								01h		
W	0	80h	AMV Auto Measurement VCOM Register	1	0	0	0	0	0	0	0			
W	1			P[1:0]		AMVT[1:0]		AMVX	AMVS	0	AMVE	00h		
W	0	81h	VV VCOM Value Register	1	0	0	0	0	0	0	1			
R	1			VV[5:0]								-		
W	0	82h	VDCS VCM_DC Setting Register	1	0	0	0	0	0	1	0			
W	1			OTP_VCM		VDCS[6:0]						00h		
W	0	83h	PTLW Partial Window	1	0	0	0	0	0	1	1			
W	1			0		0		0		HRST[7:0]		HRST[9]	HRST[8]	00h
W	1			0		0		0		HRED[7:0]		HRED[9]	HRED[8]	03h
W	1			0		0		0		VRST[7:0]		VRST[9]	VRST[8]	00h
W	1			0		0		0		VRED[7:0]		VRED[9]	VRED[8]	00h
W	1			0		0		0		VRED[7:0]		#	PMODE	A7h
W	1			0		0		0		0		0	0	00h
W	0			90h	PGM Program Mode	1	0	0	1	0	0	0	0	
W	0			91h	APG Active Program	1	0	0	1	0	0	0	1	
W	0			92h	ROTP Read OTP Data	dummy byte								-
R	1	Address 0 in OTP								-				
R	1	...								-				
R	1	Address n in OTP								-				
W	0	E0h	CCSET External TS input selection Cascade enable	1	1	1	0	0	0	0	0			
W	1			0		0		0		TSFIX		CCEIN	00h	
W	0	E3h	PWS Power Saving Register	1	1	1	0	0	0	1	1			
W	1			VCOM_W[3:0]			SD_W[3:0]						65h	
W	0	E4h	LVSEL LVD Voltage Select Register	1	1	1	0	0	1	0	0			
W	1			LVD_SEL[1:0]								03h		
W	0	E6h	TS_SET Temperature sensor override	1	1	1	0	0	0	1	1			
W	1			TS_SET[7:0]								00h		

**Note:**

- (1) The bit which has been written as "0" or "1" in Table 7-1 must be followed. Otherwise, device malfunction may occur.
- (2) The driver IC will not response to all read & write commands during BUSY\_N=0.
- (3) Commands are only effective while all corresponding parameters for that command were written completely.
- (4) Commands or parameters not shown on above table are for "Reserve" usage.
- (5) POR value may be changed without notice.

## 8 Command Table Description

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0] = 2Fh [POR] B[7:0] = 09h [POR]
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	0	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		<p>A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: 960 x 680 (Default) 01b: 960 x 672 10b: 960 x 640 11b: 880 x 528</p> <p>*Remark: Inactive Gate outputs will be VGL for DRF and AMV. Inactive Source outputs will follow VCOM LUT output for DRF</p> <p>A[5] ~ B_mode Blanking Mode for voltage switching, the duration setting follow CDI. 0: Mode A Blanking time only for ACVCOM. 1: Mode B (Default) Blanking time for ACVCOM or switch mode of source power.</p> <p>A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 ... G0 1: Scan up. (Default) First line to Last line: G0 ... Gn-1</p> <p>A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 ... S0 1: Shift right. (Default) First data to Last data: S0 ... Sn-1</p> <p>A[1] ~ SHD_N Booster and Regulator Switch: 0: PON / POF command will not execute 1: PON / POF command will execute (Default)</p> <p>A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N signal will become "0" until Soft reset is finished.</p>
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		B[7] ~ LUT_EN

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
												<p>0: During reset, auto load LUT from OTP if it is valid. When PON/DRF, analog setting will follow the content of OTP. (Default)</p> <p>1: During reset, no action to load LUT from OTP. When PON/DRF, analog setting will follow the content of MCU</p> <p>B[6:5] ~ FOPT[1:0] FOPT function 00b: NO effect. Scan 1 frame after waveform finished (Default) 01b: Will scan 1 frame same as last output (of LUT) after waveform finished. 10b: Will scan 1 frame with Floating output after waveform finished. 11b: No Scan after waveform finished (Power off floating)</p> <p>B[4] ~ VCMZ VCOM Hi-Z option 0: NO effect. (default) 1: VCOM is always floating.</p> <p>B[3] ~ TS_AUTO Temperature Sensor auto option 0: NO effect. 1: Before loading OTP, Temperature Sensor will be activated automatically one time. (default)</p> <p>B[2] ~ TIEG VGL power off option 0: NO effect. (default) 1: After power off booster, VGL will be tied to GND.</p> <p>B[1] ~ NORG VCOM display end GND option 0: NO effect. (default) 1: After refreshing display, VCOM is tied to GND before power off</p> <p>B[0] ~ VC_LUTZ VCOM display end floating option 0: NO effect. 1: After refreshing display, the output of VCOM is set to floating automatically (default)</p>

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																		
0	0	01	0	0	0	0	0	0	0	1	PWR	Power setting Register A[5:0] = 07h [POR] B[7:0] = F0h [POR] C[6:0] = 00h [POR] D[6:0] = 00h [POR] E[6:0] = 00h [POR] F[6:0] = 00h [POR]																		
0	1		0	0	0	0	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		A[2] ~ VSC_EN Source LV power selection: 0: External source power for VSH2 pin. 1: Internal DCDC function for generate source power. (default) A[1] ~ VS_EN Source LV power selection: 0: External source power for VSH1 and VSL pin. 1: Internal DCDC function for generate source power. (default) A[0] ~ VG_EN Gate power selection: 0: External gate power for VGH and VGL pin. 1: Internal DCDC function for generate gate power. (default)																		
0	1		1	1	1	1	0	0	B <sub>1</sub>	B <sub>0</sub>		B[1:0] ~ VGPN [1:0] Internal VGH / VGL Voltage Level Selection: <table border="1"> <thead> <tr> <th>VGPN [1:0]</th> <th>Gate Voltage Level</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>VGH=20V, VGL=-20V (Default) VSH1=15V, VSL=-15V</td> </tr> <tr> <td>01</td> <td>VGH=17V, VGL=-17V VSH1=15V, VSL=-15V</td> </tr> <tr> <td>10</td> <td>VGH=15V, VGL=-15V VSH1=13V, VSL=-13V</td> </tr> <tr> <td>11</td> <td>Reserved.</td> </tr> </tbody> </table>	VGPN [1:0]	Gate Voltage Level	00	VGH=20V, VGL=-20V (Default) VSH1=15V, VSL=-15V	01	VGH=17V, VGL=-17V VSH1=15V, VSL=-15V	10	VGH=15V, VGL=-15V VSH1=13V, VSL=-13V	11	Reserved.								
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0	1		0	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		C[6:0] ~ VSPL [6:0] Internal Source Voltage Level Selection for VSH2@Mode0: <table border="1"> <thead> <tr> <th>VSPL[6:0]</th> <th>Voltage Level</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>3.0V (default)</td> </tr> <tr> <td>02h</td> <td>3.2V</td> </tr> <tr> <td>04h</td> <td>3.4V</td> </tr> <tr> <td>06h</td> <td>3.6V</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>76h</td> <td>14.8V</td> </tr> <tr> <td>78h</td> <td>15.0V</td> </tr> <tr> <td>Other</td> <td>Reserved</td> </tr> </tbody> </table>	VSPL[6:0]	Voltage Level	00h	3.0V (default)	02h	3.2V	04h	3.4V	06h	3.6V	:	:	76h	14.8V	78h	15.0V	Other	Reserved
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Other	Reserved																													
0	1		0	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		D[6:0] ~ VSNL[6:0] Internal Source Voltage Level Selection for VSL@Mode1: <table border="1"> <thead> <tr> <th>VSNL[6:0]</th> <th>Voltage Level</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>-3.0V (default)</td> </tr> <tr> <td>02h</td> <td>-3.2V</td> </tr> <tr> <td>04h</td> <td>-3.4V</td> </tr> <tr> <td>06h</td> <td>-3.6V</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>76h</td> <td>-14.8V</td> </tr> <tr> <td>78h</td> <td>-15.0V</td> </tr> <tr> <td>Other</td> <td>Reserved</td> </tr> </tbody> </table>	VSNL[6:0]	Voltage Level	00h	-3.0V (default)	02h	-3.2V	04h	-3.4V	06h	-3.6V	:	:	76h	-14.8V	78h	-15.0V	Other	Reserved
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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																		
0	1		0	E <sub>6</sub>	E <sub>5</sub>	E <sub>4</sub>	E <sub>3</sub>	E <sub>2</sub>	E <sub>1</sub>	E <sub>0</sub>		E[6:0] ~ VSPL2[6:0] Internal Source Voltage Level Selection for VSH1@Mode1: <table border="1"> <thead> <tr> <th>VSPL2[6:0]</th> <th>Voltage Level</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>3.0V (default)</td> </tr> <tr> <td>02h</td> <td>3.2V</td> </tr> <tr> <td>04h</td> <td>3.4V</td> </tr> <tr> <td>06h</td> <td>3.6V</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>76h</td> <td>14.8V</td> </tr> <tr> <td>78h</td> <td>15.0V</td> </tr> <tr> <td>Other</td> <td>Reserved</td> </tr> </tbody> </table>	VSPL2[6:0]	Voltage Level	00h	3.0V (default)	02h	3.2V	04h	3.4V	06h	3.6V	:	:	76h	14.8V	78h	15.0V	Other	Reserved
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0	1		0	F <sub>6</sub>	F <sub>5</sub>	F <sub>4</sub>	F <sub>3</sub>	F <sub>2</sub>	F <sub>1</sub>	F <sub>0</sub>		F[6:0] ~ VSNL2[6:0] Internal Source Voltage Level Selection for VSH2@Mode1: <table border="1"> <thead> <tr> <th>VSNL2[6:0]</th> <th>Voltage Level</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>3.0V (default)</td> </tr> <tr> <td>02h</td> <td>3.2V</td> </tr> <tr> <td>04h</td> <td>3.4V</td> </tr> <tr> <td>06h</td> <td>3.6V</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>76h</td> <td>14.8V</td> </tr> <tr> <td>78h</td> <td>15.0V</td> </tr> <tr> <td>Other</td> <td>Reserved</td> </tr> </tbody> </table>	VSNL2[6:0]	Voltage Level	00h	3.0V (default)	02h	3.2V	04h	3.4V	06h	3.6V	:	:	76h	14.8V	78h	15.0V	Other	Reserved
VSNL2[6:0]	Voltage Level																													
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0	0	02	0	0	0	0	0	0	1	0	POF	Power OFF Command Register																		
0	1		0	0	0	0	0	0	0	0		After power off command, driver will power off based on the Power OFF Sequence. BUSY_N will output low during operation. The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. *Remark: POF works at PON only																		
0	0	03	0	0	0	0	0	0	1	1	POFS	Power on/off Sequence Setting Register A[7:0] = 00h [POR]																		
0	1		0	0	A <sub>5</sub>	A <sub>4</sub>	0	0	A <sub>1</sub>	A <sub>0</sub>		A[5:4] ~ T_VDPG_OFF[1:0] Power off delay from VGL to VGH 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b: 80ms  A[1:0] ~ T_VDS_OFF[1:0] Power off delay from VSHX/VSL to VGH 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b : 80ms																		

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																																		
0	0	04	0	0	0	0	0	1	0	0	PON	<p>Power ON Command Register</p> <p>After the Power ON command, driver will power on based on the Power ON Sequence.</p> <p>BUSY_N will output low during operation.</p> <p>* Remark: PON Include booster on, VSH1/VSH2/VSL regulator on With default BTST, timing is &gt;80ms</p>																																																																		
0	0	06	0	0	0	0	0	1	1	0	BTST	<p>VGH Booster Soft Start Setting Register (for VGH)</p> <p>A[6:0] = 0Fh [POR] B[6:0] = 8Bh [POR] C[6:0] = 93h [POR] D[6:0] = A3h [POR]</p>																																																																		
0	1		0	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		A[6:4] ~ VGHSSC_ONT [2:0]																																																																		
0	1		1	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		VGH booster maximum MOSFET ON time (reserved)																																																																		
0	1		1	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		A[6:4] = 000 (Default)																																																																		
0	1		1	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		<p>A[3:2] ~ T_VGHSSA [1:0] = 11 (Default) VGH booster soft start Phase A duration A[1:0] ~ T_VGHSSB [1:0] = 11 (Default) VGH booster soft start Phase B duration</p> <table border="1"> <thead> <tr> <th colspan="2">Soft Start Phase Period (ms)</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>10</td> </tr> <tr> <td>01</td> <td>20</td> </tr> <tr> <td>10</td> <td>30</td> </tr> <tr> <td>11</td> <td>40</td> </tr> </tbody> </table> <p>B[6:4] ~ VGHSSA_DRV [2:0], = 000 (Default) VGH Phase A Driving Strength C[6:4] ~ VGHSSB_DRV [2:0], = 001 (Default) VGH Phase B Driving Strength D[6:4] ~ VGHSSC_DRV [2:0] = 010 (Default) VGH Phase C Driving Strength</p> <table border="1"> <thead> <tr> <th colspan="4">Driving Strength</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0</td> <td>100</td> <td>(reserved)</td> </tr> <tr> <td>001</td> <td>1</td> <td>101</td> <td>(reserved)</td> </tr> <tr> <td>010</td> <td>2</td> <td>110</td> <td>(reserved)</td> </tr> <tr> <td>011</td> <td>3(strongest)</td> <td>111</td> <td>(reserved)</td> </tr> </tbody> </table> <p>B[3:0] ~ VGHSSA_OFFT [3:0], = 1011 (Default) VGH Phase A Minimum OFF Time C[3:0] ~ VGHSSB_OFFT [3:0], = 0011 (Default) VGH Phase B Minimum OFF Time D[3:0] ~ VGHSSC_OFFT [3:0], = 0011 (Default) VGH Phase C Minimum OFF Time</p> <table border="1"> <thead> <tr> <th colspan="4">Minimum OFF Time (setting)</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>OFFH0</td> <td>1000</td> <td>OFFH8</td> </tr> <tr> <td>0001</td> <td>OFFH1</td> <td>1001</td> <td>OFFH9</td> </tr> <tr> <td>0010</td> <td>OFFH2</td> <td>1010</td> <td>OFFHA</td> </tr> <tr> <td>0011</td> <td>OFFH3</td> <td>1011</td> <td>OFFHB</td> </tr> <tr> <td>0100</td> <td>OFFH4</td> <td>1100</td> <td>OFFHC</td> </tr> <tr> <td>0101</td> <td>OFFH5</td> <td>1101</td> <td>OFFHD</td> </tr> <tr> <td>0110</td> <td>OFFH6</td> <td>1110</td> <td>OFFHE</td> </tr> <tr> <td>0111</td> <td>OFFH7</td> <td>1111</td> <td>OFFHF</td> </tr> </tbody> </table>	Soft Start Phase Period (ms)		00	10	01	20	10	30	11	40	Driving Strength				000	0	100	(reserved)	001	1	101	(reserved)	010	2	110	(reserved)	011	3(strongest)	111	(reserved)	Minimum OFF Time (setting)				0000	OFFH0	1000	OFFH8	0001	OFFH1	1001	OFFH9	0010	OFFH2	1010	OFFHA	0011	OFFH3	1011	OFFHB	0100	OFFH4	1100	OFFHC	0101	OFFH5	1101	OFFHD	0110	OFFH6	1110	OFFHE	0111	OFFH7	1111	OFFHF
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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	
0	0	07	0	0	0	0	0	1	1	1	DSLSP	Deep Sleep Register	
0	1		1	0	1	0	0	1	0	1		This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion. The only one parameter is a check code, the command would be executed if check code is A5h.	
0	0	10	0	0	0	1	0	0	0	0	DTM	Data Start transmission Register	
			2 bit per pixel									This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.	
0	1		KPixel1 [1:0]	KPixel2 [1:0]	KPixel3 [1:0]	KPixel4 [1:0]							
:			...										
0	1		KPixel (4M-3) [1:0]	KPixel (4M-2) [1:0]	KPixel (4M-1) [1:0]	KPixel (4M) [1:0]						KPixel[1:0] Source Driver Output	
												DDX=1 (Default)	DDX=0
											00b	Gray 0	Gray 3
											01b	Gray 1	Gray 2
											10b	Gray 2	Gray 1
											11b	Gray 3	Gray 0
												After issue this command, the host must send at least 1 byte data to the device.	
0	0	12	0	0	0	1	0	0	1	0	DRF	Display Refresh Command Register	
0	1		0	0	0	0	0	0	0	0		After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. BUSY_N will output low during operation.	
0	0	17	0	0	0	1	0	1	1	1	AUTO	Auto Sequence Register	
0	1		A7	A6	A5	A4	A3	A2	A1	A0		This command makes the chip enter the auto sequence Single-chip application ONLY. Auto Sequence Option 0xA5: Start Auto Sequence (PON > DRF > POF) 0xA7: Start Auto Sequence (PON > DRF > POF > DSLSP). Others: No effect BUSY_N signal will become "0" until Auto Sequence is finished.	
0	0	30	0	0	1	1	0	0	0	0	PLL	Frame Rate Control register The command controls the clock frequency. A[3:0] = 2h [POR]	
0	1		0	0	0	0	0	A2	A1	A0		A[3]: Dynamic Frame Rate 0: Disable (Default) 1: Enable A[2:0] ~ FR[2:0] It supports the following frame rates. Frame Rate Selection, Frame rate for Gate/Source switching that exclude the blanking time defined in CDI.	
												FR[2:0]	Frame Rate Selection
											000	12.5Hz	
											001	25Hz	
											010	50Hz (Default)	
											011	65Hz	
											100	75Hz	
											101	85Hz	

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																									
0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register																																																									
1	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		<p>This command enables internal temperature sensor. BUSY_N will output low during operation. Then the temperature value can be read in 1degC step A[7:0] ~ TS [7:0]</p> <table border="1"> <thead> <tr> <th>TS [7:0]</th> <th>Return Value(degC)</th> </tr> </thead> <tbody> <tr> <td>E7h</td> <td>-25</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>FFh</td> <td>-1</td> </tr> <tr> <td>00h</td> <td>0</td> </tr> <tr> <td>01h</td> <td>1</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>19h</td> <td>25</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>31h</td> <td>49</td> </tr> <tr> <td>32h</td> <td>50</td> </tr> </tbody> </table>	TS [7:0]	Return Value(degC)	E7h	-25	...	...	FFh	-1	00h	0	01h	1	...	...	19h	25	...	...	31h	49	32h	50																																			
TS [7:0]	Return Value(degC)																																																																				
E7h	-25																																																																				
...	...																																																																				
FFh	-1																																																																				
00h	0																																																																				
01h	1																																																																				
...	...																																																																				
19h	25																																																																				
...	...																																																																				
31h	49																																																																				
32h	50																																																																				
0	0	41	0	1	0	0	0	0	0	1	TSE	Temperature Sensor Enable Register																																																									
0	1		0	0	0	0	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	0		<p>This command selects Temperature offset A[7:0] = 00h [POR]</p> <p>A[3:0] ~ TO[3:1], Temperature offset:</p> <table border="1"> <thead> <tr> <th>TO[3:1]</th> <th>Calculation</th> <th>TO[3:1]</th> <th>Calculation</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>+0</td> <td>100</td> <td>-4</td> </tr> <tr> <td>001</td> <td>+1</td> <td>101</td> <td>-3</td> </tr> <tr> <td>010</td> <td>+2</td> <td>110</td> <td>-2</td> </tr> <tr> <td>011</td> <td>+3</td> <td>111</td> <td>-1</td> </tr> </tbody> </table>	TO[3:1]	Calculation	TO[3:1]	Calculation	000	+0	100	-4	001	+1	101	-3	010	+2	110	-2	011	+3	111	-1																																					
TO[3:1]	Calculation	TO[3:1]	Calculation																																																																		
000	+0	100	-4																																																																		
001	+1	101	-3																																																																		
010	+2	110	-2																																																																		
011	+3	111	-1																																																																		
0	0	50	0	1	0	1	0	0	0	0	CDI	VCOM and DATA interval setting Register																																																									
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		<p>This command indicates the Border Output Selection and the interval between Vcom and data output A[7:0] = 97h [POR]</p> <p>A[7:5]~VBD [2:0] Border Output Selection:</p> <table border="1"> <thead> <tr> <th></th> <th>DDX=1</th> <th>DDX=0</th> </tr> </thead> <tbody> <tr> <th>VBD[2:0]</th> <th>LUT (Default)</th> <th>LUT</th> </tr> <tr> <td>000</td> <td>Gray 0</td> <td>HIZ</td> </tr> <tr> <td>001</td> <td>Gray 1</td> <td>Gray 3</td> </tr> <tr> <td>010</td> <td>Gray 2</td> <td>Gray 2</td> </tr> <tr> <td>011</td> <td>Gray 3</td> <td>Gray 1</td> </tr> <tr> <td>100</td> <td>HIZ(Default)</td> <td>Gray 0</td> </tr> </tbody> </table> <p>A[4]: DDX Data Polarity for Pixel Data (See DTM command) 0: Invert 1: Non-invert (Default)</p> <p>A[3:0] ~ CDI[3:0] Gate and source blanking time (No gate source scanning)</p> <table border="1"> <thead> <tr> <th>CDI [3:0]</th> <th>Interval (ms)</th> <th>CDI [3:0]</th> <th>Interval (ms)</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>2</td> <td>8h</td> <td>40</td> </tr> <tr> <td>1h</td> <td>4</td> <td>9h</td> <td>60</td> </tr> <tr> <td>2h</td> <td>8</td> <td>Ah</td> <td>80</td> </tr> <tr> <td>3h</td> <td>12</td> <td>Bh</td> <td>100</td> </tr> <tr> <td>4h</td> <td>14</td> <td>Ch</td> <td>120</td> </tr> <tr> <td>5h</td> <td>16</td> <td>Dh</td> <td>140</td> </tr> <tr> <td>6h</td> <td>18</td> <td>Eh</td> <td>160</td> </tr> <tr> <td>7h</td> <td>20 (Default)</td> <td>Fh</td> <td>Reserved</td> </tr> </tbody> </table> <p>User needs to review CDI setting to have stable VCOM in application</p>		DDX=1	DDX=0	VBD[2:0]	LUT (Default)	LUT	000	Gray 0	HIZ	001	Gray 1	Gray 3	010	Gray 2	Gray 2	011	Gray 3	Gray 1	100	HIZ(Default)	Gray 0	CDI [3:0]	Interval (ms)	CDI [3:0]	Interval (ms)	0h	2	8h	40	1h	4	9h	60	2h	8	Ah	80	3h	12	Bh	100	4h	14	Ch	120	5h	16	Dh	140	6h	18	Eh	160	7h	20 (Default)	Fh	Reserved
	DDX=1	DDX=0																																																																			
VBD[2:0]	LUT (Default)	LUT																																																																			
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010	Gray 2	Gray 2																																																																			
011	Gray 3	Gray 1																																																																			
100	HIZ(Default)	Gray 0																																																																			
CDI [3:0]	Interval (ms)	CDI [3:0]	Interval (ms)																																																																		
0h	2	8h	40																																																																		
1h	4	9h	60																																																																		
2h	8	Ah	80																																																																		
3h	12	Bh	100																																																																		
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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																
0	0	51	0	1	0	1	0	0	0	1	LPD	Lower Power Detection Register																
1	1		0	0	0	0	0	0	0	A <sub>0</sub>		BUSY_N will output low during operation. Then the LPD status can be read. A[0] ~ LPD status 0: Low power input (VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL) 1: Normal (default)																
0	0	61	0	1	1	0	0	0	0	1	TRES	Resolution setting Register A[9:0] = 3C0h [POR] B[9:0] = 2A8h [POR]																
0	1		0	0	0	0	0	0	A <sub>9</sub>	A <sub>8</sub>		This command defines alternative resolution. A[9:0] ~ HRES[9:0] Horizontal Display Resolution Remark: Horizontal resolution should be 4-multiple. B[9:0] ~ VRES[9:0] Vertical Display Resolution  e.g. HRES= 3C0h, VRES= 2A8h																
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																		
0	1		0	0	0	0	0	0	B <sub>9</sub>	B <sub>8</sub>																		
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>																		
0	1																											
												<table border="1"> <thead> <tr> <th>UD,SHL</th> <th>Source and gate sequence</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>S959,G679 to S0,G0</td> </tr> <tr> <td>01</td> <td>S0, G679 to S959,G0</td> </tr> <tr> <td>10</td> <td>S959,G0 to S0, G679</td> </tr> <tr> <td>11</td> <td>S0,G0 to S959, G679</td> </tr> </tbody> </table>	UD,SHL	Source and gate sequence	00	S959,G679 to S0,G0	01	S0, G679 to S959,G0	10	S959,G0 to S0, G679	11	S0,G0 to S959, G679						
UD,SHL	Source and gate sequence																											
00	S959,G679 to S0,G0																											
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10	S959,G0 to S0, G679																											
11	S0,G0 to S959, G679																											
												<p>Remark:</p> <ol style="list-style-type: none"> <li>Both PSR.RES &amp; TRES command can set panel resolution. Priority will be given to the last received PSR or TRES command.</li> <li>VRES[9:0] &gt;= 420</li> </ol>																
0	0	65	0	1	1	0	0	1	0	1	GSST	Gate/Source Start Setting Register A[9:0] = 0x000h [POR] B[9:0] = 0x000h [POR]																
0	1								A <sub>9</sub>	A <sub>8</sub>		A[9:0] ~ S_start[9:0] First valid source output channel setting																
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																		
0	1								B <sub>9</sub>	B <sub>8</sub>																		
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>																		
0	1																											
												<table border="1"> <thead> <tr> <th>S_start [9:0]</th> <th>First valid source output</th> </tr> </thead> <tbody> <tr> <td>000h</td> <td>S0 (Default)</td> </tr> <tr> <td>004h</td> <td>S4</td> </tr> <tr> <td>008h</td> <td>S8</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>3B8h</td> <td>S952</td> </tr> <tr> <td>3BCh</td> <td>S956</td> </tr> <tr> <td>Other</td> <td>Reserved</td> </tr> </tbody> </table>	S_start [9:0]	First valid source output	000h	S0 (Default)	004h	S4	008h	S8	...	...	3B8h	S952	3BCh	S956	Other	Reserved
S_start [9:0]	First valid source output																											
000h	S0 (Default)																											
004h	S4																											
008h	S8																											
...	...																											
3B8h	S952																											
3BCh	S956																											
Other	Reserved																											
												<p>B[9:0] ~ G_start[9:0] First valid gate output channel setting</p> <p>GSST and TRES can define the display window from target source and gate start and end line. GD: First G active = G16, G_start[9:0]=16. Last G active = G543, VRES[9:0]=528. SD: First S active = S8, S_start[9:0]=8. Last S active = S887, HRES[9:0]=880.</p> <p>Remark: G_start+VRES&lt; 680, S_start+HRES&lt; 960.</p>																

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																						
0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register The command is to read the ID A[7:0] = 07h [POR] B[7:0] = 01h [POR] C[7:0] = 01h [POR]																						
1	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																								
1	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>																								
1	1		C <sub>7</sub>	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>																								
0	0	80	1	0	0	0	0	0	0	0	AMV	Auto Measurement VCOM Register This command implements related VCOM sensing setting. A[7:0] = 00h [POR]																						
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	0	A <sub>0</sub>			<p>A[7:6] ~ P[1:0] Number of sensing Points 00: 2 (Default) 01: 4 10: 8 11: 16</p> <p>A[5:4] ~ AMVT[1:0] Auto Measure Vcom Time: Sensing Time 00: 5 sec. (Default) 01: 10 sec. 10: 15 sec. 11: 20 sec.</p> <p>A[3] ~ AMVX VCOM measurement Gate settings 0: Gate scan normally during VCOM measurement (Default) 1: All Gates ON during VCOM measurement</p> <p>A[2] ~ AMVS Source output of AMV: 0: Set Source output to 0V during Auto Measure VCOM period. (Default) 1: Set Source output to VSH_LV during Auto Measure VCOM period.</p> <p>A[0] ~ AMVE Auto Measure Vcom Enable (/Disable): 0: Disabled (Default) 1: Enabled BUSY_N will output low during operation.</p> <p>Note: AMV only can work while PON only</p>																					
0	0	81	1	0	0	0	0	0	0	1	VV	Auto Measurement VCOM Register This command gets the Vcom value after AMV.																						
1	1		1	0	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>			<p>A[5:0] ~ VV[5:0]: Vcom read Value , valid range from -0.2V to -4.0V.</p> <table border="1"> <thead> <tr> <th>VV[5:0]</th> <th>Vcom read value</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Reserved</td> </tr> <tr> <td>04h</td> <td>-0.2V</td> </tr> <tr> <td>08h</td> <td>-0.4V</td> </tr> <tr> <td>0Ch</td> <td>-0.6V</td> </tr> <tr> <td>10h</td> <td>-0.8V</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>3Ch</td> <td>-3.0V</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>50h</td> <td>-4.0V</td> </tr> <tr> <td>others</td> <td>Reserved</td> </tr> </tbody> </table>	VV[5:0]	Vcom read value	00h	Reserved	04h	-0.2V	08h	-0.4V	0Ch	-0.6V	10h	-0.8V	...	...	3Ch	-3.0V	...	...	50h	-4.0V	others
VV[5:0]	Vcom read value																																	
00h	Reserved																																	
04h	-0.2V																																	
08h	-0.4V																																	
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others	Reserved																																	

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0] = 00h [POR]
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	0	0		A[7] ~ OTP_VCM  Vcom follow VDCS after RESET. 0: Disable (Default), auto load from OTP if it is valid. 1: Enable, VCOM value from the VDCS[6:0]  A[6:0] ~ VDCS[6:0]: VCOM_DC Setting, 0.2V step from -0.2V to -4.0V.
			<b>VDCS [6:0]</b>		<b>VCOM_DC Setting</b>							
			00h		Reserved							
			04h		-0.2V							
			08h		-0.4V							
			0Ch		-0.6V							
			10h		-0.8V							
			...		...							
			3Ch		-3.0V							
			...		...							
			50h		-4.0V							
			others		Reserved							
0	0	83	1	0	0	0	0	0	1	1	PTLW	Partial Window This command sets partial window address. A[9:0] = 000h [POR] B[9:0] = 3BFh [POR] C[9:0] = 000h [POR] D[9:0] = 2A7h [POR] E[7:0] = 00h [POR]
0			0	0	0	0	0	0	A <sub>9</sub>	A <sub>8</sub>		A[9:0] ~ HRST [9:0] Horizontal start address
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		B[9:0] ~ HRED [9:0] Horizontal end address
0	1		0	0	0	0	0	0	B <sub>9</sub>	B <sub>8</sub>		C[9:0] ~ VRST [9:0] Vertical start address
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		D[9:0] ~ VRED [9:0] Vertical end address
0	1		0	0	0	0	0	0	C <sub>9</sub>	C <sub>8</sub>		E[0] ~ PMODE 0: disable partial mode (Default) 1: enable partial mode Gate scan both inside and outside of the partial window
0	1		C <sub>7</sub>	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		Note: 1) HRST [9:0] <= HRED [9:0] 2) VRST [9:0] <= VRED [9:0]
0	1		0	0	0	0	0	0	D <sub>9</sub>	D <sub>8</sub>		
0	1		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
0	1		0	0	0	0	0	0	0	E <sub>0</sub>		

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																			
0	0	90	1	0	0	1	0	0	0	0	PGM	<p>Program Mode</p> <p>This command is to set OTP program mode After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leave the program mode</p> <p>BUSY_N will output low when PGM mode is ready.</p>																																			
0	0	91	1	0	0	1	0	0	0	1	APG	<p>Active Program</p> <p>This command is to execute OTP program After this command is issued, the chip would program the OTP. BUSY_N will output low during operation.</p> <p>Note: In PON mode with internal programming power.</p>																																			
0	0	92	1	0	0	1	0	0	1	0	ROTP	<p>Read OTP Data</p> <p>This command is to read the OTP content from SRAM.</p> <p>The 1<sup>st</sup> byte read is dummy byte. The 2<sup>nd</sup> byte read is the content of Address 0 in OTP The N+1<sup>th</sup> byte read is the content of Address n in OTP After issue this command, the host must read at least 1 byte data from the device.</p>																																			
1	1		<p>1<sup>st</sup> ~ dummy 2<sup>nd</sup> ~ N+1th Parameter</p>																																												
0	0	E0	1	1	1	0	0	0	1	1	CCSET	<p>Cascade &amp; External temperature input A[7:0] = 00h [POR]</p>																																			
0	1		0	0	0	0	0	0	A <sub>1</sub>	A <sub>0</sub>		<p>A[1] ~ TSFIX 0: Use Internal Temperature Sensor (Default) 1: Use command 0xE6 TS_SET [7:0] value A[0] ~ CSEIN, cascade mode enable 0: Disable 1: Enable</p>																																			
0	0	E3	1	1	1	0	0	0	1	1	PWS	<p>Power Saving Register</p> <p>This command is sets for saving power VCOM/Source power saving during display refresh period. A[7:0] = 65h [POR]</p>																																			
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		<p>If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.</p> <p>A[7:4] = VCOM_W [3:0]</p> <table border="1"> <thead> <tr> <th>VCOM_W [3:0]</th> <th>VCOM_power saving width. (time unit)</th> <th>VCOM_W [3:0]</th> <th>VCOM_power saving width. (time unit)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Reserved</td> <td>8</td> <td>8</td> </tr> <tr> <td>1</td> <td>1</td> <td>9</td> <td>9</td> </tr> <tr> <td>2</td> <td>2</td> <td>10</td> <td>10</td> </tr> <tr> <td>3</td> <td>3</td> <td>11</td> <td>11</td> </tr> <tr> <td>4</td> <td>4</td> <td>12</td> <td>12</td> </tr> <tr> <td>5</td> <td>5</td> <td>13</td> <td>13</td> </tr> <tr> <td>6</td> <td>6[Default]</td> <td>14</td> <td>14</td> </tr> <tr> <td>7</td> <td>7</td> <td>15</td> <td>15</td> </tr> </tbody> </table>	VCOM_W [3:0]	VCOM_power saving width. (time unit)	VCOM_W [3:0]	VCOM_power saving width. (time unit)	0	Reserved	8	8	1	1	9	9	2	2	10	10	3	3	11	11	4	4	12	12	5	5	13	13	6	6[Default]	14	14	7	7	15
VCOM_W [3:0]	VCOM_power saving width. (time unit)	VCOM_W [3:0]	VCOM_power saving width. (time unit)																																												
0	Reserved	8	8																																												
1	1	9	9																																												
2	2	10	10																																												
3	3	11	11																																												
4	4	12	12																																												
5	5	13	13																																												
6	6[Default]	14	14																																												
7	7	15	15																																												

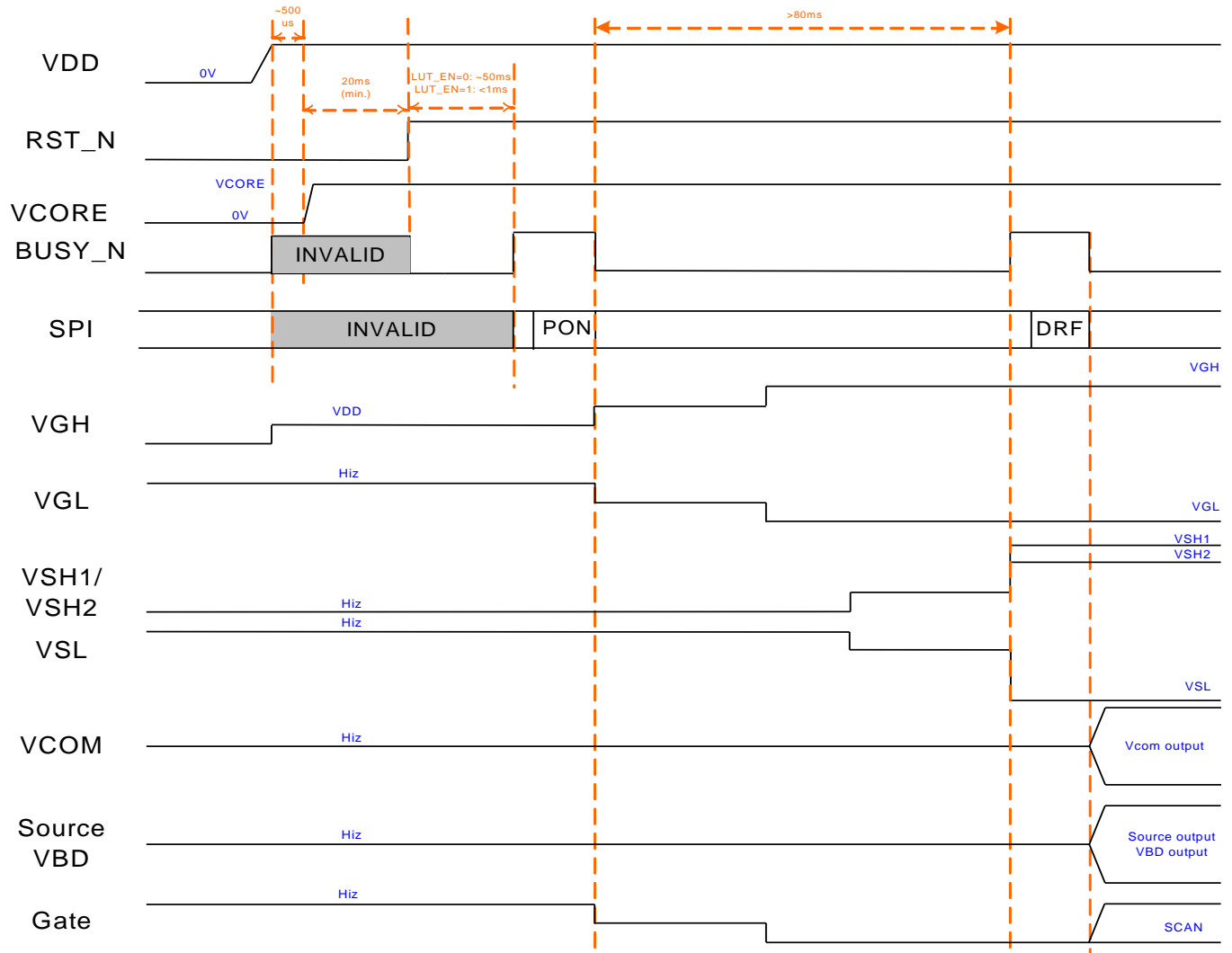
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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																				
												A[3:0] = SD_W [3:0] <table border="1"> <thead> <tr> <th>SD_W [3:0]</th> <th>Source power saving width[us]</th> <th>SD_W [3:0]</th> <th>Source power saving width [us]</th> </tr> </thead> <tbody> <tr><td>0</td><td>Reserved</td><td>8</td><td>4</td></tr> <tr><td>1</td><td>0.5</td><td>9</td><td>4.5</td></tr> <tr><td>2</td><td>1</td><td>10</td><td>5</td></tr> <tr><td>3</td><td>1.5</td><td>11</td><td>5.5</td></tr> <tr><td>4</td><td>2</td><td>12</td><td>6</td></tr> <tr><td>5</td><td>2.5[Default]</td><td>13</td><td>6.5</td></tr> <tr><td>6</td><td>3</td><td>14</td><td>7</td></tr> <tr><td>7</td><td>3.5</td><td>15</td><td>7.5</td></tr> </tbody> </table> Remark: VCOM_W setting < CDI setting SD_W setting < S2G setting	SD_W [3:0]	Source power saving width[us]	SD_W [3:0]	Source power saving width [us]	0	Reserved	8	4	1	0.5	9	4.5	2	1	10	5	3	1.5	11	5.5	4	2	12	6	5	2.5[Default]	13	6.5	6	3	14	7	7	3.5	15	7.5
SD_W [3:0]	Source power saving width[us]	SD_W [3:0]	Source power saving width [us]																																													
0	Reserved	8	4																																													
1	0.5	9	4.5																																													
2	1	10	5																																													
3	1.5	11	5.5																																													
4	2	12	6																																													
5	2.5[Default]	13	6.5																																													
6	3	14	7																																													
7	3.5	15	7.5																																													
0	0	E4	1	1	1	0	0	1	0	0	LVSEL	LVD Voltage Select Register This command is sets for low power detect level power A[1:0] = 03h [POR]																																				
0	1		0	0	0	0	0	0	A <sub>1</sub>	A <sub>0</sub>		A[1:0] ~ LVD_SEL[1:0] Low power detection threshold 00: 2.2V 01: 2.3V 10: 2.4V 11 : 2.5V (Default)																																				
0	0	E6	1	1	1	1	0	1	1	0	TS_SET	Manual input temperature value This command is to force the TS value A[7:0] = 00h [POR]																																				
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		A[7:0] ~ TS_SET[7:0] When TSFIX=1, Temperature value will be set by TS_SET[7:0]. Format of the temperature value is 8-bit binary value and it is 1degC per step. <table border="1"> <thead> <tr> <th>TS_SET[7:0]</th> <th>Force the TS Value(degC)</th> </tr> </thead> <tbody> <tr><td>E7h</td><td>-25</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>FFh</td><td>-1</td></tr> <tr><td>00h</td><td>0</td></tr> <tr><td>01h</td><td>1</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>19h</td><td>25</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>31h</td><td>49</td></tr> <tr><td>32h</td><td>50</td></tr> </tbody> </table>	TS_SET[7:0]	Force the TS Value(degC)	E7h	-25	...	...	FFh	-1	00h	0	01h	1	...	...	19h	25	...	...	31h	49	32h	50														
TS_SET[7:0]	Force the TS Value(degC)																																															
E7h	-25																																															
...	...																																															
FFh	-1																																															
00h	0																																															
01h	1																																															
...	...																																															
19h	25																																															
...	...																																															
31h	49																																															
32h	50																																															

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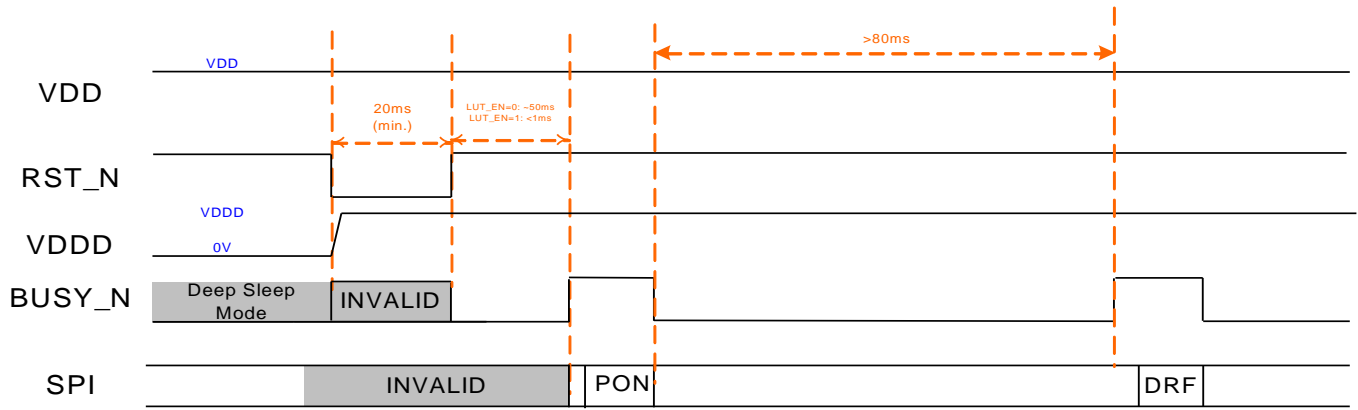
## 9 Display on/off Sequence

### 9.1 Display on sequence from VDD power on

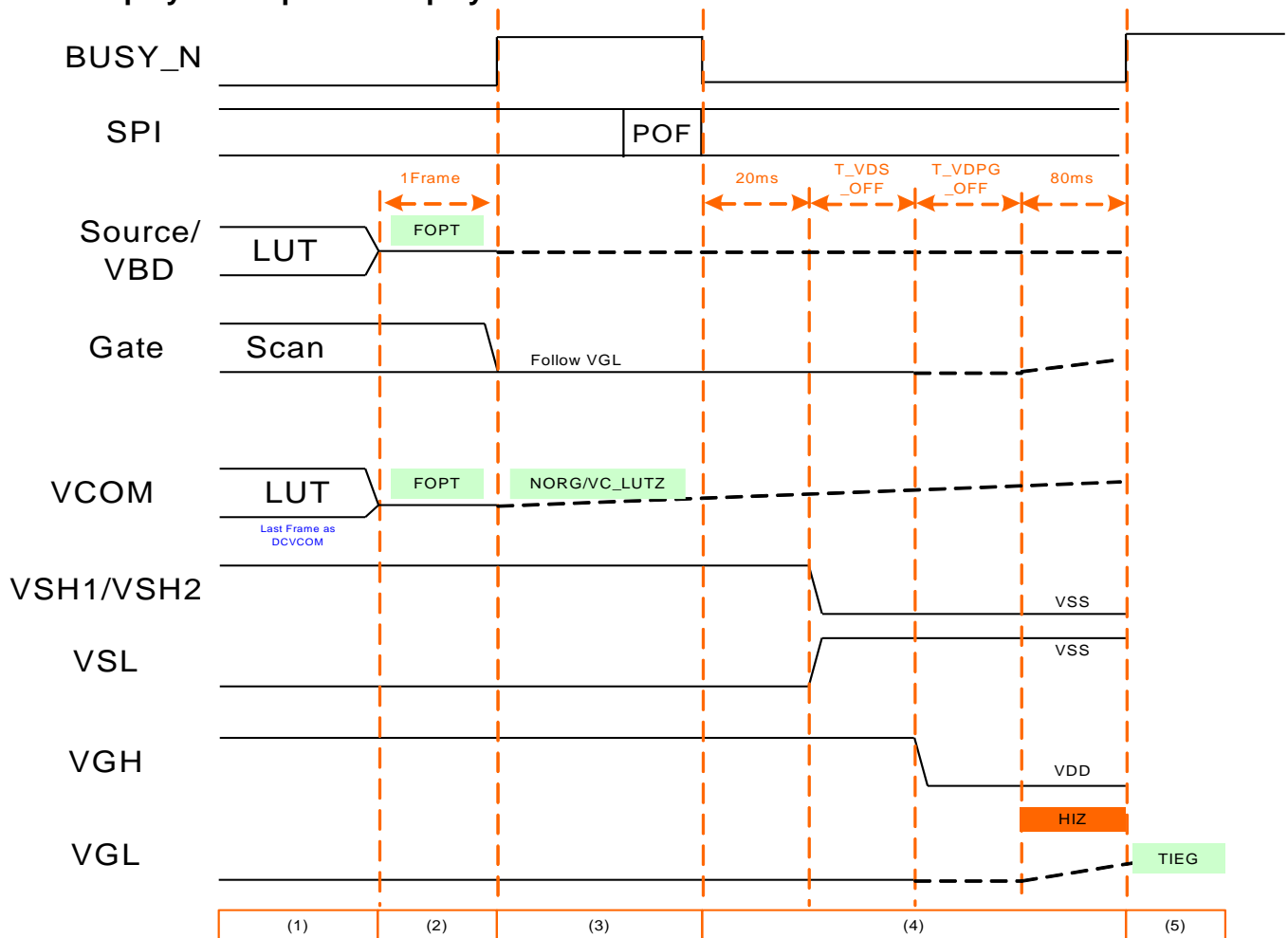


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## 9.2 Display on sequence from deep sleep mode



## 9.3 Display off Sequence Display



Note: If VCOM and VGL set as floating after display update. Please wait until the system completely discharge before next operation.

## 10 Absolute Maximum Rating

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V <sub>DD</sub>	Logic supply voltage	-0.5 to +4.0	V
V <sub>IN</sub>	Logic Input voltage	-0.5 to V <sub>DDIO</sub> +0.5	V
V <sub>OUT</sub>	Logic Output voltage	-0.5 to V <sub>DDIO</sub> +0.5	V
T <sub>OPR</sub>	Operation temperature range	-30 to +85	°C
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V<sub>DD</sub> be constrained to the range GND < V<sub>DD</sub>. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either GND or V<sub>DDIO</sub>). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

## 11 Electrical Characteristics

The following specifications apply for: GND=0V, VDD=3.0V, T<sub>OPR</sub>=25°C.

Table 11-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	VDD supply operation voltage	VDD		2.3	3.0	3.6	V
V <sub>COM_DC</sub>	VCOM_DC output voltage	VCOM		-4.0	-	-0.2	V
dV <sub>COM_DC</sub>	VCOM_DC output voltage deviation	VCOM	No output load	-200	-	200	mV
V <sub>COM_AC</sub>	VCOM_AC output voltage	VCOM		V <sub>SL</sub>	V <sub>COM_DC</sub>	V <sub>SH</sub>	V
V <sub>GATE</sub>	Gate output voltage	G0~G679		-20	-	+20	V
V <sub>GATE(p-p)</sub>	Gate output peak to peak voltage	G0~G679		-	-	40	V
V <sub>SH</sub>	Positive Source output voltage	VSH1		+3		+15	V
V <sub>SH2</sub>	Positive Source output voltage	VSH2		+3		+15	V
dV <sub>SH</sub>	VSH1/VSH2 output voltage deviation	VSH1/ VSH2	No output load	-200	-	200	mV
V <sub>SL</sub>	Negative Source output voltage	VSL		-15		-3	V
dV <sub>SL</sub>	VSL output voltage deviation	VSL	No output load	-200	-	200	mV
V <sub>IH</sub>	High level input voltage	SDA SCL, CSB, D/C, RST_N, BS1, M/S#		0.8V <sub>DDIO</sub>	-	-	V
V <sub>IL</sub>	Low level input voltage			-	-	0.2V <sub>DDIO</sub>	V
V <sub>OH</sub>	High level output voltage	SDA, BUSY_N,	IOH = -100uA	0.8V <sub>DDIO</sub>	-	-	V
V <sub>OL</sub>	Low level output voltage		IOL = 100uA	-	-	0.2V <sub>DDIO</sub>	V
V <sub>PP</sub>	OTP Program voltage	VPP		8.1	8.3	8.5	V

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Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Islp_VDD	Sleep mode current	VDD	- DC/DC off - No clock - No output load - MCU interface access - RAM data access	-	20	35	uA
I <sub>deep</sub> _VDD	deep sleep current	VDD	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data	-		1	uA
Iopr_VDD	Operating Mode current	VDD	VDD=3V	-	1	-	mA
V <sub>GH</sub>	Operating Mode Output Voltage	VGH	After PON Command	19.5	20	20.5	V
V <sub>SH</sub>		VSH1	VGH=20V VGL=-VGH VSH=15V	14.8	15	15.2	V
V <sub>SH2</sub>		VSH2	VSH=15V VSH2=15V VSL=-15V	14.8	15	15.2	V
V <sub>SL</sub>		VSL	VCOM = -2V	-15.2	-15	-14.8	V
V <sub>COM</sub>		VCOM	No waveform transitions. No output load No RAM read/write	-2.2	-2	-1.8	V

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## 12 AC Characteristics

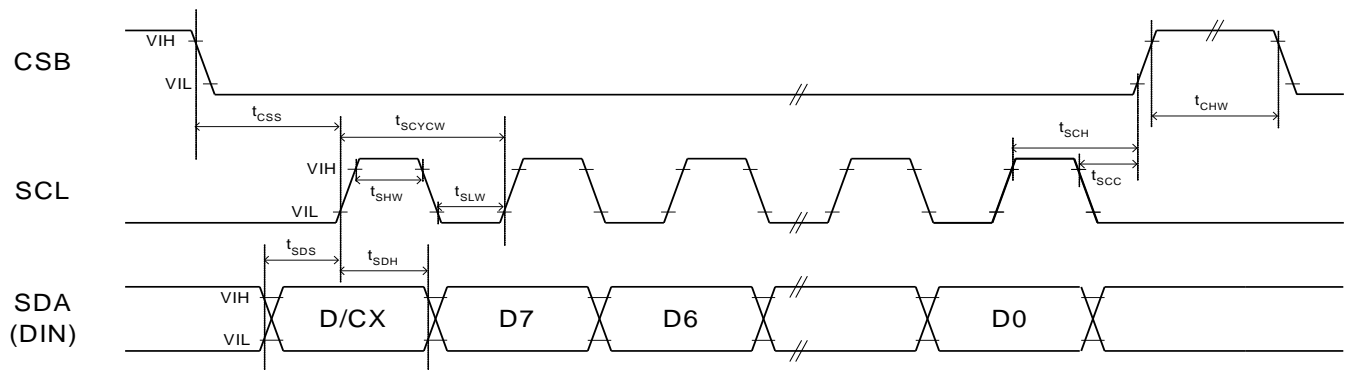
### 12.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - GND = 2.3V to 3.6V, T<sub>OPR</sub> = 25°C, CL=20pF

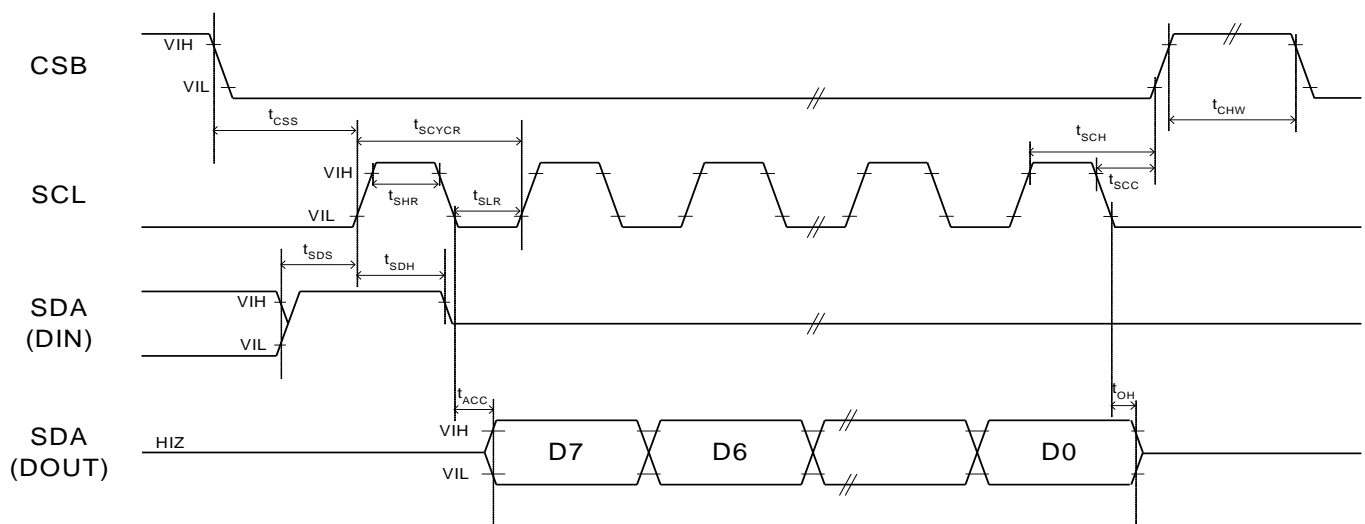
**Table 12-1 : Serial Peripheral Interface Timing Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
t <sub>CSS</sub>	CSB select setup time	60			ns
t <sub>SCH</sub>	CSB select hold time	65			ns
t <sub>SCC</sub>	CSB deselect setup time	25			ns
t <sub>CHW</sub>	CSB deselect hold time	100			ns
t <sub>SCYCW</sub>	Serial clock cycle (Write)	50			ns
t <sub>SHW</sub>	SCL "H" pulse width (Write)	25			ns
t <sub>SLW</sub>	SCL "L" pulse width (Write)	25			ns
t <sub>SCYCL</sub>	Serial clock cycle (Read)	400			ns
t <sub>SHR</sub>	SCL "H" pulse width (Read)	180			ns
t <sub>SLR</sub>	SCL "L" pulse width (Read)	180			ns
t <sub>SDS</sub>	Data setup time	30			ns
t <sub>SDH</sub>	Data hold time	30			ns
t <sub>DCS</sub>	DC setup time	40			ns
t <sub>DCH</sub>	DC hold time	40			ns
t <sub>ACC</sub>	Access time			100	ns
t <sub>OH</sub>	Output disable time	15			ns

Note: All timings are based on 20% to 80% of VDDIO-GND



**Figure 12-1: 3-wire SPI characteristics (write mode)**



**Figure 12-2: 3-wire SPI characteristics (read mode)**

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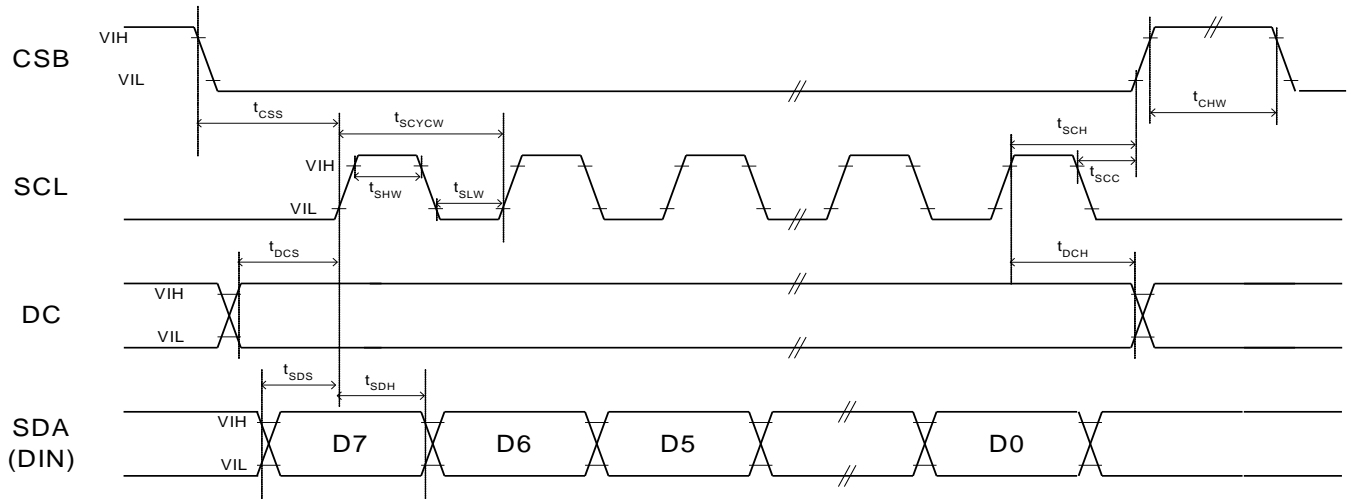


Figure 12-3: 4-wire SPI characteristics (write mode)

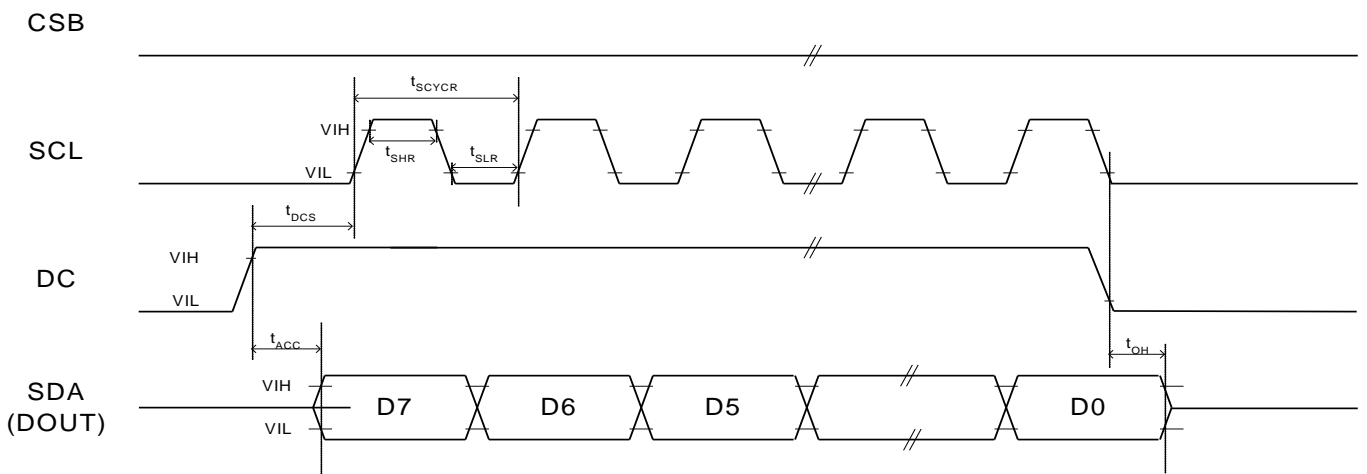


Figure 12-4: 4-wire SPI characteristics (read mode)

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## 13 Application Circuit

Figure 13-1: SSD2677 application circuit

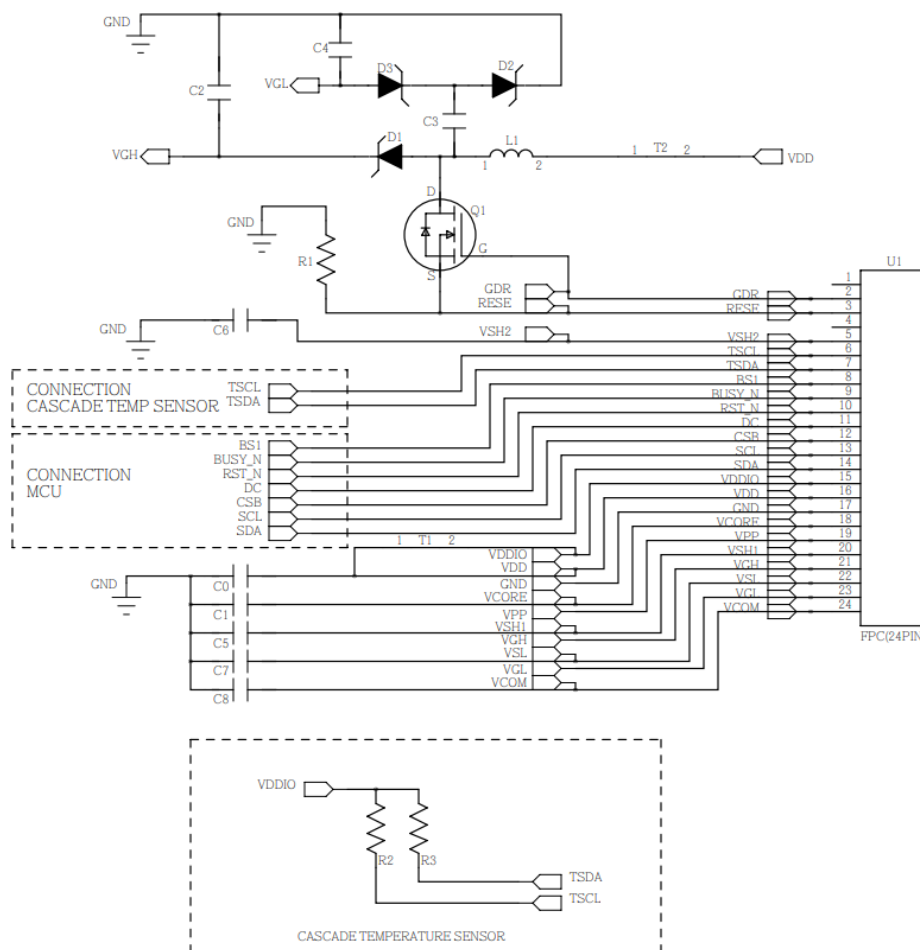


Table 13-1: Component list for SSD2677 application circuit

Part Name	Value	Requirements/Reference Part
C0	4.7uF	0603/0805: X5R/X7R; Voltage Rating : 6V or 25V
C1	1uF	0603/0805: X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	4.7uF	0805; X5R/X7R; Voltage Rating: 25V
C8	1uF	0805; X7R; Voltage Rating: 25V
R1	2.2 ohm	0805; 1%
D1-D3	Diode	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) $I_o \geq 500mA$ 3) Forward voltage $\leq 430mV$
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage $\leq 30V$ 2) $V_{gs(th)} = 0.9V$ (Typ), 1.3V (Max) 3) $R_{ds\ on} \leq 2.1\Omega$ @ $V_{gs} = 2.5V$
L1	47uH	CDRH2D18 / LDNP-470NC $I_o = 500mA$ (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

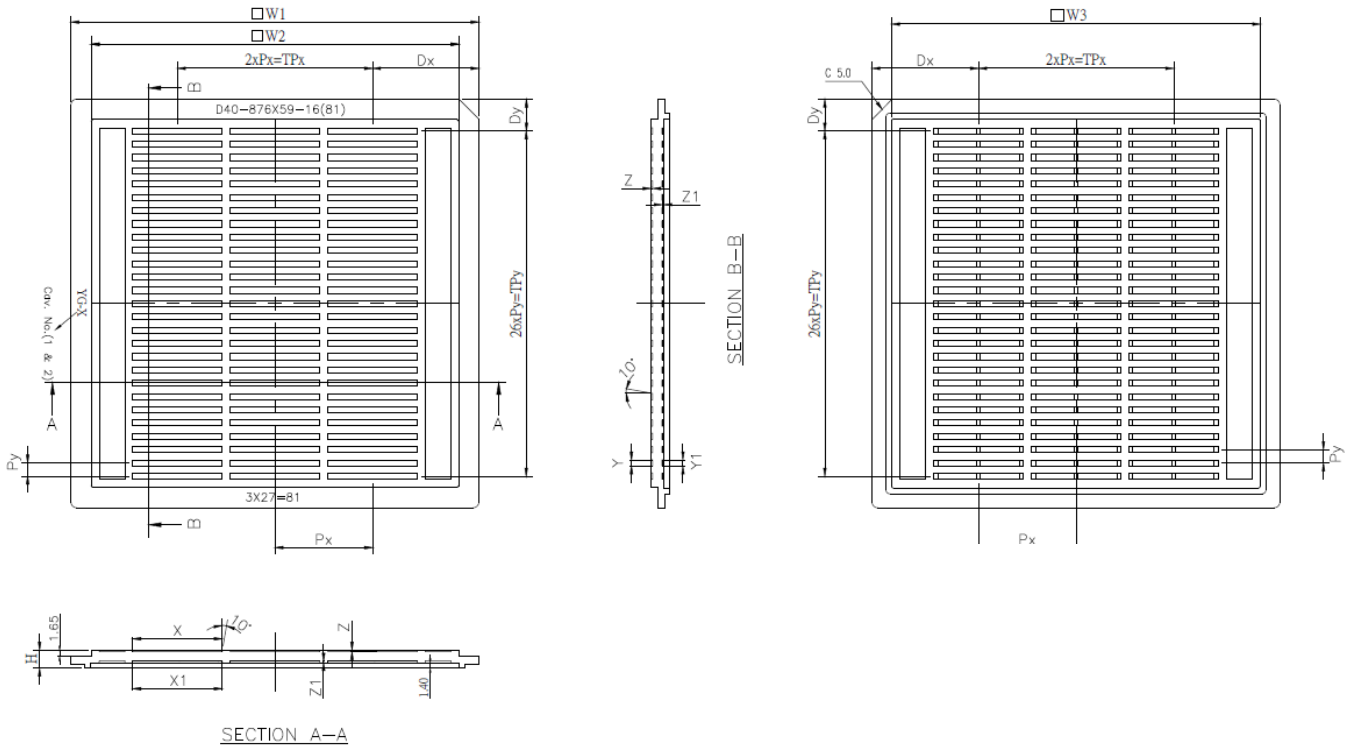
### Remarks:

- 1) The recommended component value and reference part in Table 13-1 is subject to change depending on panel loading.
- 2) Customer is required to review if the selected component value and part is suitable for their application.

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# 14 Package Information


Figure 14-1 : SSD2677ZB and SSD2677ZC tray information



Symbol	Spec (mm)
W1	101.60±0.10
W2	91.55±0.10
W3	91.85±0.10
H	4.55±0.10
Dx	26.50±0.05
TPx	48.60±0.10
Dy	7.90±0.05
Tpy	85.80±0.10
Px	24.30±0.05
Py	3.30±0.05
X	22.25±0.05
Y	1.51±0.05
Z	0.40±0.05
X1	22.25±0.05
Y1	1.51±0.05
Z1	0.35±0.05
N	81 (pocket number)

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