ST7305

Ultra-Low Power Active Matrix 264H x 320V TFT Display Driver with Controller

Datasheet

Version 0.2

Hazardous Substance Free
RoHS/ REACH Compliant

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1 INTRODUCTION

The ST7305 is a single-chip controller/driver for small and medium TFT LCD display that operate at very low frame frequency to conserve power. This chip is capable of supporting up to 264H x 320V pixels and provides a standard 8-bit 8080 parallel interface, 3-wire SPI serial interface and single/dual 4-wire SPI serial interface to configure the system and update the graphics content. The 264-channel source driver supports 1-bit per pixel (or sub-pixel) control to simplify the driver construction and lower power dissipation.

ST7305 is controlled using a conventional mobile driver SoC interface which supports an interface I/O voltage (VDDI) of 1.8V ~ 3.3V. ST7305 is equipped with all required charge pumps, buffer amplifiers and regulators to run directly from an unregulated coin cell battery source (Normal mode VDDA=2.8V ~ 3.3V; 1.8V mode VDDA=1.8V). All voltages used by the TFT channel drivers are close loop regulated by ST7305 and can be adjusted in fine increments by user controlled digital register settings to optimize power and display characteristics. The built-in timing controller (TCON) supports a wide range of output timing for various pixel organizations and driver waveform generation. The combination of timing and voltage controls allows the ST7305 driver SoC to have wide compatibility with various LCD and TFT types.

2 FEATURES

Design for Low Power Active Matrix a-Si TFT Display

Single-chip TFT-LCD Controller/Driver with On-chip Frame Memory

Support for 264H x 320V Mono pixels

Outputs bi-level 1-bit per pixel source drive

Support multiple frame rate (0.25Hz ~ 51 Hz)

Supports multiple LCD modes

- ECB or MTN
- Normally black or white

Built-in 264 x 320 x 1b internal SRAM

Dot/Column inversion DC drive of TFTs at low refresh rates

Built-in Sequential/Interlace Gate Scan Function

Microprocessor Interface

- 80 parallel 8bits
- 3/ 4-line serial interface support write-operation and read- status/RAM

Wide Power Supply Range

- Normal Mode

  VDDI(Digital) : 1.8V ~ 3.3V

  VDDA(Analog): 2.8V ~ 3.3V
- 1.8V Mode

  VDDI(Digital)=VDDA(Analog)=1.8V

On-chip Build-In Circuits

- DC/DC Converter
- Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
- Internal Oscillator for Display Clock Generation
- Timing Controller

On-chip power management system

Built in charge pump circuits

- 2x boost generates: 6.4V (Normal Mode)
- High voltage +17V/-15V charge pump

Built in low power analog circuit

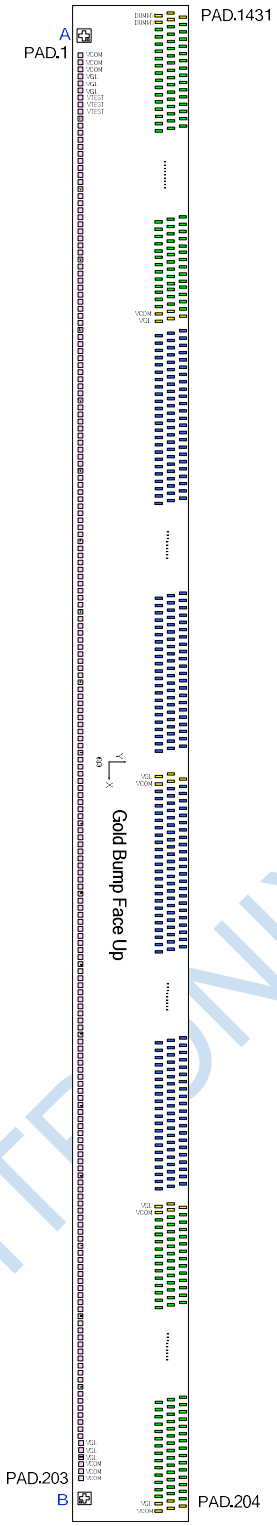
- On-chip oscillator circuit.
- Built-in voltage regulator with programmable contrast
- On-chip power system
  - VCOM level : GND
  - Source Voltage (VSHP/VSHN/VSLP/VSLN): +6.2V ~ -5.2V

- Gate Driver HIGH Level (VGH to AGND): +8V ~ +17V
- Gate Driver LOW Level (VGL to AGND): -6V ~ -15V
- Max. VGH – VGL: 32V

- **Built-in NV memory for VSHP/VSLP/VSHN/VSLN amplitude adjustment and ID setting.**
- **COG packaging**
- **Wide operating temperature range: -30°C ~ +85°C**

3 PAD ARRANGEMENT

3.1 Configuration of Signal Pads



ST7305	
Chip Thinness	200
Bump Height	12
Output Pad	13(X) x 95(Y)
I/O Pad	40(X) x 50(Y)

Unit: um

Figure 3-1 Chip

3.2 Bump

3.2.1 Output Pads

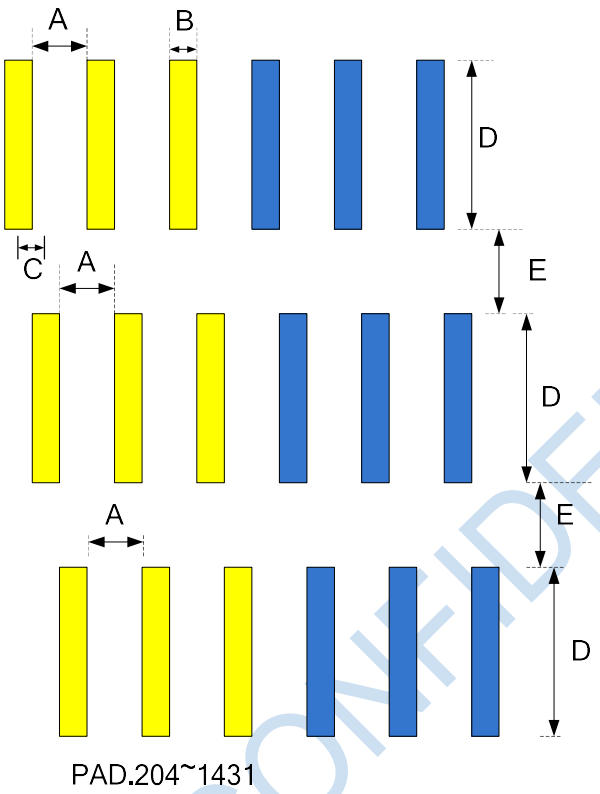
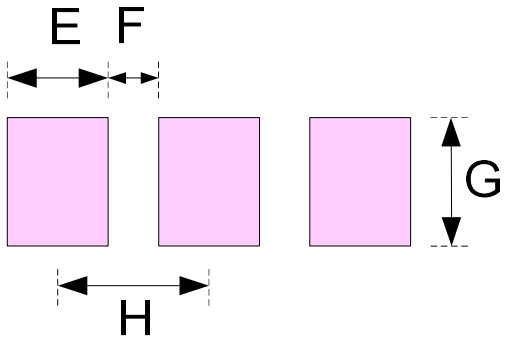


Figure 3-2 Output Pads Outline

Symbol	Item	Size (um)
A	Bump Gap (H)	17
B	Bump Width	13
C	Bump Pitch	10
D	Bump Height	95
E	Bump Gap (V)	20

3.2.2 Input Pads



Symbol	Item	Size (um)
E	Bump Width	40
F	Bump Gap	20
G	Bump Height	50
H	Bump Pitch	60

Figure 3-3 Input Pads Outline

3.2.3 Alignment Marks

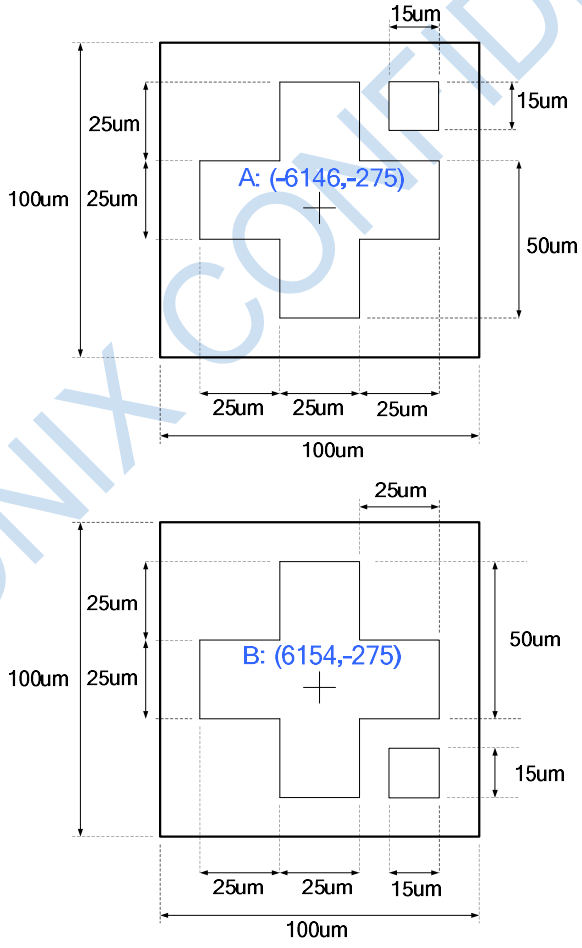


Figure 4 Alignment Marks Outline

4 PAD CENTER COORDINATES

PAD.	Name	X	Y
1	VCOM	-6056	-292.62
2	VCOM	-5996	-292.62
3	VCOM	-5936	-292.62
4	VGL	-5876	-292.62
5	VGL	-5816	-292.62
6	VGL	-5756	-292.62
7	VTEST	-5696	-292.62
8	VTEST	-5636	-292.62
9	VTEST	-5576	-292.62
10	VTEST	-5516	-292.62
11	VTEST	-5456	-292.62
12	VTEST	-5396	-292.62
13	VTEST	-5336	-292.62
14	VTEST	-5276	-292.62
15	VCOM	-5216	-292.62
16	VCOM	-5156	-292.62
17	VCOM	-5096	-292.62
18	VCOM	-5036	-292.62
19	VCOM	-4976	-292.62
20	VCOM	-4916	-292.62
21	VDDA	-4856	-292.62
22	VDDA	-4796	-292.62
23	VDDA	-4736	-292.62
24	VAGND	-4676	-292.62
25	VAGND	-4616	-292.62
26	VAGND	-4556	-292.62
27	CA1N	-4496	-292.62
28	CA1N	-4436	-292.62
29	CA1N	-4376	-292.62
30	CA1N	-4316	-292.62
31	CA1P	-4256	-292.62
32	CA1P	-4196	-292.62
33	CA1P	-4136	-292.62
34	CA1P	-4076	-292.62
35	CA1P	-4016	-292.62
36	CA1P	-3956	-292.62
37	VPV	-3896	-292.62
38	VPV	-3836	-292.62
39	VPV	-3776	-292.62
40	VPV	-3716	-292.62
41	VPV	-3656	-292.62
42	VPV	-3596	-292.62
43	CA2P	-3536	-292.62
44	CA2P	-3476	-292.62
45	CA2P	-3416	-292.62
46	CA2P	-3356	-292.62
47	CA2P	-3296	-292.62
48	CA2P	-3236	-292.62
49	CA2N	-3176	-292.62
50	CA2N	-3116	-292.62
51	CA2N	-3056	-292.62
52	CA2N	-2996	-292.62
53	CA2N	-2936	-292.62
54	CA2N	-2876	-292.62
55	VNV	-2816	-292.62
56	VNV	-2756	-292.62
57	VNV	-2696	-292.62
58	VNV	-2636	-292.62
59	VNV	-2576	-292.62
60	VNV	-2516	-292.62
61	CF1N	-2456	-292.62
62	CF1N	-2396	-292.62
63	CF1N	-2336	-292.62
64	CF1N	-2276	-292.62
65	CF1P	-2216	-292.62
66	CF1P	-2156	-292.62
67	CF1P	-2096	-292.62
68	CF1P	-2036	-292.62
69	AVDD	-1976	-292.62
70	AVDD	-1916	-292.62
71	AVDD	-1856	-292.62
72	AVDD	-1796	-292.62
73	AVDD	-1736	-292.62
74	AVDD	-1676	-292.62
75	CB2P	-1616	-292.62
76	CB2P	-1556	-292.62
77	CB2P	-1496	-292.62
78	CB2P	-1436	-292.62
79	CB2N	-1376	-292.62
80	CB2N	-1316	-292.62
81	CB2N	-1256	-292.62
82	CB2N	-1196	-292.62
83	CB1P	-1136	-292.62
84	CB1P	-1076	-292.62
85	CB1N	-1016	-292.62
86	CB1N	-956	-292.62
87	CB1N	-896	-292.62
88	CB1N	-836	-292.62
89	V1V	-776	-292.62
90	V1V	-716	-292.62
91	CE1P	-656	-292.62
92	CE1P	-596	-292.62
93	CE1N	-536	-292.62
94	CE1N	-476	-292.62
95	NAVDD	-416	-292.62
96	NAVDD	-356	-292.62
97	CE2N	-296	-292.62
98	CE2N	-236	-292.62
99	CE2P	-176	-292.62

PAD.	Name	X	Y
100	CE2P	-116	-292.62
101	CC1N	-56	-292.62
102	CC1N	4	-292.62
103	CC1P	64	-292.62
104	CC1P	124	-292.62
105	VGH	184	-292.62
106	VGH	244	-292.62
107	CD1P	304	-292.62
108	CD1P	364	-292.62
109	CD1N	424	-292.62
110	CD1N	484	-292.62
111	VGL	544	-292.62
112	VGL	604	-292.62
113	VCCO	664	-292.62
114	VCCO	724	-292.62
115	VCCI	784	-292.62
116	VCCI	844	-292.62
117	VDDA	904	-292.62
118	VDDA	964	-292.62
119	VDDA	1024	-292.62
120	VDDA	1084	-292.62
121	VDDA	1144	-292.62
122	VDDA	1204	-292.62
123	VDDR	1264	-292.62
124	VDDR	1324	-292.62
125	VDDI	1384	-292.62
126	VDDI	1444	-292.62
127	VDDI	1504	-292.62
128	VDDI	1564	-292.62
129	VDGND	1624	-292.62
130	VDGND	1684	-292.62
131	VDGND	1744	-292.62
132	VDGND	1804	-292.62
133	VAGND	1864	-292.62
134	VAGND	1924	-292.62
135	VAGND	1984	-292.62
136	VAGND	2044	-292.62
137	VAGND	2104	-292.62
138	VAGND	2164	-292.62
139	VRGND	2224	-292.62
140	VRGND	2284	-292.62
141	VDDI	2344	-292.62
142	CSB	2404	-292.62
143	A0	2464	-292.62
144	ERD	2524	-292.62
145	RWR	2584	-292.62
146	TESTENB	2644	-292.62
147	MTest5	2704	-292.62
148	MTest4	2764	-292.62
149	MTest3	2824	-292.62
150	RSTB	2884	-292.62
151	VDGND	2944	-292.62
152	D0	3004	-292.62
153	D1	3064	-292.62
154	D2	3124	-292.62
155	D3	3184	-292.62
156	D4	3244	-292.62
157	D5	3304	-292.62
158	D6	3364	-292.62
159	D7	3424	-292.62
160	VDDI	3484	-292.62
161	ModeSel	3544	-292.62
162	IF1	3604	-292.62
163	IF0	3664	-292.62
164	CLS	3724	-292.62
165	CL	3784	-292.62
166	TE	3844	-292.62
167	EXTB	3904	-292.62
168	VPP	3964	-292.62
169	VPP	4024	-292.62
170	VPP	4084	-292.62
171	VPP	4144	-292.62
172	VPP	4204	-292.62
173	VPP	4264	-292.62
174	VDGND	4324	-292.62
175	TESTB	4384	-292.62
176	TESTA	4444	-292.62
177	MTest2	4504	-292.62
178	MTest1	4564	-292.62
179	MTest0	4624	-292.62
180	VDDI	4684	-292.62
181	VCOM	4744	-292.62
182	VCOM	4804	-292.62
183	VCOM	4864	-292.62
184	VCOM	4924	-292.62
185	VCOM	4984	-292.62
186	VCOM	5044	-292.62
187	DUMMY	5104	-292.62
188	DUMMY	5164	-292.62
189	DUMMY	5224	-292.62
190	DUMMY	5284	-292.62
191	DUMMY	5344	-292.62
192	DUMMY	5404	-292.62
193	DUMMY	5464	-292.62
194	DUMMY	5524	-292.62
195	DUMMY	5584	-292.62
196	DUMMY	5644	-292.62
197	DUMMY	5704	-292.62
198	VGL	5764	-292.62
199	VGL	5824	-292.62
200	VGL	5884	-292.62
201	VCOM	5944	-292.62

PAD.	Name	X	Y
202	VCOM	6004	-292.62
203	VCOM	6064	-292.62
204	DUMMY	6239	35.58
205	DUMMY	6229	150.58
206	Gtest	6219	265.58
207	DUMMY	6209	35.58
208	Gtest	6199	150.58
209	G2	6189	265.58
210	G4	6179	35.58
211	G6	6169	150.58
212	G8	6159	265.58
213	G10	6149	35.58
214	G12	6139	150.58
215	G14	6129	265.58
216	G16	6119	35.58
217	G18	6109	150.58
218	G20	6099	265.58
219	G22	6089	35.58
220	G24	6079	150.58
221	G26	6069	265.58
222	G28	6059	35.58
223	G30	6049	150.58
224	G32	6039	265.58
225	G34	6029	35.58
226	G36	6019	150.58
227	G38	6009	265.58
228	G40	5999	35.58
229	G42	5989	150.58
230	G44	5979	265.58
231	G46	5969	35.58
232	G48	5959	150.58
233	G50	5949	265.58
234	G52	5939	35.58
235	G54	5929	150.58
236	G56	5919	265.58
237	G58	5909	35.58
238	G60	5899	150.58
239	G62	5889	265.58
240	G64	5879	35.58
241	G66	5869	150.58
242	G68	5859	265.58
243	G70	5849	35.58
244	G72	5839	150.58
245	G74	5829	265.58
246	G76	5819	35.58
247	G78	5809	150.58
248	G80	5799	265.58
249	G82	5789	35.58
250	G84	5779	150.58
251	G86	5769	265.58
252	G88	5759	35.58
253	G90	5749	150.58
254	G92	5739	265.58
255	G94	5729	35.58
256	G96	5719	150.58
257	G98	5709	265.58
258	G100	5699	35.58
259	G102	5689	150.58
260	G104	5679	265.58
261	G106	5669	35.58
262	G108	5659	150.58
263	G110	5649	265.58
264	G112	5639	35.58
265	G114	5629	150.58
266	G116	5619	265.58
267	G118	5609	35.58
268	G120	5599	150.58
269	G122	5589	265.58
270	G124	5579	35.58
271	G126	5569	150.58
272	G128	5559	265.58
273	G130	5549	35.58
274	G132	5539	150.58
275	G134	5529	265.58
276	G136	5519	35.58
277	G138	5509	150.58
278	G140	5499	265.58
279	G142	5489	35.58
280	G144	5479	150.58
281	G146	5469	265.58
282	G148	5459	35.58
283	G150	5449	150.58
284	G152	5439	265.58
285	G154	5429	35.58
286	G156	5419	150.58
287	G158	5409	265.58
288	G160	5399	35.58
289	G162	5389	150.58
290	G164	5379	265.58
291	G166	5369	35.58
292	G168	5359	150.58
293	G170	5349	265.58
294	G172	5339	35.58
295	G174	5329	150.58
296	G176	5319	265.58
297	G178	5309	35.58
298	G180	5299	150.58
299	G182	5289	265.58
300	G184	5279	35.58
301	G186	5269	150.58
302	G188	5259	265.58
303	G190	5249	35.58

PAD.	Name	X	Y
304	G192	5239	150.58
305	G194	5229	265.58
306	G196	5219	35.58
307	G198	5209	150.58
308	G200	5199	265.58
309	G202	5189	35.58
310	G204	5179	150.58
311	G206	5169	265.58
312	G208	5159	35.58
313	G210	5149	150.58
314	G212	5139	265.58
315	G214	5129	35.58
316	G216	5119	150.58
317	G218	5109	265.58
318	G220	5099	35.58
319	G222	5089	150.58
320	G224	5079	265.58
321	G226	5069	35.58
322	G228	5059	150.58
323	G230	5049	265.58
324	G232	5039	35.58
325	G234	5029	150.58
326	G236	5019	265.58
327	G238	5009	35.58
328	G240	4999	150.58
329	G242	4989	265.58
330	G244	4979	35.58
331	G246	4969	150.58
332	G248	4959	265.58
333	G250	4949	35.58
334	G252	4939	150.58
335	G254	4929	265.58
336	G256	4919	35.58
337	G258	4909	150.58
338	G260	4899	265.58
339	G262	4889	35.58
340	G264	4879	150.58
341	G266	4869	265.58
342	G268	4859	35.58
343	G270	4849	150.58
344	G272	4839	265.58
345	G274	4829	35.58
346	G276	4819	150.58
347	G278	4809	265.58
348	G280	4799	35.58
349	G282	4789	150.58
350	G284	4779	265.58
351	G286	4769	35.58
352	G288	4759	150.58
353	G290	4749	265.58
354	G292	4739	35.58
355	G294	4729	150.58
356	G296	4719	265.58
357	G298	4709	35.58
358	G300	4699	150.58
359	G302	4689	265.58
360	G304	4679	35.58
361	G306	4669	150.58
362	G308	4659	265.58
363	G310	4649	35.58
364	G312	4639	150.58
365	G314	4629	265.58
366	G316	4619	35.58
367	G318	4609	150.58
368	G320	4599	265.58
369	G322	4589	35.58
370	DUMMY	4579	150.58
371	DUMMY	4569	265.58
372	DUMMY	4559	35.58
373	DUMMY	4549	150.58
374	DUMMY	4539	265.58
375	DUMMY	4529	35.58
376	DUMMY	4519	150.58
377	DUMMY	4509	265.58
378	DUMMY	4499	35.58
379	DUMMY	4489	150.58
380	DUMMY	4479	265.58
381	DUMMY	4469	35.58
382	DUMMY	4459	150.58
383	DUMMY	4449	265.58
384	DUMMY	4439	35.58
385	DUMMY	4429	150.58
386	DUMMY	4419	265.58
387	DUMMY	4409	35.58
388	DUMMY	4399	150.58
389	DUMMY	4389	265.58
390	DUMMY	4379	35.58
391	DUMMY	4369	150.58
392	DUMMY	4359	265.58
393	DUMMY	4349	35.58
394	DUMMY	4339	150.58
395	DUMMY	4329	265.58
396	DUMMY	4319	35.58
397	DUMMY	4309	150.58
398	DUMMY	4299	265.58
399	DUMMY	4289	35.58
400	DUMMY	4279	150.58
401	DUMMY	4269	265.58
402	DUMMY	4259	35.58
403	DUMMY	4249	150.58
404	DUMMY	4239	265.58
405	DUMMY	4229	35.58

PAD.	Name	X	Y
406	DUMMY	4219	150.58
407	DUMMY	4209	265.58
408	DUMMY	4199	35.58
409	DUMMY	4189	150.58
410	DUMMY	4179	265.58
411	DUMMY	4169	35.58
412	DUMMY	4159	150.58
413	DUMMY	4149	265.58
414	DUMMY	4139	35.58
415	DUMMY	4129	150.58
416	DUMMY	4119	265.58
417	DUMMY	4109	35.58
418	DUMMY	4099	150.58
419	DUMMY	4089	265.58
420	DUMMY	4079	35.58
421	DUMMY	4069	150.58
422	DUMMY	4059	265.58
423	DUMMY	4049	35.58
424	DUMMY	4039	150.58
425	DUMMY	4029	265.58
426	DUMMY	4019	35.58
427	DUMMY	4009	150.58
428	DUMMY	3999	265.58
429	DUMMY	3989	35.58
430	DUMMY	3979	150.58
431	DUMMY	3969	265.58
432	DUMMY	3959	35.58
433	DUMMY	3949	150.58
434	DUMMY	3939	265.58
435	DUMMY	3929	35.58
436	DUMMY	3919	150.58
437	DUMMY	3909	265.58
438	DUMMY	3899	35.58
439	DUMMY	3889	150.58
440	DUMMY	3879	265.58
441	DUMMY	3869	35.58
442	DUMMY	3859	150.58
443	DUMMY	3849	265.58
444	DUMMY	3839	35.58
445	DUMMY	3829	150.58
446	DUMMY	3819	265.58
447	DUMMY	3809	35.58
448	DUMMY	3799	150.58
449	DUMMY	3789	265.58
450	DUMMY	3779	35.58
451	DUMMY	3769	150.58
452	DUMMY	3759	265.58
453	VGL	3749	35.58
454	DUMMY	3739	150.58
455	DUMMY	3699	265.58
456	DUMMY	3689	35.58
457	DUMMY	3679	150.58
458	DUMMY	3669	265.58
459	DUMMY	3659	35.58
460	DUMMY	3649	150.58
461	DUMMY	3639	265.58
462	DUMMY	3629	35.58
463	DUMMY	3619	150.58
464	DUMMY	3609	265.58
465	DUMMY	3599	35.58
466	DUMMY	3589	150.58
467	DUMMY	3579	265.58
468	DUMMY	3569	35.58
469	DUMMY	3559	150.58
470	DUMMY	3549	265.58
471	DUMMY	3539	35.58
472	DUMMY	3529	150.58
473	DUMMY	3519	265.58
474	DUMMY	3509	35.58
475	DUMMY	3499	150.58
476	DUMMY	3489	265.58
477	DUMMY	3479	35.58
478	DUMMY	3469	150.58
479	DUMMY	3459	265.58
480	DUMMY	3449	35.58
481	DUMMY	3439	150.58
482	DUMMY	3429	265.58
483	DUMMY	3419	35.58
484	DUMMY	3409	150.58
485	DUMMY	3399	265.58
486	DUMMY	3389	35.58
487	DUMMY	3379	150.58
488	DUMMY	3369	265.58
489	DUMMY	3359	35.58
490	DUMMY	3349	150.58
491	DUMMY	3339	265.58
492	DUMMY	3329	35.58
493	DUMMY	3319	150.58
494	DUMMY	3309	265.58
495	DUMMY	3299	35.58
496	DUMMY	3289	150.58
497	DUMMY	3279	265.58
498	DUMMY	3269	35.58
499	DUMMY	3259	150.58
500	DUMMY	3249	265.58
501	DUMMY	3239	35.58
502	DUMMY	3229	150.58
503	DUMMY	3219	265.58
504	DUMMY	3209	35.58
505	DUMMY	3199	150.58
506	DUMMY	3189	265.58
507	DUMMY	3179	35.58

PAD.	Name	X	Y
508	DUMMY	3169	150.58
509	DUMMY	3159	265.58
510	DUMMY	3149	35.58
511	DUMMY	3139	150.58
512	DUMMY	3129	265.58
513	DUMMY	3119	35.58
514	DUMMY	3109	150.58
515	DUMMY	3099	265.58
516	DUMMY	3089	35.58
517	DUMMY	3079	150.58
518	DUMMY	3069	265.58
519	DUMMY	3059	35.58
520	DUMMY	3049	150.58
521	DUMMY	3039	265.58
522	DUMMY	3029	35.58
523	DUMMY	3019	150.58
524	DUMMY	3009	265.58
525	DUMMY	2999	35.58
526	DUMMY	2989	150.58
527	DUMMY	2979	265.58
528	DUMMY	2969	35.58
529	DUMMY	2959	150.58
530	DUMMY	2949	265.58
531	DUMMY	2939	35.58
532	DUMMY	2929	150.58
533	DUMMY	2919	265.58
534	DUMMY	2909	35.58
535	DUMMY	2899	150.58
536	DUMMY	2889	265.58
537	DUMMY	2879	35.58
538	DUMMY	2869	150.58
539	DUMMY	2859	265.58
540	DUMMY	2849	35.58
541	DUMMY	2839	150.58
542	DUMMY	2829	265.58
543	DUMMY	2819	35.58
544	DUMMY	2809	150.58
545	DUMMY	2799	265.58
546	DUMMY	2789	35.58
547	DUMMY	2779	150.58
548	DUMMY	2769	265.58
549	DUMMY	2759	35.58
550	DUMMY	2749	150.58
551	DUMMY	2739	265.58
552	DUMMY	2729	35.58
553	DUMMY	2719	150.58
554	DUMMY	2709	265.58
555	DUMMY	2699	35.58
556	DUMMY	2689	150.58
557	DUMMY	2679	265.58
558	DUMMY	2669	35.58
559	DUMMY	2659	150.58
560	DUMMY	2649	265.58
561	DUMMY	2639	35.58
562	DUMMY	2629	150.58
563	DUMMY	2619	265.58
564	DUMMY	2609	35.58
565	DUMMY	2599	150.58
566	DUMMY	2589	265.58
567	DUMMY	2579	35.58
568	DUMMY	2569	150.58
569	DUMMY	2559	265.58
570	DUMMY	2549	35.58
571	DUMMY	2539	150.58
572	DUMMY	2529	265.58
573	DUMMY	2519	35.58
574	DUMMY	2509	150.58
575	DUMMY	2499	265.58
576	DUMMY	2489	35.58
577	DUMMY	2479	150.58
578	DUMMY	2469	265.58
579	DUMMY	2459	35.58
580	DUMMY	2449	150.58
581	DUMMY	2439	265.58
582	DUMMY	2429	35.58
583	DUMMY	2419	150.58
584	DUMMY	2409	265.58
585	DUMMY	2399	35.58
586	DUMMY	2389	150.58
587	DUMMY	2379	265.58
588	DUMMY	2369	35.58
589	DUMMY	2359	150.58
590	DUMMY	2349	265.58
591	DUMMY	2339	35.58
592	DUMMY	2329	150.58
593	DUMMY	2319	265.58
594	DUMMY	2309	35.58
595	DUMMY	2299	150.58
596	DUMMY	2289	265.58
597	DUMMY	2279	35.58
598	DUMMY	2269	150.58
599	DUMMY	2259	265.58
600	DUMMY	2249	35.58
601	DUMMY	2239	150.58
602	DUMMY	2229	265.58
603	DUMMY	2219	35.58
604	DUMMY	2209	150.58
605	DUMMY	2199	265.58
606	DUMMY	2189	35.58
607	DUMMY	2179	150.58
608	DUMMY	2169	265.58
609	DUMMY	2159	35.58

PAD.	Name	X	Y
610	DUMMY	2149	150.58
611	DUMMY	2139	265.58
612	DUMMY	2129	35.58
613	DUMMY	2119	150.58
614	DUMMY	2109	265.58
615	DUMMY	2099	35.58
616	DUMMY	2089	150.58
617	DUMMY	2079	265.58
618	DUMMY	2069	35.58
619	DUMMY	2059	150.58
620	DUMMY	2049	265.58
621	DUMMY	2039	35.58
622	DUMMY	2029	150.58
623	DUMMY	2019	265.58
624	DUMMY	2009	35.58
625	DUMMY	1999	150.58
626	DUMMY	1989	265.58
627	DUMMY	1979	35.58
628	DUMMY	1969	150.58
629	DUMMY	1959	265.58
630	DUMMY	1949	35.58
631	DUMMY	1939	150.58
632	DUMMY	1929	265.58
633	DUMMY	1919	35.58
634	DUMMY	1909	150.58
635	DUMMY	1899	265.58
636	DUMMY	1889	35.58
637	DUMMY	1879	150.58
638	DUMMY	1869	265.58
639	DUMMY	1859	35.58
640	DUMMY	1849	150.58
641	DUMMY	1839	265.58
642	DUMMY	1829	35.58
643	DUMMY	1819	150.58
644	DUMMY	1809	265.58
645	DUMMY	1799	35.58
646	DUMMY	1789	150.58
647	DUMMY	1779	265.58
648	DUMMY	1769	35.58
649	DUMMY	1759	150.58
650	DUMMY	1749	265.58
651	DUMMY	1739	35.58
652	DUMMY	1729	150.58
653	DUMMY	1719	265.58
654	DUMMY	1709	35.58
655	DUMMY	1699	150.58
656	DUMMY	1689	265.58
657	DUMMY	1679	35.58
658	DUMMY	1669	150.58
659	DUMMY	1659	265.58
660	DUMMY	1649	35.58
661	DUMMY	1639	150.58
662	DUMMY	1629	265.58
663	DUMMY	1619	35.58
664	DUMMY	1609	150.58
665	DUMMY	1599	265.58
666	DUMMY	1589	35.58
667	DUMMY	1579	150.58
668	DUMMY	1569	265.58
669	DUMMY	1559	35.58
670	DUMMY	1549	150.58
671	DUMMY	1539	265.58
672	DUMMY	1529	35.58
673	DUMMY	1519	150.58
674	DUMMY	1509	265.58
675	DUMMY	1499	35.58
676	DUMMY	1489	150.58
677	DUMMY	1479	265.58
678	DUMMY	1469	35.58
679	DUMMY	1459	150.58
680	DUMMY	1449	265.58
681	DUMMY	1439	35.58
682	DUMMY	1429	150.58
683	DUMMY	1419	265.58
684	S264	1409	35.58
685	S263	1399	150.58
686	S262	1389	265.58
687	S261	1379	35.58
688	S260	1369	150.58
689	S259	1359	265.58
690	S258	1349	35.58
691	S257	1339	150.58
692	S256	1329	265.58
693	S255	1319	35.58
694	S254	1309	150.58
695	S253	1299	265.58
696	S252	1289	35.58
697	S251	1279	150.58
698	S250	1269	265.58
699	S249	1259	35.58
700	S248	1249	150.58
701	S247	1239	265.58
702	S246	1229	35.58
703	S245	1219	150.58
704	S244	1209	265.58
705	S243	1199	35.58
706	S242	1189	150.58
707	S241	1179	265.58
708	S240	1169	35.58
709	S239	1159	150.58
710	S238	1149	265.58
711	S237	1139	35.58

PAD.	Name	X	Y
712	S236	1129	150.58
713	S235	1119	265.58
714	S234	1109	35.58
715	S233	1099	150.58
716	S232	1089	265.58
717	S231	1079	35.58
718	S230	1069	150.58
719	S229	1059	265.58
720	S228	1049	35.58
721	S227	1039	150.58
722	S226	1029	265.58
723	S225	1019	35.58
724	S224	1009	150.58
725	S223	999	265.58
726	S222	989	35.58
727	S221	979	150.58
728	S220	969	265.58
729	S219	959	35.58
730	S218	949	150.58
731	S217	939	265.58
732	S216	929	35.58
733	S215	919	150.58
734	S214	909	265.58
735	S213	899	35.58
736	S212	889	150.58
737	S211	879	265.58
738	S210	869	35.58
739	S209	859	150.58
740	S208	849	265.58
741	S207	839	35.58
742	S206	829	150.58
743	S205	819	265.58
744	S204	809	35.58
745	S203	799	150.58
746	S202	789	265.58
747	S201	779	35.58
748	S200	769	150.58
749	S199	759	265.58
750	S198	749	35.58
751	S197	739	150.58
752	S196	729	265.58
753	S195	719	35.58
754	S194	709	150.58
755	S193	699	265.58
756	S192	689	35.58
757	S191	679	150.58
758	S190	669	265.58
759	S189	659	35.58
760	S188	649	150.58
761	S187	639	265.58
762	S186	629	35.58
763	S185	619	150.58
764	S184	609	265.58
765	S183	599	35.58
766	S182	589	150.58
767	S181	579	265.58
768	S180	569	35.58
769	S179	559	150.58
770	S178	549	265.58
771	S177	539	35.58
772	S176	529	150.58
773	S175	519	265.58
774	S174	509	35.58
775	S173	499	150.58
776	S172	489	265.58
777	S171	479	35.58
778	S170	469	150.58
779	S169	459	265.58
780	S168	449	35.58
781	S167	439	150.58
782	S166	429	265.58
783	S165	419	35.58
784	S164	409	150.58
785	S163	399	265.58
786	S162	389	35.58
787	S161	379	150.58
788	S160	369	265.58
789	S159	359	35.58
790	S158	349	150.58
791	S157	339	265.58
792	S156	329	35.58
793	S155	319	150.58
794	S154	309	265.58
795	S153	299	35.58
796	S152	289	150.58
797	S151	279	265.58
798	S150	269	35.58
799	S149	259	150.58
800	S148	249	265.58
801	S147	239	35.58
802	S146	229	150.58
803	S145	219	265.58
804	S144	209	35.58
805	S143	199	150.58
806	S142	189	265.58
807	S141	179	35.58
808	S140	169	150.58
809	S139	159	265.58
810	S138	149	35.58
811	S137	139	150.58
812	S136	129	265.58
813	S135	119	35.58

PAD.	Name	X	Y
814	S134	109	150.58
815	S133	99	265.58
816	DUMMY	89	35.58
817	DUMMY	79	150.58
818	GTest	69	265.58
819	DUMMY	59	35.58
820	GTest	49	150.58
821	S132	-99	35.58
822	S131	-109	150.58
823	S130	-119	265.58
824	S129	-129	35.58
825	S128	-139	150.58
826	S127	-149	265.58
827	S126	-159	35.58
828	S125	-169	150.58
829	S124	-179	265.58
830	S123	-189	35.58
831	S122	-199	150.58
832	S121	-209	265.58
833	S120	-219	35.58
834	S119	-229	150.58
835	S118	-239	265.58
836	S117	-249	35.58
837	S116	-259	150.58
838	S115	-269	265.58
839	S114	-279	35.58
840	S113	-289	150.58
841	S112	-299	265.58
842	S111	-309	35.58
843	S110	-319	150.58
844	S109	-329	265.58
845	S108	-339	35.58
846	S107	-349	150.58
847	S106	-359	265.58
848	S105	-369	35.58
849	S104	-379	150.58
850	S103	-389	265.58
851	S102	-399	35.58
852	S101	-409	150.58
853	S100	-419	265.58
854	S99	-429	35.58
855	S98	-439	150.58
856	S97	-449	265.58
857	S96	-459	35.58
858	S95	-469	150.58
859	S94	-479	265.58
860	S93	-489	35.58
861	S92	-499	150.58
862	S91	-509	265.58
863	S90	-519	35.58
864	S89	-529	150.58
865	S88	-539	265.58
866	S87	-549	35.58
867	S86	-559	150.58
868	S85	-569	265.58
869	S84	-579	35.58
870	S83	-589	150.58
871	S82	-599	265.58
872	S81	-609	35.58
873	S80	-619	150.58
874	S79	-629	265.58
875	S78	-639	35.58
876	S77	-649	150.58
877	S76	-659	265.58
878	S75	-669	35.58
879	S74	-679	150.58
880	S73	-689	265.58
881	S72	-699	35.58
882	S71	-709	150.58
883	S70	-719	265.58
884	S69	-729	35.58
885	S68	-739	150.58
886	S67	-749	265.58
887	S66	-759	35.58
888	S65	-769	150.58
889	S64	-779	265.58
890	S63	-789	35.58
891	S62	-799	150.58
892	S61	-809	265.58
893	S60	-819	35.58
894	S59	-829	150.58
895	S58	-839	265.58
896	S57	-849	35.58
897	S56	-859	150.58
898	S55	-869	265.58
899	S54	-879	35.58
900	S53	-889	150.58
901	S52	-899	265.58
902	S51	-909	35.58
903	S50	-919	150.58
904	S49	-929	265.58
905	S48	-939	35.58
906	S47	-949	150.58
907	S46	-959	265.58
908	S45	-969	35.58
909	S44	-979	150.58
910	S43	-989	265.58
911	S42	-999	35.58
912	S41	-1009	150.58
913	S40	-1019	265.58
914	S39	-1029	35.58
915	S38	-1039	150.58

PAD.	Name	X	Y
916	S37	-1049	265.58
917	S36	-1059	35.58
918	S35	-1069	150.58
919	S34	-1079	265.58
920	S33	-1089	35.58
921	S32	-1099	150.58
922	S31	-1109	265.58
923	S30	-1119	35.58
924	S29	-1129	150.58
925	S28	-1139	265.58
926	S27	-1149	35.58
927	S26	-1159	150.58
928	S25	-1169	265.58
929	S24	-1179	35.58
930	S23	-1189	150.58
931	S22	-1199	265.58
932	S21	-1209	35.58
933	S20	-1219	150.58
934	S19	-1229	265.58
935	S18	-1239	35.58
936	S17	-1249	150.58
937	S16	-1259	265.58
938	S15	-1269	35.58
939	S14	-1279	150.58
940	S13	-1289	265.58
941	S12	-1299	35.58
942	S11	-1309	150.58
943	S10	-1319	265.58
944	S9	-1329	35.58
945	S8	-1339	150.58
946	S7	-1349	265.58
947	S6	-1359	35.58
948	S5	-1369	150.58
949	S4	-1379	265.58
950	S3	-1389	35.58
951	S2	-1399	150.58
952	S1	-1409	265.58
953	DUMMY	-1419	35.58
954	DUMMY	-1429	150.58
955	DUMMY	-1439	265.58
956	DUMMY	-1449	35.58
957	DUMMY	-1459	150.58
958	DUMMY	-1469	265.58
959	DUMMY	-1479	35.58
960	DUMMY	-1489	150.58
961	DUMMY	-1499	265.58
962	DUMMY	-1509	35.58
963	DUMMY	-1519	150.58
964	DUMMY	-1529	265.58
965	DUMMY	-1539	35.58
966	DUMMY	-1549	150.58
967	DUMMY	-1559	265.58
968	DUMMY	-1569	35.58
969	DUMMY	-1579	150.58
970	DUMMY	-1589	265.58
971	DUMMY	-1599	35.58
972	DUMMY	-1609	150.58
973	DUMMY	-1619	265.58
974	DUMMY	-1629	35.58
975	DUMMY	-1639	150.58
976	DUMMY	-1649	265.58
977	DUMMY	-1659	35.58
978	DUMMY	-1669	150.58
979	DUMMY	-1679	265.58
980	DUMMY	-1689	35.58
981	DUMMY	-1699	150.58
982	DUMMY	-1709	265.58
983	DUMMY	-1719	35.58
984	DUMMY	-1729	150.58
985	DUMMY	-1739	265.58
986	DUMMY	-1749	35.58
987	DUMMY	-1759	150.58
988	DUMMY	-1769	265.58
989	DUMMY	-1779	35.58
990	DUMMY	-1789	150.58
991	DUMMY	-1799	265.58
992	DUMMY	-1809	35.58
993	DUMMY	-1819	150.58
994	DUMMY	-1829	265.58
995	DUMMY	-1839	35.58
996	DUMMY	-1849	150.58
997	DUMMY	-1859	265.58
998	DUMMY	-1869	35.58
999	DUMMY	-1879	150.58
1000	DUMMY	-1889	265.58
1001	DUMMY	-1899	35.58
1002	DUMMY	-1909	150.58
1003	DUMMY	-1919	265.58
1004	DUMMY	-1929	35.58
1005	DUMMY	-1939	150.58
1006	DUMMY	-1949	265.58
1007	DUMMY	-1959	35.58
1008	DUMMY	-1969	150.58
1009	DUMMY	-1979	265.58
1010	DUMMY	-1989	35.58
1011	DUMMY	-1999	150.58
1012	DUMMY	-2009	265.58
1013	DUMMY	-2019	35.58
1014	DUMMY	-2029	150.58
1015	DUMMY	-2039	265.58
1016	DUMMY	-2049	35.58
1017	DUMMY	-2059	150.58

PAD.	Name	X	Y
1018	DUMMY	-2069	265.58
1019	DUMMY	-2079	35.58
1020	DUMMY	-2089	150.58
1021	DUMMY	-2099	265.58
1022	DUMMY	-2109	35.58
1023	DUMMY	-2119	150.58
1024	DUMMY	-2129	265.58
1025	DUMMY	-2139	35.58
1026	DUMMY	-2149	150.58
1027	DUMMY	-2159	265.58
1028	DUMMY	-2169	35.58
1029	DUMMY	-2179	150.58
1030	DUMMY	-2189	265.58
1031	DUMMY	-2199	35.58
1032	DUMMY	-2209	150.58
1033	DUMMY	-2219	265.58
1034	DUMMY	-2229	35.58
1035	DUMMY	-2239	150.58
1036	DUMMY	-2249	265.58
1037	DUMMY	-2259	35.58
1038	DUMMY	-2269	150.58
1039	DUMMY	-2279	265.58
1040	DUMMY	-2289	35.58
1041	DUMMY	-2299	150.58
1042	DUMMY	-2309	265.58
1043	DUMMY	-2319	35.58
1044	DUMMY	-2329	150.58
1045	DUMMY	-2339	265.58
1046	DUMMY	-2349	35.58
1047	DUMMY	-2359	150.58
1048	DUMMY	-2369	265.58
1049	DUMMY	-2379	35.58
1050	DUMMY	-2389	150.58
1051	DUMMY	-2399	265.58
1052	DUMMY	-2409	35.58
1053	DUMMY	-2419	150.58
1054	DUMMY	-2429	265.58
1055	DUMMY	-2439	35.58
1056	DUMMY	-2449	150.58
1057	DUMMY	-2459	265.58
1058	DUMMY	-2469	35.58
1059	DUMMY	-2479	150.58
1060	DUMMY	-2489	265.58
1061	DUMMY	-2499	35.58
1062	DUMMY	-2509	150.58
1063	DUMMY	-2519	265.58
1064	DUMMY	-2529	35.58
1065	DUMMY	-2539	150.58
1066	DUMMY	-2549	265.58
1067	DUMMY	-2559	35.58
1068	DUMMY	-2569	150.58
1069	DUMMY	-2579	265.58
1070	DUMMY	-2589	35.58
1071	DUMMY	-2599	150.58
1072	DUMMY	-2609	265.58
1073	DUMMY	-2619	35.58
1074	DUMMY	-2629	150.58
1075	DUMMY	-2639	265.58
1076	DUMMY	-2649	35.58
1077	DUMMY	-2659	150.58
1078	DUMMY	-2669	265.58
1079	DUMMY	-2679	35.58
1080	DUMMY	-2689	150.58
1081	DUMMY	-2699	265.58
1082	DUMMY	-2709	35.58
1083	DUMMY	-2719	150.58
1084	DUMMY	-2729	265.58
1085	DUMMY	-2739	35.58
1086	DUMMY	-2749	150.58
1087	DUMMY	-2759	265.58
1088	DUMMY	-2769	35.58
1089	DUMMY	-2779	150.58
1090	DUMMY	-2789	265.58
1091	DUMMY	-2799	35.58
1092	DUMMY	-2809	150.58
1093	DUMMY	-2819	265.58
1094	DUMMY	-2829	35.58
1095	DUMMY	-2839	150.58
1096	DUMMY	-2849	265.58
1097	DUMMY	-2859	35.58
1098	DUMMY	-2869	150.58
1099	DUMMY	-2879	265.58
1100	DUMMY	-2889	35.58
1101	DUMMY	-2899	150.58
1102	DUMMY	-2909	265.58
1103	DUMMY	-2919	35.58
1104	DUMMY	-2929	150.58
1105	DUMMY	-2939	265.58
1106	DUMMY	-2949	35.58
1107	DUMMY	-2959	150.58
1108	DUMMY	-2969	265.58
1109	DUMMY	-2979	35.58
1110	DUMMY	-2989	150.58
1111	DUMMY	-2999	265.58
1112	DUMMY	-3009	35.58
1113	DUMMY	-3019	150.58
1114	DUMMY	-3029	265.58
1115	DUMMY	-3039	35.58
1116	DUMMY	-3049	150.58
1117	DUMMY	-3059	265.58
1118	DUMMY	-3069	35.58
1119	DUMMY	-3079	150.58

PAD.	Name	X	Y
1120	DUMMY	-3089	265.58
1121	DUMMY	-3099	35.58
1122	DUMMY	-3109	150.58
1123	DUMMY	-3119	265.58
1124	DUMMY	-3129	35.58
1125	DUMMY	-3139	150.58
1126	DUMMY	-3149	265.58
1127	DUMMY	-3159	35.58
1128	DUMMY	-3169	150.58
1129	DUMMY	-3179	265.58
1130	DUMMY	-3189	35.58
1131	DUMMY	-3199	150.58
1132	DUMMY	-3209	265.58
1133	DUMMY	-3219	35.58
1134	DUMMY	-3229	150.58
1135	DUMMY	-3239	265.58
1136	DUMMY	-3249	35.58
1137	DUMMY	-3259	150.58
1138	DUMMY	-3269	265.58
1139	DUMMY	-3279	35.58
1140	DUMMY	-3289	150.58
1141	DUMMY	-3299	265.58
1142	DUMMY	-3309	35.58
1143	DUMMY	-3319	150.58
1144	DUMMY	-3329	265.58
1145	DUMMY	-3339	35.58
1146	DUMMY	-3349	150.58
1147	DUMMY	-3359	265.58
1148	DUMMY	-3369	35.58
1149	DUMMY	-3379	150.58
1150	DUMMY	-3389	265.58
1151	DUMMY	-3399	35.58
1152	DUMMY	-3409	150.58
1153	DUMMY	-3419	265.58
1154	DUMMY	-3429	35.58
1155	DUMMY	-3439	150.58
1156	DUMMY	-3449	265.58
1157	DUMMY	-3459	35.58
1158	DUMMY	-3469	150.58
1159	DUMMY	-3479	265.58
1160	DUMMY	-3489	35.58
1161	DUMMY	-3499	150.58
1162	DUMMY	-3509	265.58
1163	DUMMY	-3519	35.58
1164	DUMMY	-3529	150.58
1165	DUMMY	-3539	265.58
1166	DUMMY	-3549	35.58
1167	DUMMY	-3559	150.58
1168	DUMMY	-3569	265.58
1169	DUMMY	-3579	35.58
1170	DUMMY	-3589	150.58
1171	DUMMY	-3599	265.58
1172	DUMMY	-3609	35.58
1173	DUMMY	-3619	150.58
1174	DUMMY	-3629	265.58
1175	DUMMY	-3639	35.58
1176	DUMMY	-3649	150.58
1177	DUMMY	-3659	265.58
1178	DUMMY	-3669	35.58
1179	DUMMY	-3679	150.58
1180	DUMMY	-3689	265.58
1181	VGL	-3739	35.58
1182	DUMMY	-3749	150.58
1183	DUMMY	-3759	265.58
1184	DUMMY	-3769	35.58
1185	DUMMY	-3779	150.58
1186	DUMMY	-3789	265.58
1187	DUMMY	-3799	35.58
1188	DUMMY	-3809	150.58
1189	DUMMY	-3819	265.58
1190	DUMMY	-3829	35.58
1191	DUMMY	-3839	150.58
1192	DUMMY	-3849	265.58
1193	DUMMY	-3859	35.58
1194	DUMMY	-3869	150.58
1195	DUMMY	-3879	265.58
1196	DUMMY	-3889	35.58
1197	DUMMY	-3899	150.58
1198	DUMMY	-3909	265.58
1199	DUMMY	-3919	35.58
1200	DUMMY	-3929	150.58
1201	DUMMY	-3939	265.58
1202	DUMMY	-3949	35.58
1203	DUMMY	-3959	150.58
1204	DUMMY	-3969	265.58
1205	DUMMY	-3979	35.58
1206	DUMMY	-3989	150.58
1207	DUMMY	-3999	265.58
1208	DUMMY	-4009	35.58
1209	DUMMY	-4019	150.58
1210	DUMMY	-4029	265.58
1211	DUMMY	-4039	35.58
1212	DUMMY	-4049	150.58
1213	DUMMY	-4059	265.58
1214	DUMMY	-4069	35.58
1215	DUMMY	-4079	150.58
1216	DUMMY	-4089	265.58
1217	DUMMY	-4099	35.58
1218	DUMMY	-4109	150.58
1219	DUMMY	-4119	265.58
1220	DUMMY	-4129	35.58
1221	DUMMY	-4139	150.58

PAD.	Name	X	Y
1222	DUMMY	-4149	265.58
1223	DUMMY	-4159	35.58
1224	DUMMY	-4169	150.58
1225	DUMMY	-4179	265.58
1226	DUMMY	-4189	35.58
1227	DUMMY	-4199	150.58
1228	DUMMY	-4209	265.58
1229	DUMMY	-4219	35.58
1230	DUMMY	-4229	150.58
1231	DUMMY	-4239	265.58
1232	DUMMY	-4249	35.58
1233	DUMMY	-4259	150.58
1234	DUMMY	-4269	265.58
1235	DUMMY	-4279	35.58
1236	DUMMY	-4289	150.58
1237	DUMMY	-4299	265.58
1238	DUMMY	-4309	35.58
1239	DUMMY	-4319	150.58
1240	DUMMY	-4329	265.58
1241	DUMMY	-4339	35.58
1242	DUMMY	-4349	150.58
1243	DUMMY	-4359	265.58
1244	DUMMY	-4369	35.58
1245	DUMMY	-4379	150.58
1246	DUMMY	-4389	265.58
1247	DUMMY	-4399	35.58
1248	DUMMY	-4409	150.58
1249	DUMMY	-4419	265.58
1250	DUMMY	-4429	35.58
1251	DUMMY	-4439	150.58
1252	DUMMY	-4449	265.58
1253	DUMMY	-4459	35.58
1254	DUMMY	-4469	150.58
1255	DUMMY	-4479	265.58
1256	DUMMY	-4489	35.58
1257	DUMMY	-4499	150.58
1258	DUMMY	-4509	265.58
1259	DUMMY	-4519	35.58
1260	DUMMY	-4529	150.58
1261	DUMMY	-4539	265.58
1262	DUMMY	-4549	35.58
1263	DUMMY	-4559	150.58
1264	DUMMY	-4569	265.58
1265	DUMMY	-4579	35.58
1266	G321	-4589	150.58
1267	G319	-4599	265.58
1268	G317	-4609	35.58
1269	G315	-4619	150.58
1270	G313	-4629	265.58
1271	G311	-4639	35.58
1272	G309	-4649	150.58
1273	G307	-4659	265.58
1274	G305	-4669	35.58
1275	G303	-4679	150.58
1276	G301	-4689	265.58
1277	G299	-4699	35.58
1278	G297	-4709	150.58
1279	G295	-4719	265.58
1280	G293	-4729	35.58
1281	G291	-4739	150.58
1282	G289	-4749	265.58
1283	G287	-4759	35.58
1284	G285	-4769	150.58
1285	G283	-4779	265.58
1286	G281	-4789	35.58
1287	G279	-4799	150.58
1288	G277	-4809	265.58
1289	G275	-4819	35.58
1290	G273	-4829	150.58
1291	G271	-4839	265.58
1292	G269	-4849	35.58
1293	G267	-4859	150.58
1294	G265	-4869	265.58
1295	G263	-4879	35.58
1296	G261	-4889	150.58
1297	G259	-4899	265.58
1298	G257	-4909	35.58
1299	G255	-4919	150.58
1300	G253	-4929	265.58
1301	G251	-4939	35.58
1302	G249	-4949	150.58
1303	G247	-4959	265.58
1304	G245	-4969	35.58
1305	G243	-4979	150.58
1306	G241	-4989	265.58
1307	G239	-4999	35.58
1308	G237	-5009	150.58
1309	G235	-5019	265.58
1310	G233	-5029	35.58
1311	G231	-5039	150.58
1312	G229	-5049	265.58
1313	G227	-5059	35.58
1314	G225	-5069	150.58
1315	G223	-5079	265.58
1316	G221	-5089	35.58
1317	G219	-5099	150.58
1318	G217	-5109	265.58
1319	G215	-5119	35.58
1320	G213	-5129	150.58
1321	G211	-5139	265.58
1322	G209	-5149	35.58
1323	G207	-5159	150.58

PAD.	Name	X	Y
1324	G205	-5169	265.58
1325	G203	-5179	35.58
1326	G201	-5189	150.58
1327	G199	-5199	265.58
1328	G197	-5209	35.58
1329	G195	-5219	150.58
1330	G193	-5229	265.58
1331	G191	-5239	35.58
1332	G189	-5249	150.58
1333	G187	-5259	265.58
1334	G185	-5269	35.58
1335	G183	-5279	150.58
1336	G181	-5289	265.58
1337	G179	-5299	35.58
1338	G177	-5309	150.58
1339	G175	-5319	265.58
1340	G173	-5329	35.58
1341	G171	-5339	150.58
1342	G169	-5349	265.58
1343	G167	-5359	35.58
1344	G165	-5369	150.58
1345	G163	-5379	265.58
1346	G161	-5389	35.58
1347	G159	-5399	150.58
1348	G157	-5409	265.58
1349	G155	-5419	35.58
1350	G153	-5429	150.58
1351	G151	-5439	265.58
1352	G149	-5449	35.58
1353	G147	-5459	150.58
1354	G145	-5469	265.58
1355	G143	-5479	35.58
1356	G141	-5489	150.58
1357	G139	-5499	265.58
1358	G137	-5509	35.58
1359	G135	-5519	150.58
1360	G133	-5529	265.58
1361	G131	-5539	35.58
1362	G129	-5549	150.58
1363	G127	-5559	265.58
1364	G125	-5569	35.58
1365	G123	-5579	150.58
1366	G121	-5589	265.58
1367	G119	-5599	35.58
1368	G117	-5609	150.58
1369	G115	-5619	265.58
1370	G113	-5629	35.58
1371	G111	-5639	150.58
1372	G109	-5649	265.58
1373	G107	-5659	35.58
1374	G105	-5669	150.58
1375	G103	-5679	265.58
1376	G101	-5689	35.58
1377	G99	-5699	150.58
1378	G97	-5709	265.58
1379	G95	-5719	35.58
1380	G93	-5729	150.58
1381	G91	-5739	265.58
1382	G89	-5749	35.58
1383	G87	-5759	150.58
1384	G85	-5769	265.58
1385	G83	-5779	35.58
1386	G81	-5789	150.58
1387	G79	-5799	265.58
1388	G77	-5809	35.58
1389	G75	-5819	150.58
1390	G73	-5829	265.58
1391	G71	-5839	35.58
1392	G69	-5849	150.58
1393	G67	-5859	265.58
1394	G65	-5869	35.58
1395	G63	-5879	150.58
1396	G61	-5889	265.58
1397	G59	-5899	35.58
1398	G57	-5909	150.58
1399	G55	-5919	265.58
1400	G53	-5929	35.58
1401	G51	-5939	150.58
1402	G49	-5949	265.58
1403	G47	-5959	35.58
1404	G45	-5969	150.58
1405	G43	-5979	265.58
1406	G41	-5989	35.58
1407	G39	-5999	150.58
1408	G37	-6009	265.58
1409	G35	-6019	35.58
1410	G33	-6029	150.58
1411	G31	-6039	265.58
1412	G29	-6049	35.58
1413	G27	-6059	150.58
1414	G25	-6069	265.58
1415	G23	-6079	35.58
1416	G21	-6089	150.58
1417	G19	-6099	265.58
1418	G17	-6109	35.58
1419	G15	-6119	150.58
1420	G13	-6129	265.58
1421	G11	-6139	35.58
1422	G9	-6149	150.58
1423	G7	-6159	265.58
1424	G5	-6169	35.58
1425	G3	-6179	150.58

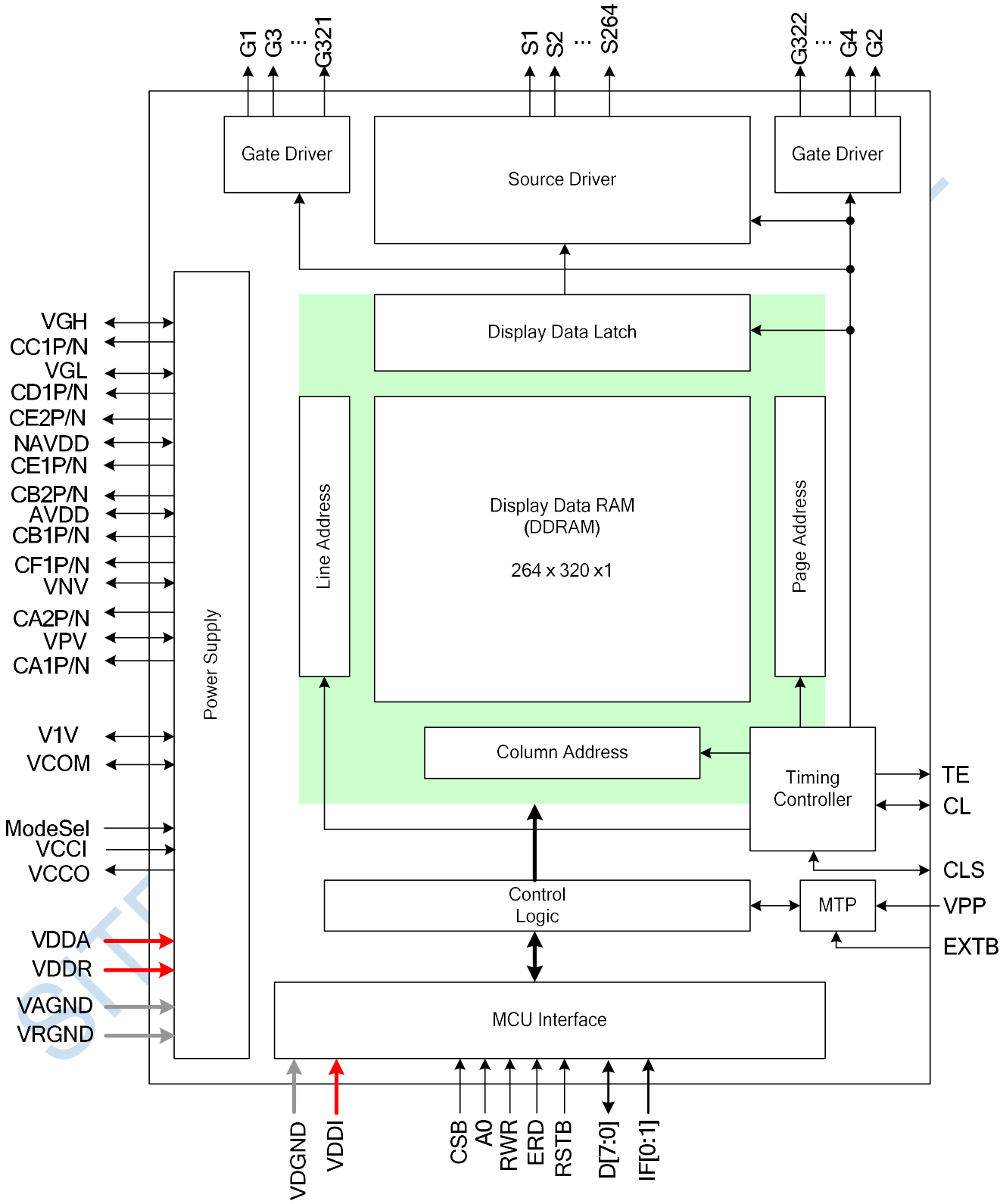
PAD.	Name	X	Y
1426	G1	-6189	265.58
1427	DUMMY	-6199	35.58
1428	GTest	-6209	150.58

PAD.	Name	X	Y
1429	GTest	-6219	265.58
1430	DUMMY	-6229	35.58
1431	DUMMY	-6239	150.58

PAD.	Name	X	Y
Mark	ALIGN_L	-6146	-275
Mark	ALIGN_R	6154	-275

Unit: um

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power supply Pin

Name	Type	Description
VDDI	Power	Power Supply (Digital)
VDDA	Power	Power Supply (Analog)
VDDR	Power	Power Supply (Reference)
VCCI/VCCO	Power	VCCI is the power source of digital circuits. VCCO is the VCC output. VCCI and VCCO should be connected together.
ModeSel	I	Power Mode Selection. ModeSel = “VAGND”: 1.8V mode (VDDI=VDDA=1.8V) ModeSel = “VDDA”: Normal mode (VDDI=1.8V~3.6V ; VDDA=2.55~3.6V)
VDGND	Power	Ground (Digital)
VAGND	Power	Ground (Analog)
VRGND	Power	Ground (Reference)

6.2 Digital I/O

Name	Type	Description
RSTB	I	Reset input pin. When RSTB is “L”, internal initialization procedure is executed.
IF[1:0]	I	These pins select interface operation mode. IF1 / IF0 / MPU interface type: L / L / 8-bit 8080 parallel interface L / H / Single 4-line serial interface H / L / Dual 4-line serial interface H / H / 3-line serial interface
CSB	I	Chip select input pin. CSB=“L”: This chip is selected and the MPU interface is active. CSB=“H”: This chip is not selected and the MPU interface is disabled (D[7:0] are high impedance).
A0	I	**When using 8080, Single 4SPI and Dual 4SPI mode.** It determines whether the access is related to data or command. A0 = "H": Indicates that D[7:0] are display data; A0 = "L": Indicates that D[7:0] are control data. **When using 3SPI.** There is no A0 pin in 3-Line. A0 should be fixed to “H” by VDDI.

Name	Type	Description
RWR	I	**When using 8080** Write enable in 8080 parallel interface. **When using Dual 4SPI** Second data lane in Dual 4SPI interface. This pin is not used in 3-Line and Single 4-Line SPI. RWR should be connected to VDDI
ERD	I	Read enable in 8080 interface. This pin is not used in serial interfaces and should be connected to VDDI.
D[7:0]	I/O	**When using 8-bit parallel interface: 8080 mode** 8 bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor. When CSB is “H”, D[7:0] are high impedance.
	I/O	**When using serial interface: Single/Dual 4-line SPI, 3-line SPI** D[7:4] : fix to “H” by VDDI. D[3:2] : serial output data (SDA_OUT). D[1] : serial input data (SDA_IN). D[0] : serial input clock (SCLK). **D1 to D3 must be connected together (SDA)** When CSB is “H”, D[7:0] are high impedance.
TE	O	Tearing effect signal is used to synchronize MCU to frame memory writing. If not used, please let this pin open.

Note:

1. After VDDI is turned ON, all MPU interface pins should not be left OPEN.

6.3 Clock System Input

Name	Type	Description
CLS	I	Clock source selection pin. CLS="H": enable internal clock. CLS="L": disable internal clock and use external clock.
CL	I/O	For external clock. If CLS="H": this pin is open. If CLS="L": this pin is the input of oscillator.

6.4 Driving Output Pin

Name	Type	Description
S1 to S264	O	Source driver output pins.
G1 to G322	O	Gate driver output pins.
VPV VNV V1V AVDD NAVDD	O	Power output pin for analog circuit.
VGH	O	Power output (positive) pin for gate driver.
VGL	O	Power output (negative) pin for gate driver.
VCOM	O	COM outputs. A power supply for the TFT-LCD common electrode. **Must be connected to GND of FPC.**
CA1P/N CA2P/N	O	Capacitor connecting pins for step-up circuit. (for VPV)
CB1P/N CB2P/N	O	Capacitor connecting pins for step-up circuit. (for AVDD)
CC1P/N	O	Capacitor connecting pins for step-up circuit. (for VGH)
CD1P/N	O	Capacitor connecting pins for step-up circuit. (for VGL)
CE1P/N CE2P/N	O	Capacitor connecting pins for step-up circuit. (for NAVDD)
CF1P/N	O	Capacitor connecting pins for step-up circuit. (for VNV)

6.5 MTP Pin

Name	Type	Description
VPP	Power	The programming power supply of the built-in NVM. Apply external power 7.5V here when programming (> 8mA for successful programming). If not used, left this pin open.
EXTB	I	EXTB="L": Enable the extension operation mode. When programming MTP, connect EXTB to VDGND externally. This pin has an internal pull-high resistor. Please leave this pin OPEN after special operation.

6.6 Others

Name	Type	Description
VTEST TESTENB TESTA TESTB GTest DUMMY MTest[5:0]	O	Reserved for test only. Please leave these pins open.

6.7 Recommend Resistance

Item	Pin name	Resistance
Powers	VDDA, VAGND	< 3 ohm
	VCCO, VCCI	< 20 ohm
	VDDI, VDGND, VDDR, VRGND	< 50 ohm
Driving Output	CAxN/P, VPV, VNV, AVDD	< 3 ohm
	CBxN/P, CF1N/P	< 5 ohm
	V1V, CExP/N, NAVDD	< 10 ohm
	CC1N/P, VGH, CD1N/P, VGL	< 20 ohm
	VCOM	< 50 ohm
Digital	D[7:0], CSB, RSTB, A0, RWR, ERD	< 100 ohm
	IF[1:0], CLS, CL, TE, EXTB, TESTB, TESTA, ModeSel	< 200 ohm
MTP	VPP	< 10 ohm

7 FUNCTION DESCRIPTION

ST7305 supports 8-bit parallel data bus for 8080 series CPU, 3-line and single/dual 4-line interface.

7.1 Microprocessor Interface

7.1.1 Chip Select Input

CSB pin is used for chip selection. This driver can interface with an MPU when CSB is "L". If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 4-Line and 3-Line serial interface, the internal shift register and serial counter are reset when CSB is “H”.

7.1.2 Interface Selection

The interface selection is controlled by IF[1:0] pins. Please refer to the table below:

Table 1 Parallel/Serial Interface Mode

Setting		MCU Type	Interface Pin Function				
IF1	IF0		CSB	A0	RWR	ERD	D[7:0]
L	L	8-bit 8080 Parallel interface	CSB	A0	/WR	/RD	D[7:0]
L	H	Single 4-line serial interface			-	-	D[0]=SCL, D[1:3]=SDA, D[4:7]= -
H	L	Dual 4-line serial interface			SDA2		
H	H	3-line serial interface		-	-	-	

Note: The un-used pins are marked as “-” and should be connected to “H” by VDDI.

7.1.3 8080 Parallel Interface

ST7305 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig1. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Fig2. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

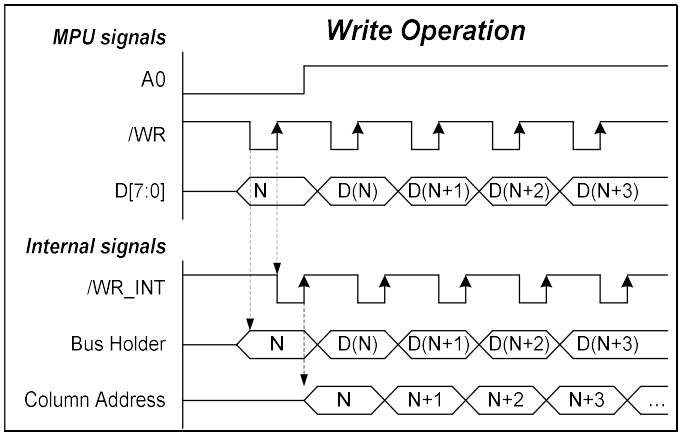


Fig1. Data Transfer: Write

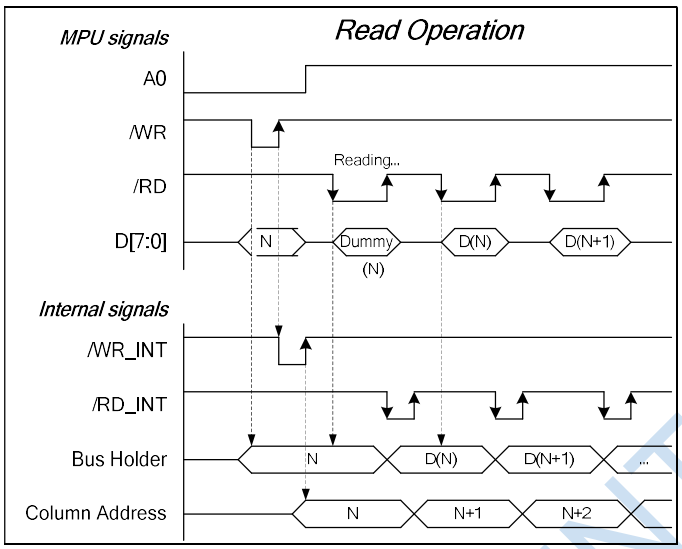
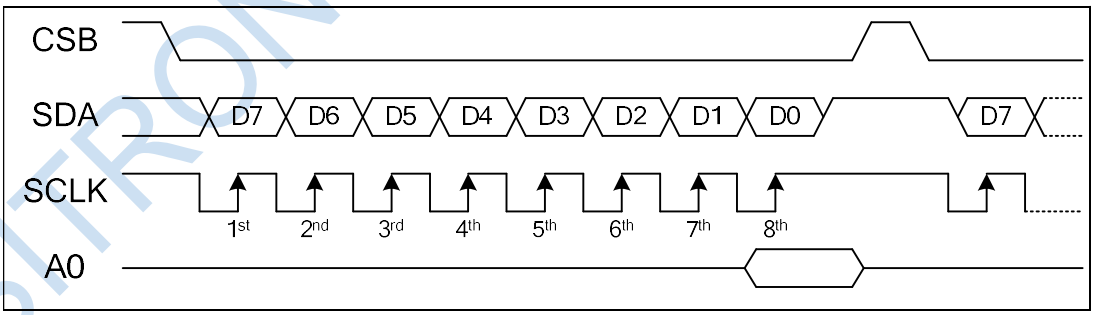


Fig2. Data Transfer: Read

7.1.4 Single 4-Line Serial Interface

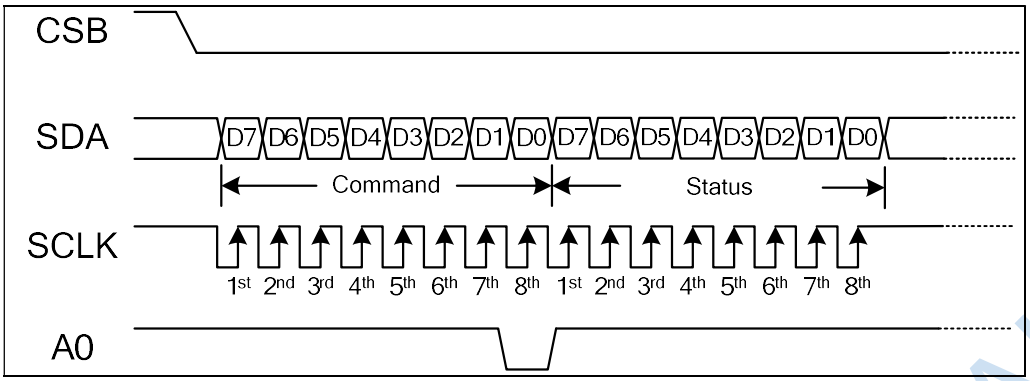
ST7305 is active when CSB is “L”, serial data (SDA) and serial clock (SCLK) inputs are enabled. When CSB is “H”, ST7305 is not active, the internal 8-bit shift register and 3-bit counter are reset. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCLK). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.



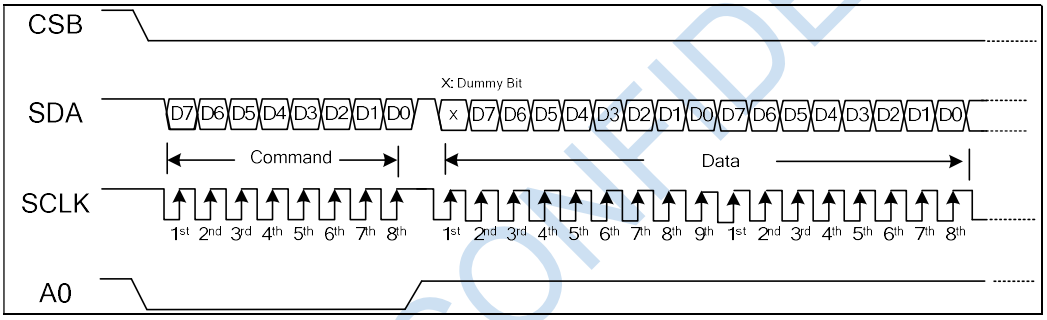
Write Operation of 4-Line SPI

After entering the “Read Status” instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.



Read Status Operation of 4-Line SPI

After entering the “Memory Read” instruction to read data, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. And when reading data from on-chip-RAM to the MCU, the first data bit will be dummy .



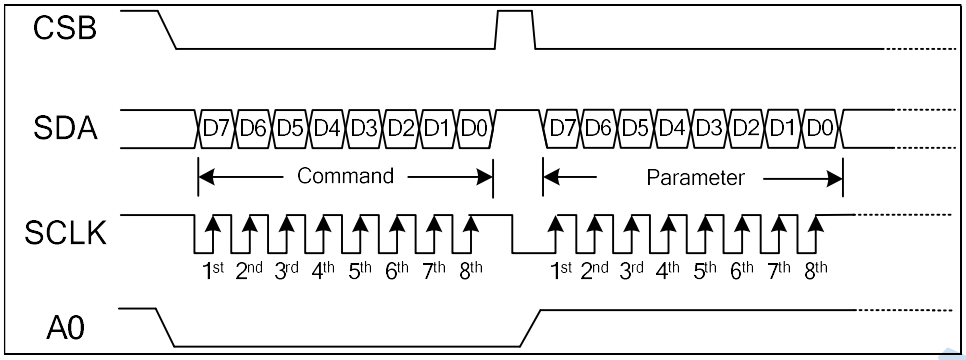
Read RAM Operation of 4-Line SPI Interface

7.1.5 Dual 4-Line Serial Interface

Dual 4-line serial interface use: CSB (chip enable), SCLK (serial clock), SDA (serial data input/output 1), RWR (serial data input 2) and A0.

Command write mode:

The command write protocol of dual 4-line serial interface is the same with the single 4-line serial interface. The display data/command indication is controlled by the register selection pin (A0). Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSB is high. In this state, SCLK clock pulse or SDA data have no effect. A falling edge on CSB enables the serial interface and indicates the start of data transmission.

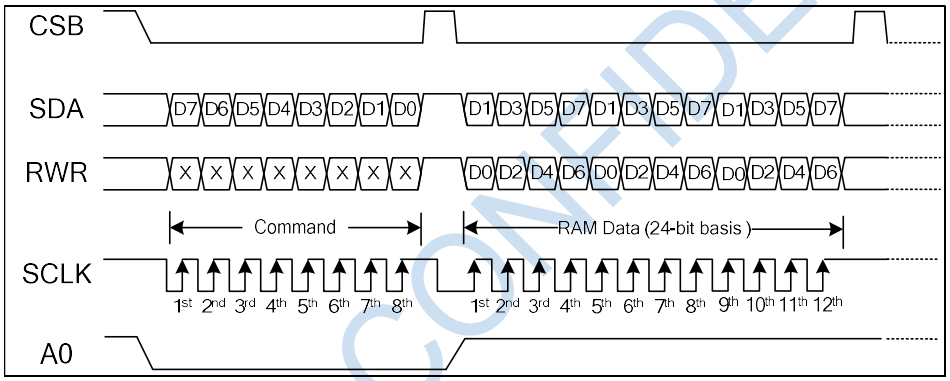


Command Write Operation of Dual 4-Line SPI

RAM write mode:

The RAM write mode of dual 4-line serial interface need use SDA pin and RWR pin to be data input pins.

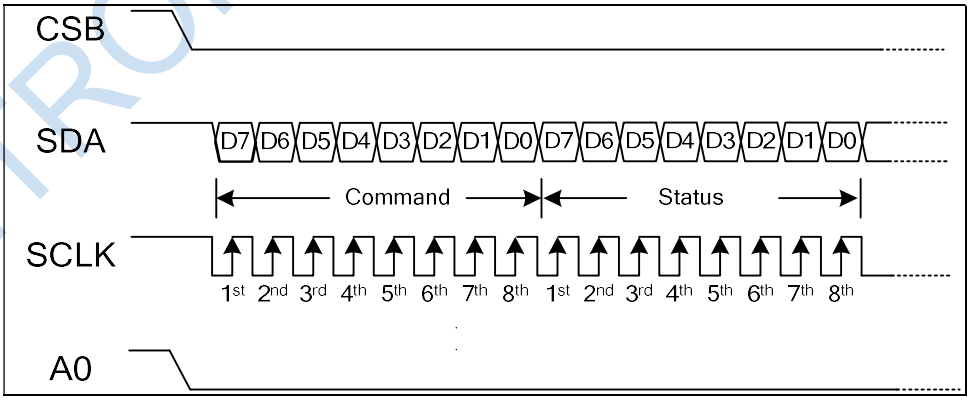
The LSB is transmitted first and the data bit will be exchanged between SDA and RWR.



RAM Write Operation of Dual 4-Line SPI

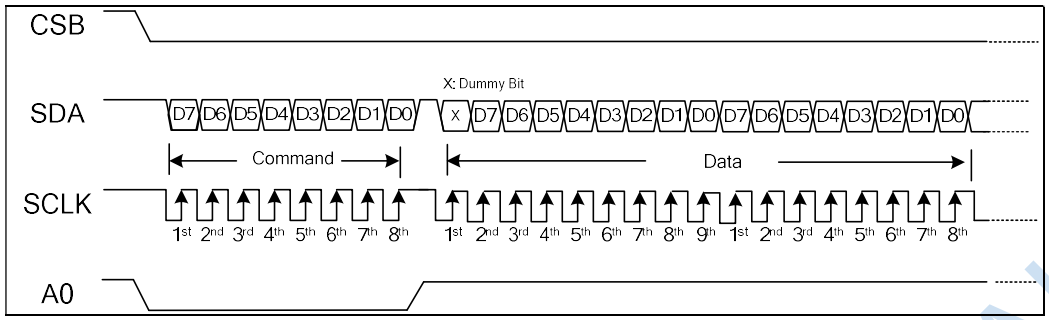
Read protocol for dual 4-line serial interface:

Read protocol (for RDID1/RDID2/RDID3 command: 8-bit read):



Read Status Operation of Dual 4-Line SPI Interface

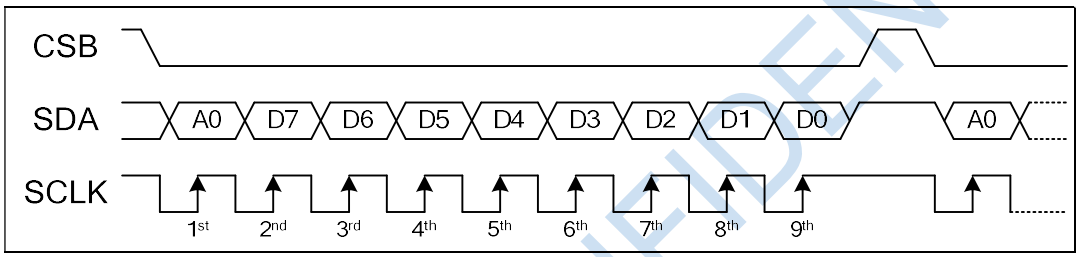
Read protocol (for RAM Data: 8-bit read):



Read RAM Operation of Dual 4-Line SPI Interface

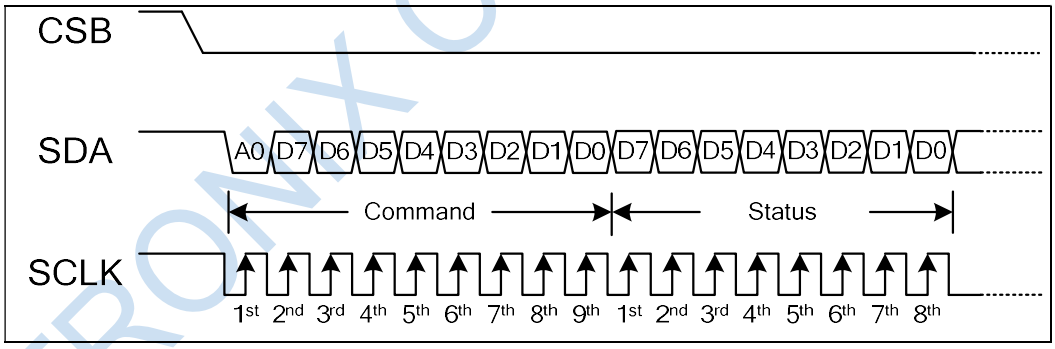
7.1.6 3-Line Serial Interface

In 3-Line interface, A0 pin is not available. The 1st output bit defines command byte or parameter byte.

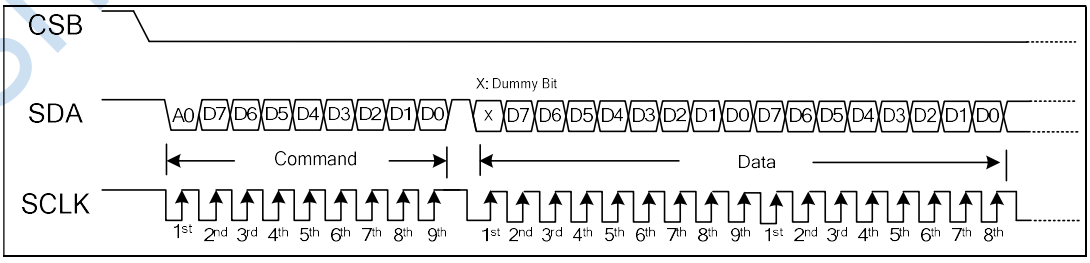


Write Operation of 3-Line SPI

After entering the “Read Status” instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.



Read Status Operation of 3-Line SPI



Read RAM Operation of 3-Line SPI Interface

7.2 Data Color Coding

Use specific command for switching between data input modes.

7.2.1 Data Input Mode

(1) 8080/Single 4SPI/3SPI Interface

TYPE1: There are 4 write operations for 24-bit data. (Set by “BPS=0” of command 0x3Ah)

Command	A0	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
1st write	1	P1	P2	P3	P4	P5	P6	-	-
2nd write	1	P7	P8	P9	P10	P11	P12	-	-
3rd write	1	P13	P14	P15	P16	P17	P18	-	-
4th write	1	P19	P20	P21	P22	P23	P24	-	-

Note: - don’t care

TYPE2: There are 3 write operations for 24-bit data. (Set by “BPS=1” of command 0x3Ah)

Command	A0	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
1st write	1	P1	P2	P3	P4	P5	P6	P7	P8
2nd write	1	P9	P10	P11	P12	P13	P14	P15	P16
3rd write	1	P17	P18	P19	P20	P21	P22	P23	P24

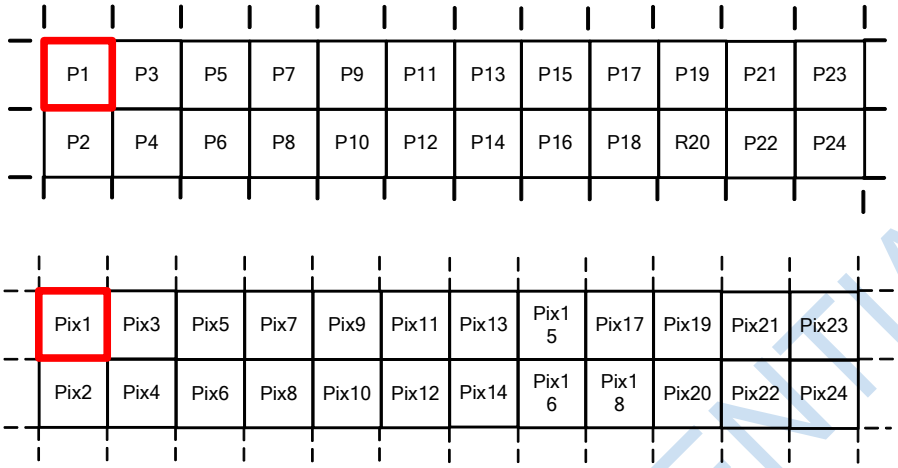
(2) Dual 4SP Interface

There are 3 write operations for 24-bit data at the same time.

Command	A0	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
1st write	1	P1	P2	P3	P4	P5	P6	P7	P8
2nd write	1	P9	P10	P11	P12	P13	P14	P15	P16
3rd write	1	P17	P18	P19	P20	P21	P22	P23	P24

7.2.2 Data to Display Mapping

The data mapping of mono display is as below.



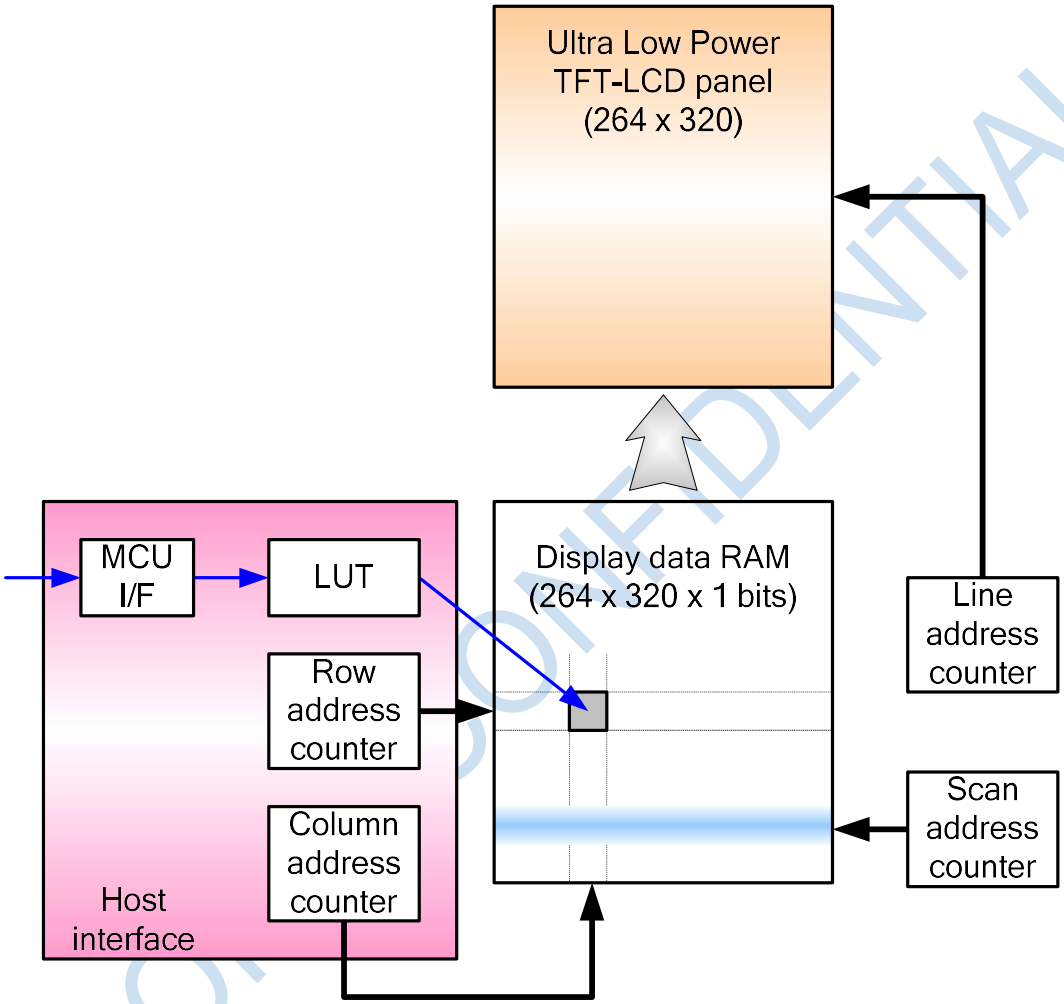
7.2.3 Memory to Display Address Mapping

PA		19											..	40											NOR	CA
NOR	INV	40											..	19											INV	
0	159	P1	P3	P5	P7	P9	P11	P13	P15	P17	P19	P21	P23	..												L1
		P2	P4	P6	P8	P10	P12	P14	P16	P18	P20	P22	P24	..												L2
1	159																									L3
																										L4
:	:	:	:	:														:	:	:						:
158	1																									L317
																										L318
159	0																									L319
																										L320
Source		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	..	S253	S254	S255	S256	S257	S258	S259	S260	S261	S262	S263	S264	Line

7.3 Display Data RAM

7.3.1 Configuration

The display module has an integrated 264 x 320 x 1b graphic type static RAM. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and interface Read or Write to the same location of the Frame Memory.



7.4 Address Control

The address counter sets the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The locations of RAM are addressed by the address pointers. The address ranges are X=19(13h) to X=40 (28h) and Y=0 to Y=159 (9Fh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=19 (13h) YS=0 (0h) and XE=40 (28h), YE=159 (9Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 7.4 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below

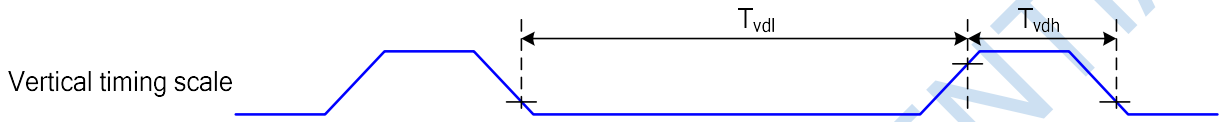
Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

7.5 Tearing Effect

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.5.1 Tearing effect line modes

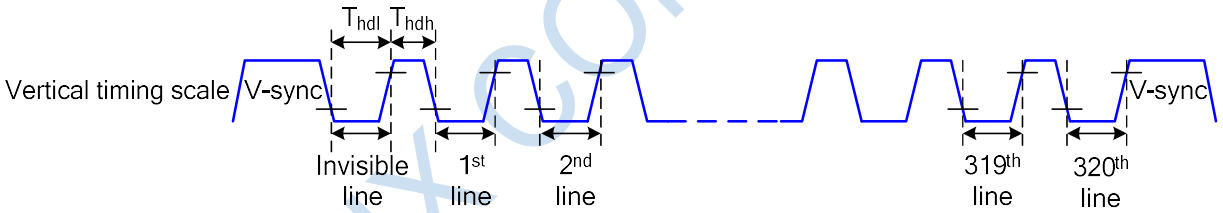
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

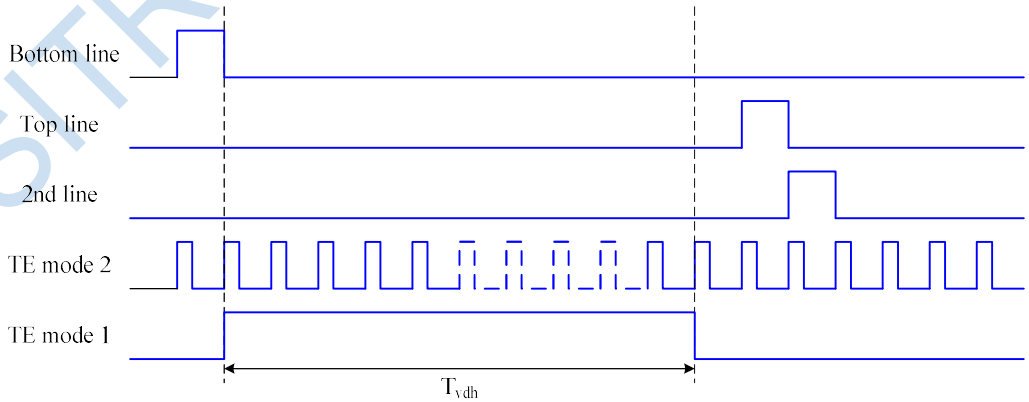
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

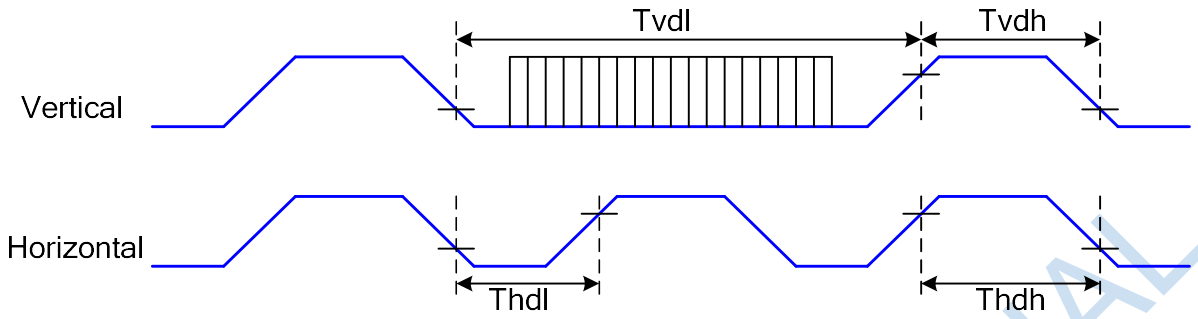
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

7.5.2 Tearing effect line timings

The Tearing Effect signal is described below:



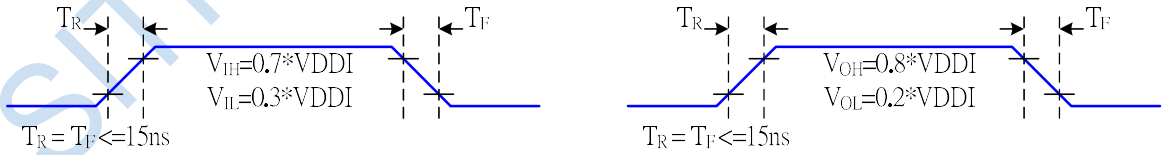
Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	30	-	ms	
tvdh	Vertical Timing High Duration	1.2	-	ms	
thdl	Horizontal Timing Low Duration	31.2	-	µs	
thdh	Horizontal Timing Low Duration	31.2	-	µs	

AC characteristics of Tearing Effect Signal HPM Mode (Frame Rate = 32 Hz, Ta=25°C)

Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	990.5	-	ms	
tvdh	Vertical Timing High Duration	9.5	-	ms	
thdl	Horizontal Timing Low Duration	250	-	µs	
thdh	Horizontal Timing Low Duration	250	-	µs	

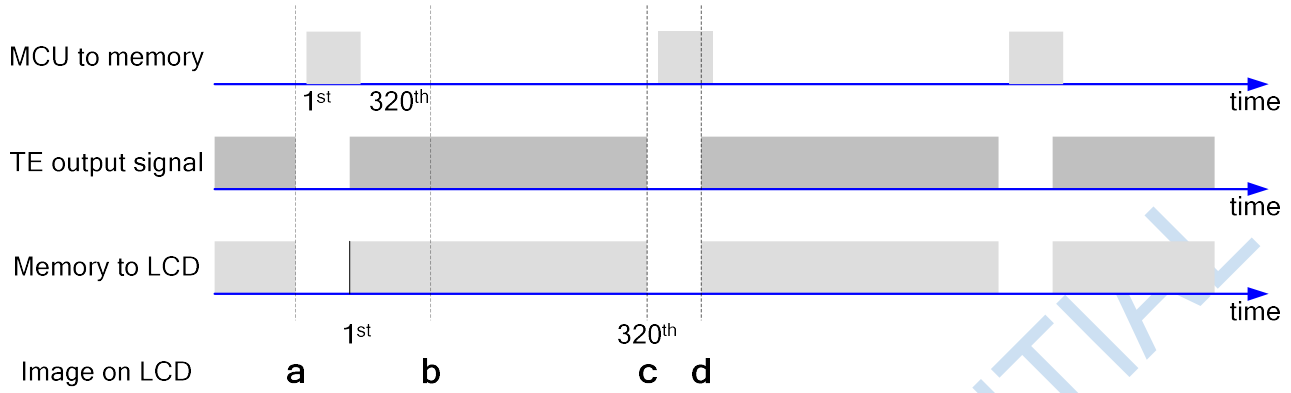
AC characteristics of Tearing Effect Signal LPM Mode (Frame Rate = 1 Hz, Ta=25°C)

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

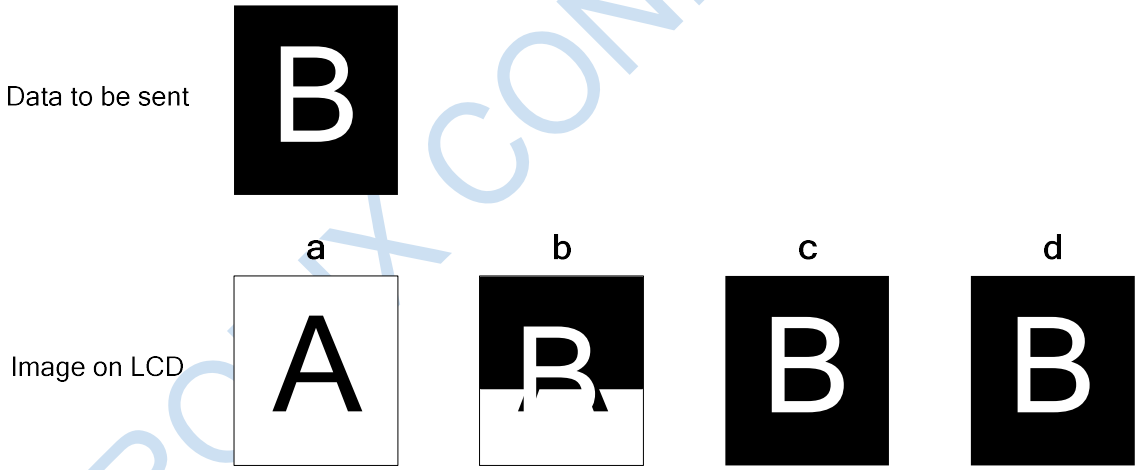


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

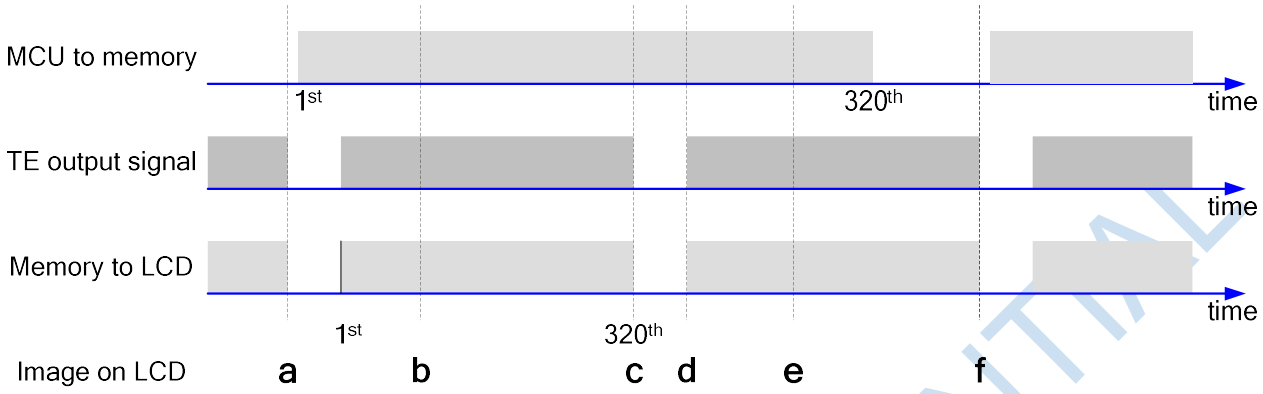
7.5.3 Example 1: MPU Write is faster than panel read



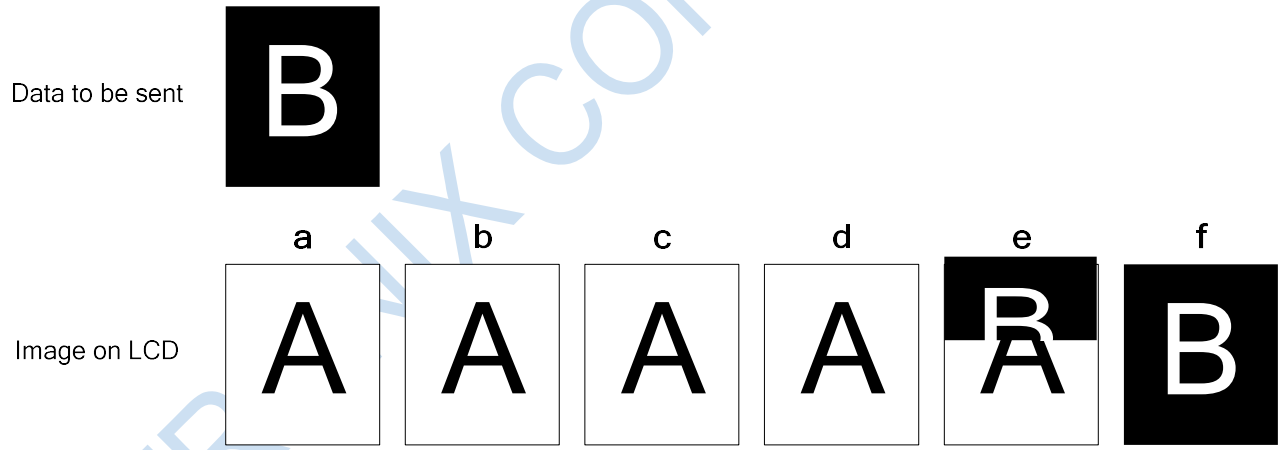
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



7.5.4 Example 2: MPU write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



7.6 Oscillation Circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, connect CLS to VDDI;

when the external oscillator is used, connect CLS to VSS and input external clock to CL pin. This oscillator signal is used by the voltage booster and display timing generation circuit.

7.7 Reset

Setting RSTB pin to “L” (hardware reset) can initialize internal function. Generally, VDDI is not stable at the time that the system power is just turned ON. The hardware reset or software reset is required to initialize internal registers after VDDI is stable. Initialization by RSTB pin or command SWRESET is essential before operating.

7.8 Power ON/OFF Sequence

VDDI and VDDA can be applied in any order.

VDDA and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down minimum 120msec after RSTB has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after RSTB has been released.

CSB can be applied at any timing or can be permanently grounded. RSTB has priority over CSB.

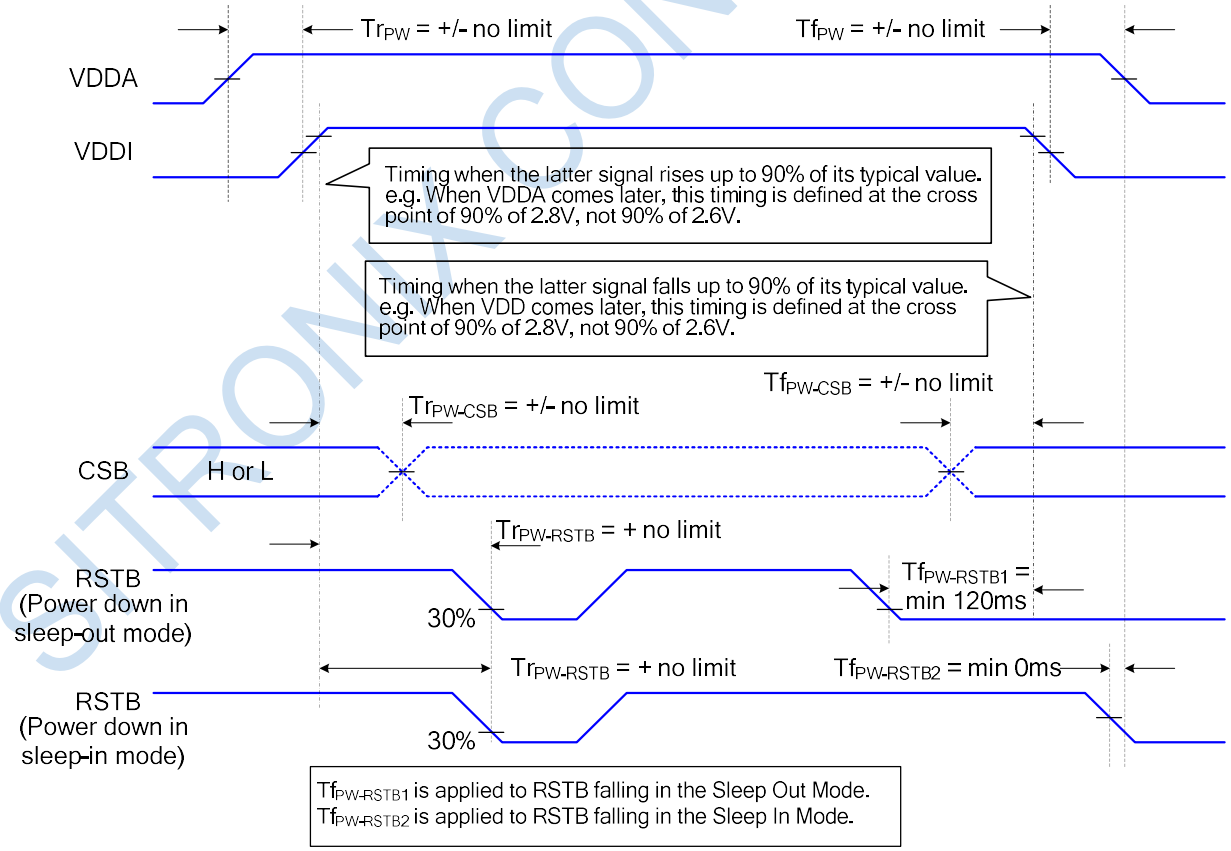
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

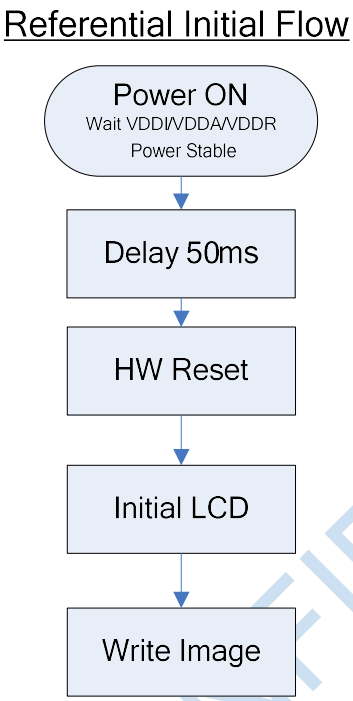
Note 4: If RSTB line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RSTB) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



7.9 Referential Initial Setup Flow

7.9.1 Initial Setting Flow



7.9.2 Referential Initial Code

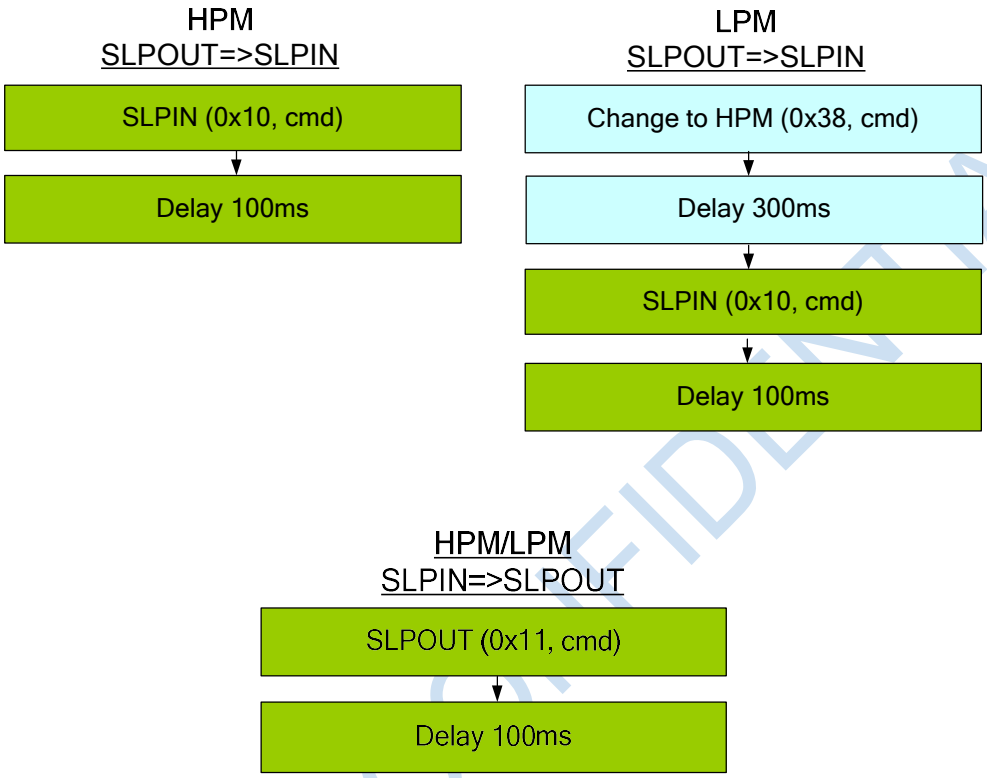
```
Void Initialization_ST7305(void)
 {
        Write(Command, 0xD6);          // NVM Load Control
        Write(Data, 0x17);
        Write(Data, 0x02);
        Write(Command, 0xD1);          //Booster Enable
        Write(Data, 0x01);
        Write(Command, 0xC0);          //Gate Voltage Control
        Write(Data, 0x0E)               // VGH=15V
        Write(Data, 0x0A)               // VGL=-10V
        Write(Command, 0xC1);          //VSHP Setting
        Write(Data, 0x41);             //VSHP1=5V
        Write(Data, 0x41);             //VSHP2=5V
        Write(Data, 0x41);             //VSHP3=5V
        Write(Data, 0x41);             //VSHP4=5V
        Write(Command, 0xC2);          //VSLP Setting
        Write(Data, 0x32);             //VSLP1=1V
```

```
Write(Data, 0x32);          //VSLP2=1V
Write(Data, 0x32);          //VSLP3=1V
Write(Data, 0x32);          //VSLP4=1V
Write(Command, 0xC4);       //VSHN Setting
Write(Data, 0x46);          //VSHN1=-3.9V
Write(Data, 0x46);          //VSHN2=-3.9V
Write(Data, 0x46);          //VSHN3=-3.9V
Write(Data, 0x46);          //VSHN4=-3.9V
Write(Command, 0xC5);       //VSLN Setting
Write(Data, 0x46);          //VSLN1=-0.4V
Write(Data, 0x46);          //VSLN2=-0.4V
Write(Data, 0x46);          //VSLN3=-0.4V
Write(Data, 0x46);          //VSLN4=-0.4V
Write(Command, 0xB2);       //Frame Rate Control
Write(Data, 0x12);          //HPM=32Hz ; LPM=1Hz

Write(Command, 0xB3);       //Update Period Gate EQ Control in HPM
Write(Data, 0xE5);
Write(Data, 0xF6);
Write(Data, 0x05);          //HPM EQ Control
Write(Data, 0x46);
Write(Data, 0x77);
Write(Data, 0x77);
Write(Data, 0x77);
Write(Data, 0x77);
Write(Data, 0x76);
Write(Data, 0x45);
Write(Command, 0xB4);       //Update Period Gate EQ Control in LPM
Write(Data, 0x05);          //LPM EQ Control
Write(Data, 0x46);
Write(Data, 0x77);
Write(Data, 0x77);
Write(Data, 0x77);
Write(Data, 0x77);
Write(Data, 0x76);
Write(Data, 0x45);
```

```
        Write(Command, 0xB7);       //Source EQ Enable
        Write(Data, 0x13);
        Write(Command, 0xB0);       //Gate Line Setting
        Write(Data, 0x50);          //320 line
        Write(Command, 0x11);       //Sleep-out
        Delay_ms (120);

        Write(Command, 0xD8);       //OSC Setting
        Write(Data, 0x80);          //51Hz
        Write(Data, 0xE9);
        Write(Command, 0xC9);       //Source Voltage Select
        Write(Data, 0x00);          //VSHP1; VSLP1 ; VSHN1 ; VSLN1
        Write(Command, 0x36);       //Memory Data Access Control
        Write(Data, 0x48);
        Write(Command, 0x3A);       //Data Format Select
        Write(Data, 0x10);
        Write(Command, 0xB9);       //Gamma Mode Setting
        Write(Data, 0x20);          // Mono
        Write(Command, 0xB8);       //Panel Setting
        Write(Data, 0x00);          // 2line interlace and 2line panel layout
        Write(Command, 0x2A);       //Column Address Setting
        Write(Data, 0x13);
        Write(Data, 0x28);
        Write(Command, 0x2B);       //Row Address Setting
        Write(Data, 0x00);
        Write(Data, 0x9F);
        Write(Command, 0x35);       //TE Setting
        Write(Data, 0x00);
        Write(Command, 0xD0);       //Enable Auto Power down
        Write(Data, 0xFF);
        Write(Command, 0x39);       //LPM ON
        Write(Command, 0x29);       //Display ON
}
```

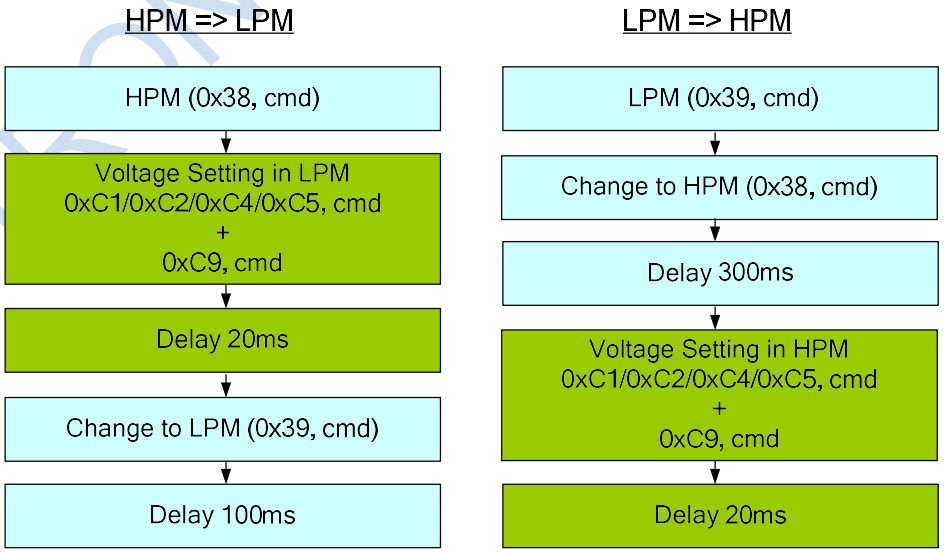
7.10 Sleep-In/Out Sequence

Sleep-in/out mode can be used to save power when display function is not required. To enter or exit from Sleep-in/out mode, refer to the following sequence.



7.11 Power Mode (HPM/LPM) Sequence

To switch between HPM and LPM, follow the sequences below.



8 COMMAND

8.1 Command Table1

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1. NOP	0	↑	1	0	0	0	0	0	0	0	0	(00h)	No operation
2.SWRESET	0	↑	1	0	0	0	0	0	0	0	1	(01h)	Software reset
3.RDDID	0	↑	1	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
4.RDDST	0	↑	1	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑	BSTON	MY	MX	MV	0	GS	DO	0		Display status1
	1	1	↑	0	XDE	0	BPS	LPM	PTLON	SLOUT	NORON		Display status2
	1	1	↑	VSON	0	INVON	0	0	DISON	TEON	0		Display status3
5.RDDPM	0	↑	1	0	0	0	0	1	0	1	0	(0Ah)	Read display Power Mode
	1	1	↑	BSTON	LPM	PTLON	SLPOUT	NORON	DISON	0	0		Display Power Status
6.SLPIN	0	↑	1	0	0	0	1	0	0	0	0	(10h)	Sleep in
7.SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	(11h)	Sleep out
8.PTLON	0	↑	1	0	0	0	1	0	0	1	0	(12h)	Partial on (240 duty set)
9.PTLOFF	0	↑	1	0	0	0	1	0	0	1	1	(13h)	Partial off (320 duty set)
10.INVOFF	0	↑	1	0	0	1	0	0	0	0	0	(20h)	Display inversion off
11.INVON	0	↑	1	0	0	1	0	0	0	0	1	(21h)	Display inversion on
12.DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	(28h)	Display off
13.DISPON	0	↑	1	0	0	1	0	1	0	0	1	(29h)	Display on
14.CASET	0	↑	1	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	0	0	XS5	XS4	XS3	XS2	XS1	XS0		X address start: 19≦XS≦X
	1	↑	1	0	0	XE5	XE4	XE3	XE2	XE1	XE0		X address end S≦XE≦X
15.RASET	0	↑	1	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		Y address start: 0≦YS≦Y
	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		Y address end: S≦YE≦Y
16.RAMWR	0	↑	1	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
17.RAMRD	0	↑	1	0	0	1	0	1	1	1	0	(2Eh)	Memory read
	1	1	↑	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
18.TEOFF	0	↑	1	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
19.TEON	0	↑	1	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	1	0	0	0	0	0	0	0	TEM		
20.MADCTL	0	↑	1	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	MY	MX	MV	0	DO	GS	0	0		
21.VSCSAD	0	↑	1	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	1	0	0	0	0	0	0	0	VSP8		
	1	↑	1	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
22.HPM	0	↑	1	0	0	1	1	1	0	0	0	(38h)	High power mode
23.LPM	0	↑	1	0	0	1	1	1	0	0	1	(39h)	Low power mode
24.DTFORM	0	↑	1	0	0	1	1	1	0	1	0	(3Ah)	Data format select
	1	↑	1	0	0	0	XDE	0	0	0	BPS		
25.RAMWRC	0	↑	1	0	0	1	1	1	1	0	0	(3Ch)	Write memory continue
	1	↑	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
26.RAMRD	0	↑	1	0	0	1	1	1	1	1	0	(3Eh)	Memory read
	1	1	↑	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	↑	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
27.TESCAN	0	↑	1	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	1	0	0	0	0	0	0	0	N8		
	1	↑	1	N7	N6	N5	N4	N3	N2	N1	N0		
28.RDID1	0	↑	1	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
29.RDID2	0	↑	1	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
30,RDID3	0	↑	1	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

"-": Don't care

8.1.1 NOP (00h)

00H	NOP (No Operation)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter											
Description	This command is empty command.											

8.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter-											
Description	-The display module performs a software reset, registers are written with their SW reset default values. -Frame memory contents are unaffected by this command.											
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command. Software reset command cannot be sent during sleep out sequence.											

8.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	0	0	0	0	0	1	0	0	(04h)
1st parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
2nd parameter	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
3rd parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	-This read byte returns 24-bit display identification information. -The 1st parameter (ID17 to ID10): LCD module's manufacturer ID. -The 2nd parameter (ID26 to ID20): LCD module/driver version ID -The 3rd parameter (ID37 to UD30): LCD module/driver ID. -Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 1,2,3 of the command 04h, respectively.											
Default Value (D7 to D0)	1st parameter= 0x00h 2nd parameter =0x00h 3rd parameter = 0x00h											

8.1.4 RDDST (09h): Read Display Status

09H	RDDST(Read Display Status)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	0	0	0	0	1	0	0	1	(09h)
1st parameter	1	1	↑	BSTON	MY	MX	MV	0	GS	DO	0	
2nd parameter	1	1	↑	0	XDE	0	BPS	LPM	PTLON	SLOUT	NORON	
3rd parameter	1	1	↑	VSON	0	INVON	0	0	DISON	TEON	0	

Description

- This command indicates the current status of the display as described in the table below

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, (when BSTEN (D1h) D0='1') '0' =Booster off, (when BSTEN (D1h) D0='0')
MY	Row Address Order	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
MV	Row/Column Exchange	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')
DO	Data Order	'0' =Left to right (When MADCTL (36h) D3='1') '1' = Right to left (When MADCTL (36h) D3='0', using in MX=1)
GS	Gate Scan Order	'0' = Data refresh Top to Bottom (when MADCTL (36h) D2='0') '1' = Data refresh Bottom to Top (when MADCTL (36h) D2='1')
XDE	Data Up Down Switch	'0' = Switch ON(when DTFORM (3Ah) D4='1', Using with MY=1) '1' = Switch OFF (when DTFORM (3Ah) D4='0')
BPS	Bytes Per Pixel Select	'0' = 4 writes operations for 24-bit data (when DTFORM (3Ah) D0='0') '1' = 3 writes operations for 24-bit data (when DTFORM (3Ah) D0='1')
LPM	Power Mode Select	'0' = HPM, '1' = LPM
PTLON	Partial Mode ON/OFF	'0' = OFF, '1' = ON
SLPOUT	Sleep In/Out	'0' = In, '1' = Out
NORON	Display Normal Mode On/Off	'0' = Scroll or Partial ON, '1' = Normal,
VSON	Scroll Mode On/Off	'0' = Off, '1' = On
INVON	Inversion Status	'0' = Normal, '1' = Inverse
DISON	Display On/Off	'1' = On, "0" = Off
TEON	Tearing effect line on/off	'1' = On, "0" = Off

Default Value: 1st parameter= 0x00h

(D7 to D0)	2nd parameter =0x40h 3rd parameter = 0x00h

8.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	0	0	0	0	1	0	1	0	(0Ah)
Parameter	1	1	↑	BSTON	LPM	PTLON	SLPOUT	NORON	DISON	0	0	

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, (when BSTEN (D1h) D0='1') '0' =Booster off, (when BSTEN (D1h) D0='0')
LPM	Power Mode Select	'0' = High Power Mode, '1' = Low Power Mode
PTLON	Partial Mode ON/OFF	'0' = OFF, '1' = ON
SLPOUT	Sleep In/Out	'0' = In, '1' = Out
NORON	Display Normal Mode On/Off	'0' = Scroll or Partial ON, '1' = Normal,
DISON	Display On/Off	'1' = On, "0" = Off

Default Value (D7 to D0)	0x08h

8.1.6 SLPIN (10h): Sleep in

10H	SLPIN (Sleep In)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	↑	1	0	0	0	1	0	0	0	0	(10h)
Parameter	No Parameter											
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped. -MCU interface and memory are still working and the memory keeps its contents.											
Restriction	-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 100msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.											

8.1.7 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	(11h)
Parameter	No Parameter											
Description	-This command turn off sleep mode. -In this mode the DC/DC converter is enable, internal display oscillator is started, and panel scanning is started.											
Restriction	-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 100msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.											

8.1.8 PTLON (12h): Partial On

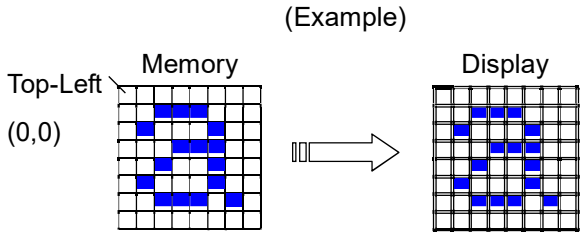
12H	PTLON (Partial On)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	0	↑	1	0	0	0	1	0	0	1	0	(12h)
Parameter	No Parameter											
Description	-This command turns on Partial mode. When partial on, display window become 240duty. -To leave Partial mode, the Partial off command (13h) should be written.											

8.1.9 PTLOFF (13h): Partial Off

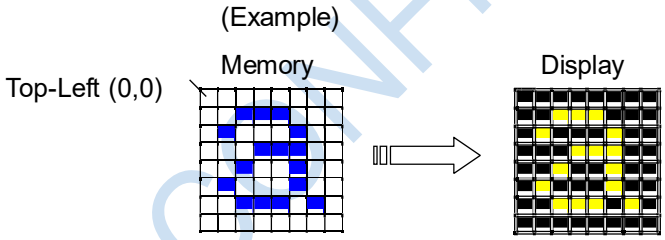
13H	PTLOFF (Partial Off)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLOFF	0	↑	1	0	0	0	1	0	0	1	1	(13h)
Parameter	No Parameter											
Description	-This command turns the display to partial off mode. When partial off, display window become 320duty. -Exit from NORON by the partial mode on command.											

8.1.10 INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	0	0	1	0	0	0	0	0	(20h)
Parameter	No Parameter											

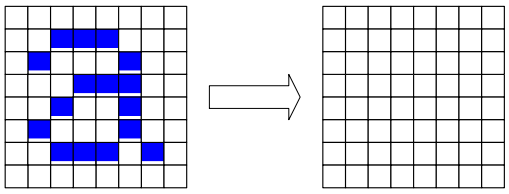
Description	-This command is used to recover from display inversion mode. 

8.1.11 INVON (21h): Display Inversion On

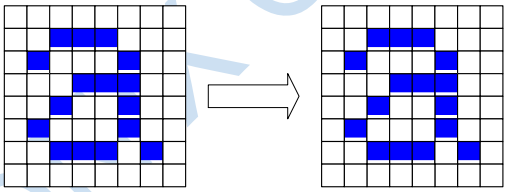
21H	INVON (Display Inversion On)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	0	0	1	0	0	0	0	1	(21h)
Parameter	No Parameter											
Description	-This command is used to enter into display inversion mode. 											

8.1.12 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	(28h)
Parameter	No Parameter											
Description	- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29h)											

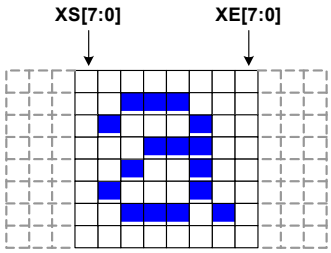
	(Example) Memory → Display 

8.1.13 DISPON (29h): Display On

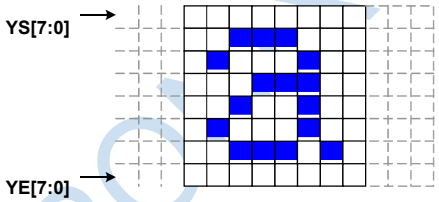
29H	DISPON (Display On)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPON	0	↑	1	0	0	1	0	1	0	0	1	(29h)
Parameter	No Parameter											
Description	- This command is used to recover from DISPLAY OFF mode. - Output from the Frame Memory is enabled. - This command makes no change of contents of frame memory. - This command does not change any other status. (Example) Memory → Display 											

8.1.14 CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	↑	1	0	0	1	0	1	0	1	0	(2Ah)
1st parameter	1	↑	1	0	0	XS5	XS4	XS3	XS2	XS1	XS0	
2th parameter	1	↑	1	0	0	XE5	XE4	XE3	XE2	XE1	XE0	
Description	-The value of XS [5:0] and XE [5:0] are referred when RAMWR command comes. -Each value represents one column line in the Frame Memory.											

	
Restriction	XS [5:0] always must be equal to or less than XE [5:0] When XS [5:0] or XE [5:0] is greater than maximum address like below, data of out of range will be ignored.(Parameter range: 19(13h)≤ XS [5:0] < XE [5:0] ≤ 40 (28h)
Default Value (D7 to D0)	1st parameter= 0x00h 2nd parameter =0x00h

8.1.15 RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET	0	↑	1	0	0	1	0	1	0	1	1	(2Bh)
1nd parameter	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
2th parameter	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
Description	-This command is used to defined area of frame memory where MCU can access. -The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes. -Each value represents one page line in the Frame Memory. 											
Restriction	YS [7:0] always must be equal to or less than YE [15:0] When YS [7:0] or YE [7:0] is greater than maximum address like below, data of out of range will be ignored.(Parameter range: 0 ≤ YS [7:0] < YE [7:0] ≤ 159 (9Fh)											
Default Value (D7 to D0)	1st parameter= 0x00h 2nd parameter =0x00h											

8.1.16 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	0	0	1	0	1	1	0	0	(2Ch)
1st parameter	1	↑	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
…	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
N parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command is used to transfer data from MCU to frame memory. -When this command is accepted, the column register and the page register are reset to the start column/start page positions. -The start column/start page positions are different in accordance with MADCTL setting. -Sending any other command can stop frame write.											

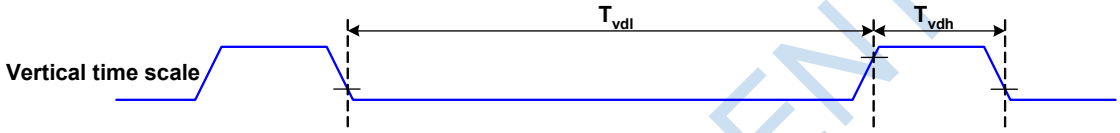
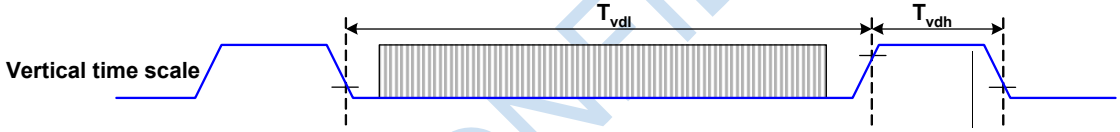
8.1.17 RAMRD (2Eh): Memory Read

2EH	RAMRD (Memory Read)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	0	↑	1	0	0	1	0	1	1	1	0	(2Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	
:	1	1	↑	:	:	:	:	:	:	:	:	
(N+1)th parameter	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	
Description	-This command is used to transfer data from frame memory to MCU. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. -Then D[7:0] is read back from the frame memory and the column register and the row register incremented -Frame Read can be cancelled by sending any other command.											

8.1.18 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	0	0	1	1	0	1	0	0	(34h)
Parameter	No Parameter											
Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.											

8.1.19 TEON (35h): Tearing Effect Line On

35H	TEON (Tearing Effect Line On)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	0	0	1	1	0	1	0	1	(35h)
Parameter	1	↑	1	0	0	0	0	0	0	0	TEM	
Description	-This command is used to turn ON the Tearing Effect output signal from the TE signal line. -The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line: -When TEM ='0': The Tearing Effect output line consists of V-Blanking information only  -When TEM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.											
Default Value (D7 to D0)	0x00h											

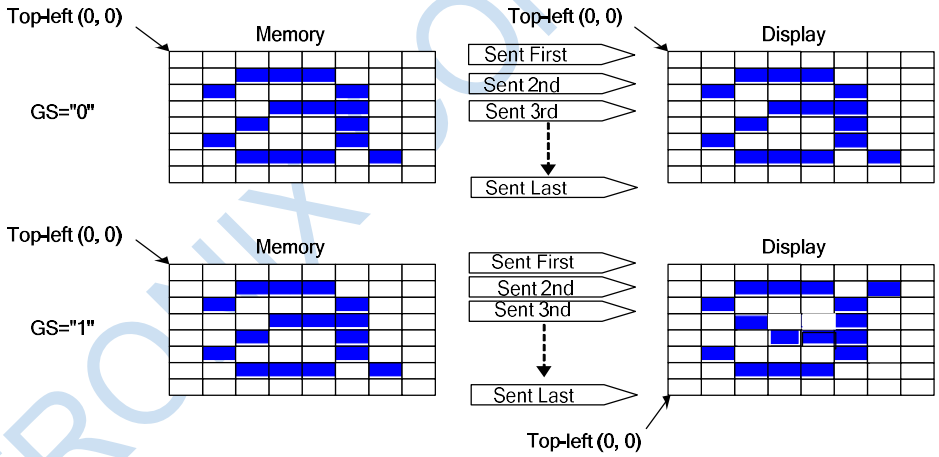
8.1.20 MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	0	0	1	1	0	1	1	0	(36h)
Parameter	1	↑	1	MY	MX	MV	0	DO	GS	0	0	

Description

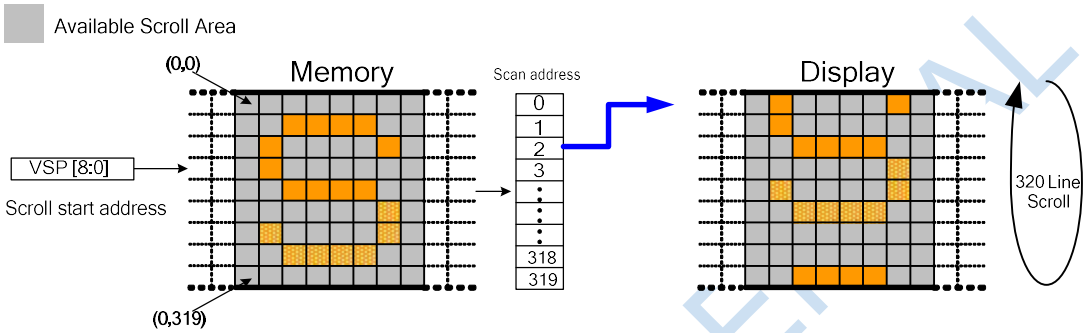
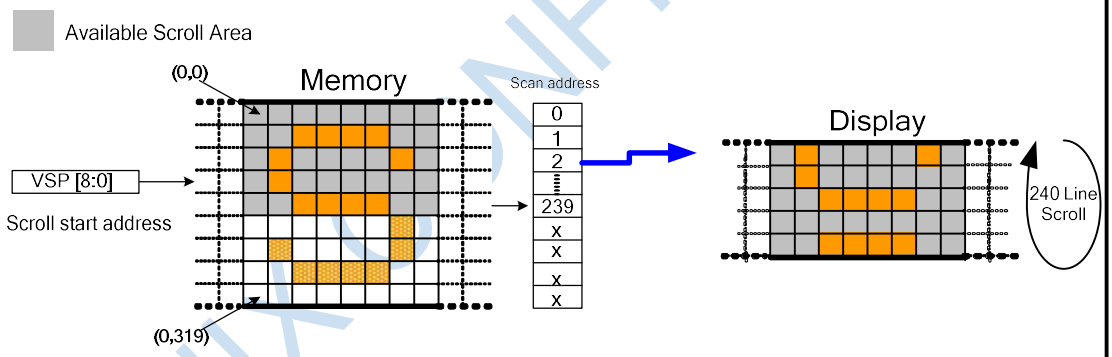
-This command defines read/ write scanning direction of frame memory.

Bit	NAME	DESCRIPTION
D7	MY	Page Address Order
D6	MX	Column Address Order
D5	MV	Page/Column Order
D3	DO	Data Output Order
D2	GS	Gate Scan Order

	-Bit Assignment **Bit D7- Page Address Order (MY)** "0" = Top to Bottom (When MADCTL D7="0"). "1" = Bottom to Top (When MADCTL D7="1"). **Bit D6- Column Address Order (MX)** "0" = Left to Right (When MADCTL D6="0"). "1" = Right to Left (When MADCTL D6="1"). **Bit D5- Page/Column Order (MV)** "0" = Column Direction Mode (When MADCTL D5="0"). "1" = Page Direction Mode (When MADCTL D5="1") **Bit D3- Data Order (DO)** "0" = Left to Right (When MADCTL D3="0" , using in MX=0) "1" = Right to Left (When MADCTL D3="1", using in MX=1) **Bit D2- Gate Scan Order (GS)** "0" =Data refresh Top to Bottom (When MADCTL D2="0") "0" =Data refresh Bottom to Top (When MADCTL D2="1") **Gate Scan Order (GS)** 
Default Value (D7 to D0)	0x00h

8.1.21 VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Address of RAM)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	↑	1	0	0	1	1	0	1	1	1	(37h)
1st parameter	1	↑	1	0	0	0	0	0	0	0	VSP8	
2ND parameter	1	↑	1	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	

Description	- The Vertical Scrolling Start Address command has two parameters which describe which line in the Frame Memory will be written as the first line after the last line on the display as illustrated below: . Example: When partial off (320 Duty) and VSP = '2' (0<=VSP[8:0] <=319)  When partial on (240 Duty) and VSP = '2' (0<=VSP[8:0] <=239) 
Default Value (D7 to D0)	1st parameter = 0x00h 2nd parameter = 0x00h

8.1.22 HPM (38h): High Power Mode ON

38H	HPM (High Power Mode ON)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
HPM	0	↑	1	0	0	1	1	1	0	0	0	(38h)
Parameter	No Parameter											
Description	-This command is used to switch display drive mode to high power mode. In HPM, IC drivers LCD with frame rate (16 / 32 / 25.5 / 51 Hz) that set by **FRCTRL (0xB2h) & OSCSET (0XD8h)** command. -Default setting of IC is HPM. -After reset, it is in high power mode.											

8.1.23 LPM (39h): Low Power Mode ON

39H	LPM (Low Power Mode ON)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
LPM	0	↑	1	0	0	1	1	1	0	0	1	(39h)
Parameter	No Parameter											
Description	-This command is used to switch display drive mode to low power mode. In LPM, IC drivers LCD with frame rate (0.25 to 8Hz) that set by **FRCTRL (0xB2h)** command.											

8.1.24 DTFORM (3Ah): Data Format Select

3AH	DTFORM (Data Format Select)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DTFORM	0	↑	1	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	↑	1	0	0	0	XDE	0	0	0	BPS	
Description	-This command defines data format select. Bit / NAME / DESCRIPTION D4 / XDE / Data Up Down Switch D0 / BPS / Bytes Per Pixel Select **Bit D4- Data Up Down Switch (XDE)** "0" = Switch ON (Using with MY=1) "1" = Switch OFF **Bit D0- Bytes Per Pixel Select (BPS)** "0" = 4 write operations for 24-bit data "1" = 3 write operations for 24-bit data											
Default Value (D7 to D0)	0x00h											

8.1.25 WRMEMC (3Ch): Write Memory Continue

3CH	WRMEMC (Write Memory Continue)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRMEMC	0	↑	1	0	0	1	1	1	1	0	0	(3Ch)
1ST parameter	1	↑	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
⋮	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command.											

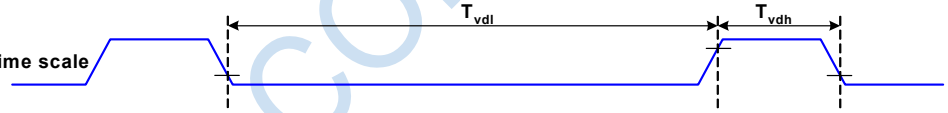
	-If MV=0: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored. If MV=1: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.

8.1.26 RDMEMC (3Eh): Read Memory Continue

3EH	RDMEMC (Read Memory Continue)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDMEMC	0	↑	1	0	0	1	1	1	1	1	0	(3Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
:	1	1	↑	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	1	↑	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous read memory continue or memory read command. -If MV=0: Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If MV=1:											

	Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command.

8.1.27 TESCAN (44h): Set Tear Scanline

44H	TESCAN (Set Tear Scanline)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TESCAN	0	↑	1	0	1	0	0	0	1	0	0	(44h)
1st Parameter	1	↑	1	0	0	0	0	0	0	0	N8	
2nd parameter	1	↑	1	N7	N6	N5	N4	N3	N2	N1	N0	
Description	-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV. -The tearing effect line on has one parameter that describes the tearing effect output line mode. -The tearing effect output line consist of V-blanking information only. Vertical time scale  Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0. The tearing effect output line shall be active low when the display module is in sleep mode											
Default Value (D7 to D0)	1st parameter = 0x00h 2nd parameter = 0x00h											

8.1.28 RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	1	1	0	1	1	0	1	0	(DAh)
Parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Description	-This read byte is used to track the LCD module IC version.											

8.1.29 RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	1	1	0	1	1	0	1	1	(DBh)
Parameter	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
Description	-This read byte is used to track the LCD module/driver IC version.											

8.1.30 RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	1	1	0	1	1	1	0	0	(DCh)
Parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	-This read byte identifies the LCD module/driver.											

8.2 Command Table2

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1.GATESET	0	↑	1	1	0	1	1	0	0	0	0	(B0h)	Gate
	1	↑	1	0	GL[6]	GL[5]	GL[4]	GL[3]	GL[2]	GL[1]	GL[0]		Setting
2.FSTCOM	0	↑	1	1	0	1	1	0	0	0	1	(B1h)	First
	1	↑	1	0	0	0	0	0	0	0	FST[8]		Gate
	1	↑	1	FST[7]	FST[6]	FST[5]	FST[4]	FST[3]	FST[2]	FST[1]	FST[0]		Setting
3.FRCTRL	0	↑	1	1	0	1	1	0	0	1	0	(B2h)	FR
	1	↑	1	0	0	0	HFRA	0	LFRA[2]	LFRA[1]	LFRA[0]		Control
4.GTUPEQH	0	↑	1	1	0	1	1	0	0	1	1	(B3h)	
	1	↑	1	1	GEQEN	1	1	0	1	0	1		
	1	↑	1	1	1	1	1	0	1	1	0		
	1	↑	1	0	GPCHPU0[2:0]			0	GPCHPU1[2:0]				Update
	1	↑	1	0	GPCHPU2[2:0]			0	GPCHPU3[2:0]				Period
	1	↑	1	0	GPCHPU4[2:0]			0	GPCHPU5[2:0]				Gate EQ
	1	↑	1	0	GPCHPU6[2:0]			0	GPCHPU7[2:0]				Control
	1	↑	1	0	GPCHPU8[2:0]			0	GPCHPU9[2:0]				In HPM
	1	↑	1	0	GPCHPU10[2:0]			0	GPCHPU11[2:0]				
	1	↑	1	0	GPCHPU12[2:0]			0	GPCHPU13[2:0]				
	1	↑	1	0	GPCHPU14[2:0]			0	GPCHPU15[2:0]				
5.GTUPEQL	0	↑	1	1	0	1	1	0	1	0	0	(B4h)	
	1	↑	1	0	GPCLPU0[2:0]			0	GPCLPU1[2:0]				
	1	↑	1	0	GPCLPU2[2:0]			0	GPCLPU3[2:0]				Update
	1	↑	1	0	GPCLPU4[2:0]			0	GPCLPU5[2:0]				Period
	1	↑	1	0	GPCLPU6[2:0]			0	GPCLPU7[2:0]				Gate EQ
	1	↑	1	0	GPCLPU8[2:0]			0	GPCLPU9[2:0]				Control
	1	↑	1	0	GPCLPU10[2:0]			0	GPCLPU11[2:0]				In LPM
	1	↑	1	0	GPCLPU12[2:0]			0	GPCLPU13[2:0]				
	1	↑	1	0	GPCLPU14[2:0]			0	GPCLPU15[2:0]				
6.SOUEQ	0	↑	1	1	0	1	1	0	1	1	1	(B7h)	Source
	0	↑	1	0	0	0	SOUEQ	0	0	1	1		EQ Enable
7.PNLSET	0	↑	1	1	0	1	1	1	0	0	0	(B8h)	Panel
	0	↑	1	0	DOTINV[1]	DOTINV[0]	0	DPSCN[1]	DPSCN[0]	LAY[1]	LAY[0]		Setting

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
8.GAMAMS	0	↑	1	1	0	1	1	1	0	0	1	(B9h)	Gamma Mode Setting
	0	↑	1	0	0	GAMA	0	0	0	0	0		
9.CLRAM	0	↑	1	1	0	1	1	1	0	1	1	(BBh)	CLR RAM
	1	↑	1	CLR	1	0	0	1	1	1	1		
10.GCTRL	0	↑	1	1	1	0	0	0	0	0	0	(C0h)	Gate Control
	1	↑	1	0	0	0	VGHA4	VGHA3	VGHA2	VGHA1	VGHA0		
	1	↑	1	0	0	0	VGLA4	VGLA3	VGLA2	VGLA1	VGLA0		
11.VSHPCTRL	0	↑	1	1	1	0	0	0	0	0	1	(C1h)	Source High Positive Voltage Control
	1	↑	1	VSHPA1[7]	VSHPA1[6]	VSHPA1[5]	VSHPA1[4]	VSHPA1[3]	VSHPA1[2]	VSHPA1[1]	VSHPA1[0]		
	1	↑	1	VSHPA2[7]	VSHPA2[6]	VSHPA2[5]	VSHPA2[4]	VSHPA2[3]	VSHPA2[2]	VSHPA2[1]	VSHPA2[0]		
	1	↑	1	VSHPA3[7]	VSHPA3[6]	VSHPA3[5]	VSHPA3[4]	VSHPA3[3]	VSHPA3[2]	VSHPA3[1]	VSHPA3[0]		
	1	↑	1	VSHPA4[7]	VSHPA4[6]	VSHPA4[5]	VSHPA4[4]	VSHPA4[3]	VSHPA4[2]	VSHPA4[1]	VSHPA4[0]		
12.VSLPCTRL	0	↑	1	1	1	0	0	0	0	1	0	(C2h)	Source Low Positive Voltage Control
	1	↑	1	VSLPA1[7]	VSLPA1[6]	VSLPA1[5]	VSLPA1[4]	VSLPA1[3]	VSLPA1[2]	VSLPA1[1]	VSLPA1[0]		
	1	↑	1	VSLPA2[7]	VSLPA2[6]	VSLPA2[5]	VSLPA2[4]	VSLPA2[3]	VSLPA2[2]	VSLPA2[1]	VSLPA2[0]		
	1	↑	1	VSLPA3[7]	VSLPA3[6]	VSLPA3[5]	VSLPA3[4]	VSLPA3[3]	VSLPA3[2]	VSLPA3[1]	VSLPA3[0]		
	1	↑	1	VSLPA4[7]	VSLPA4[6]	VSLPA4[5]	VSLPA4[4]	VSLPA4[3]	VSLPA4[2]	VSLPA4[1]	VSLPA4[0]		
13.VSHNCTRL	0	↑	1	1	1	0	0	0	1	0	0	(C4h)	Source High Negative Voltage Control
	1	↑	1	VSHNA1[7]	VSHNA1[6]	VSHNA1[5]	VSHNA1[4]	VSHNA1[3]	VSHNA1[2]	VSHNA1[1]	VSHNA1[0]		
	1	↑	1	VSHNA2[7]	VSHNA2[6]	VSHNA2[5]	VSHNA2[4]	VSHNA2[3]	VSHNA2[2]	VSHNA2[1]	VSHNA2[0]		
	1	↑	1	VSHNA3[7]	VSHNA3[6]	VSHNA3[5]	VSHNA3[4]	VSHNA3[3]	VSHNA3[2]	VSHNA3[1]	VSHNA3[0]		
	1	↑	1	VSHNA4[7]	VSHNA4[6]	VSHNA4[5]	VSHNA4[4]	VSHNA4[3]	VSHNA4[2]	VSHNA4[1]	VSHNA4[0]		
14.VSLNCTRL	0	↑	1	1	1	0	0	0	1	0	1	(C5h)	Source Low Negative Voltage Control
	1	↑	1	VSLNA1[7]	VSLNA1[6]	VSLNA1[5]	VSLNA1[4]	VSLNA1[3]	VSLNA1[2]	VSLNA1[1]	VSLNA1[0]		
	1	↑	1	VSLNA2[7]	VSLNA2[6]	VSLNA2[5]	VSLNA2[4]	VSLNA2[3]	VSLNA2[2]	VSLNA2[1]	VSLNA2[0]		
	1	↑	1	VSLNA3[7]	VSLNA3[6]	VSLNA3[5]	VSLNA3[4]	VSLNA3[3]	VSLNA3[2]	VSLNA3[1]			
	1	↑	1	VSLNA4[7]	VSLNA4[6]	VSLNA4[5]	VSLNA4[4]	VSLNA4[3]	VSLNA4[2]	VSLNA4[1]	VSLNA4[0]		
15.VSIKCTRL	0	↑	1	1	1	0	0	1	0	0	0	(C8h)	Source

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	VSIP[7]	VSIP[6]	VSIP[5]	VSIP[4]	VSIP[3]	VSIP[2]	VSIP[1]	VSIP[0]		Gamma Voltage Control
	1	↑	1	VSKP[7]	VSKP[6]	VSKP[5]	VSKP[4]	VSKP[3]	VSKP[2]	VSKP[1]	VSKP[0]		
	1	↑	1	VSIN[7]	VSIN[6]	VSIN[5]	VSIN[4]	VSIN[3]	VSIN[2]	VSIN[1]	VSIN[0]		
	1	↑	1	VSKN[7]	VSKN[6]	VSKN[5]	VSKN[4]	VSKN[3]	VSKN[2]	VSKN[1]	VSKN[0]		
16.VSHLSEL	0	↑	1	1	1	0	0	1	0	0	1	(C9h)	Source Voltage Select
	1	↑	1	0	0	0	0	0	0	VSHLSEL[1:0]			
17.ID1SET	0	↑	1	1	1	0	0	1	0	1	0	(CAh)	ID1 Set
	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
18.ID2SET	0	↑	1	1	1	0	0	1	0	1	1	(CBh)	ID2 Set
	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
19.ID3SET	0	↑	1	1	1	0	0	1	1	0	0	(CCh)	ID3 Set
	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
20 AUTOPWR	0	↑	1	1	1	0	1	0	0	0	0	(D0h)	Enable Auto Power Down
	1	↑	1	AUTOPWR	1	1	1	1	1	1	1		
21.BSTEN	0	↑	1	1	1	0	1	0	0	0	1	(D1h)	Booster Enable
	1	↑	1	0	0	0	0	0	0	0	BSTEN		
22. NVLOADCTRL	0	↑	1	1	1	0	1	0	1	1	0	(D6h)	NV Load Ctrl
	1	↑	1	0	0	0	1	0	VS_EN	ID_EN	1		
	1	↑	1	0	0	0	0	0	NRDTIME	NRDSLP	0		
23. OSCSET	0	↑	1	1	1	0	1	1	0	0	0	(D8h)	OSC Setting
	1	↑	1	OSCEN	0	OSCSW2	0	0	OSCSW1	OSCSW0	0		
	1	↑	1	1	1	1	0	1	0	0	1		
24.NVMRD	0	↑	1	1	1	1	0	1	0	0	1	(E9h)	OTP Data Read
	1	1	↑	DO[7]	DO[6]	DO[5]	DO[4]	DO[3]	DO[2]	DO[1]	DO[0]		

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
25.EXTBCTRL	0	↑	1	1	1	1	0	1	1	0	0	(ECh)	EXTB
	1	↑	1	EXTB_CTRL [7:0]									Control
26.NVMCTRL1	0	↑	1	1	1	1	1	1	0	0	0	(F8h)	
	1	↑	1	0	1	0	1	1	0	1	0	(5Ah)	NVM
	1	↑	1	0	1	1	0	1	0	0	1	(69h)	WR/RD
	1	↑	1	1	1	1	0	1	1	1	0	(EEh)	Control
	1	↑	1	0	0	0	0	0	PROG	RD	0		
27.NVMCTRL2	0	↑	1	1	1	1	1	1	0	1	0	(FAh)	NVM
	1	↑	1	0	0	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]		Program
	1	↑	1	PIN[7]	PIN[6]	PIN[5]	PIN[4]	PIN[3]	PIN[2]	PIN[1]	PIN[0]		Setting
28.NVMRDEN	0	↑	1	1	1	1	1	1	0	1	1	(FBh)	Enable
	1	↑	1	0	1	0	0	1	0	1	0	(4Ah)	NVM
	1	↑	1	1	0	1	0	0	1	0	1	(A5h)	Read
29.NVPROM	0	↑	1	1	1	1	1	1	1	0	0	(FCh)	Enable
	1	↑	1	0	0	1	0	1	0	0	1	(29h)	NVM
	1	↑	1	1	0	1	0	0	1	0	1	(A5h)	Program

8.2.1 GATESET (B0h): Gate Line Setting

B0H	GATESET (Gate Line Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATESET	0	↑	1	1	0	1	1	0	0	0	0	(B0h)
1st parameter	1	↑	1	0	GL[6]	GL[5]	GL[4]	GL[3]	GL[2]	GL[1]	GL[0]	
Description	**GL[6:0]** specifies the gate line of the module in 4-line basis. This command must be selected before sleep-out. Do not change this command while the display is turned on. The relationship between the parameter GL[6:0] and the number of display lines is shown below.											
Default Value (D7 to D0)	0x00h											

GL[6]	GL[5]	GL[4]	GL[3]	GL[2]	GL[1]	GL[0]	Gate Line of Module
0	0	0	0	0	0	1	4
0	0	0	0	0	1	0	8
0	0	0	0	0	1	1	12
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	312
1	0	0	1	1	1	1	316
1	0	1	0	0	0	0	320

8.2.2 FSTCOM (B1h): First Gate Setting

B1H	FSTCOM (First Gate Setting)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FSTCOM	0	↑	1	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	↑	1	0	0	0	0	0	0	0	FST[8]	
2nd parameter	1	↑	1	FST[7]	FST[6]	FST[5]	FST[4]	FST[3]	FST[2]	FST[1]	FST[0]	
Description	**FST[8:0]** specifies “the first output gate number – 1 “ that mapping to the RAM page address 0. Continuously increasing or decreasing the first gate setting results in vertical-scrolling in 4-line basis. For detail setting value, please see the table as below.											

FST8	FST7	FST6	FST5	FST4	FST3	FST2	FST1	FST0	Line address
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	1	4
0	0	0	0	0	0	1	1	1	8
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	0	1	1	1	312
1	0	0	1	1	1	0	1	1	316
1	0	0	1	1	1	1	1	1	320

	Example: If FST[8:0]=7h, Gate 8 would output the data of RAM page address 0.
Default Value (D7 to D0)	1st Parameter=0x00h 2nd parameter=0x00h

8.2.3 FRCTRL (B2h): Frame Rate Control

B2H	FRCTRL (Frame Rate Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRCTRL	0	↑	1	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	↑	1	0	0	0	HFRA	0	LFRA[2]	LFRA[1]	LFRA[0]	

Description

HFRA: Frame rate control in high power mode (HPM).

Parameter Setting of 0xD8h Command	HFRA	Frame rate (Hz)
Parameter 1: 0xA6h (OSCSW[2:0]=111)	0	16
Parameter 2: 0XE9h	1	32
Parameter 1: 0x80h (OSCSW[2:0]=000)	0	25.5
Parameter 2: 0XE9h	1	51

LFRA[2:0]: Frame rate control in low power mode (LPM)

LFRA [2:0]	Frame rate (Hz)
0h	0.25
1h	0.5
2h	1
3h	2
4h	4
5h	8

Default Value (D7 to D0)	0x12h

8.2.4 GTUPEQH (B3h): Update Period Gate EQ Control in HPM

B3H	GTUPEQH (Update Period Gate EQ Control in HPM)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GTUPEQH	0	↑	1	1	0	1	1	0	0	1	1	(B3h)
1st parameter	1	↑	1	1	GEQEN	1	0	0	1	0	1	
2nd parameter	1	↑	1	1	1	1	1	0	1	1	0	
3rd parameter	1	↑	1	0	GPCHPU0[2:0]			0	GPCHPU1[2:0]			
4th parameter	1	↑	1	0	GPCHPU2[2:0]			0	GPCHPU3[2:0]			
5th parameter	1	↑	1	0	GPCHPU4[2:0]			0	GPCHPU5[2:0]			
6th parameter	1	↑	1	0	GPCHPU6[2:0]			0	GPCHPU7[2:0]			
7rd parameter	1	↑	1	0	GPCHPU8[2:0]			0	GPCHPU9[2:0]			
8th parameter	1	↑	1	0	GPCHPU10[2:0]			0	GPCHPU11[2:0]			
9th parameter	1	↑	1	0	GPCHPU12[2:0]			0	GPCHPU13[2:0]			
10th parameter	1	↑	1	0	GPCHPU14[2:0]			0	GPCHPU15[2:0]			

Description

-This command is used to set gate EQ waveform in update period.

GEQEN: Gate EQ Enable (HPM/LPM both)

GEQEN	Gate EQ Enable
0	Disable
1	Enable

GPCHPU0~ GPCHPU15: Gate EQ Control in HPM at 0~15 PWM

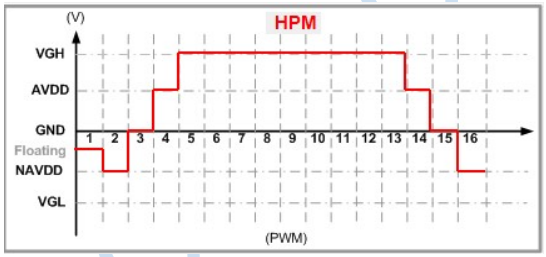
Gate EQ of HPM update period includes 16 PWMs to achieve..

GPCHPU0~15[2:0]	Gate EQ Voltage
000	Floating
001	VGL
100	GND
101	NAVDD
110	AVDD
111	VGH

Default HPM Update EQ Setting.

HPM PWM	Default Parameter	Voltage
GPCHPU0	000	Floating
GPCHPU1	101	NAVDD
GPCHPU2	100	GND
GPCHPU3	110	AVDD
GPCHPU4	111	VGH
GPCHPU5	111	VGH
GPCHPU6	111	VGH
GPCHPU7	111	VGH
GPCHPU8	111	VGH
GPCHPU9	111	VGH
GPCHPU10	111	VGH
GPCHPU11	111	VGH
GPCHPU12	111	VGH
GPCHPU13	110	AVDD
GPCHPU14	100	GND
GPCHPU15	101	NAVDD

Default HPM Update EQ Waveform as below



Default Value (D7 to D0)

1st Parameter=0xE5h

2nd parameter=0xF6h

3rd parameter=0x05h

4th parameter=0x46h

5th parameter=0x77h

6th parameter=0x77h

7rd parameter= 0x77h

8th parameter=0x77h

9th parameter=0x76h

10th parameter=0x45h

8.2.5 GTUPEQL (B4h): Update Period Gate EQ Control in LPM

B4H	GTUPEQL (Update Period Gate EQ Control in LPM)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GTUPEQL	0	↑	1	1	0	1	1	0	1	0	0	(B4h)
1st parameter	1	↑	1	0	GPCLPU0[2:0]			0	GPCLPU1[2:0]			
2nd parameter	1	↑	1	0	GPCLPU2[2:0]			0	GPCLPU3[2:0]			
3rd parameter	1	↑	1	0	GPCLPU4[2:0]			0	GPCLPU5[2:0]			
4th parameter	1	↑	1	0	GPCLPU6[2:0]			0	GPCLPU7[2:0]			
5th parameter	1	↑	1	0	GPCLPU8[2:0]			0	GPCLPU9[2:0]			
6th parameter	1	↑	1	0	GPCLPU10[2:0]			0	GPCLPU11[2:0]			
7rd parameter	1	↑	1	0	GPCLPU12[2:0]			0	GPCLPU13[2:0]			
8th parameter	1	↑	1	0	GPCLPU14[2:0]			0	GPCLPU15[2:0]			

Description

GPCLPU0~ GPCLPU15: Gate EQ Control in LPM at 0~15 PWM

Gate EQ of LPM update period includes 16 PWMs to achieve.

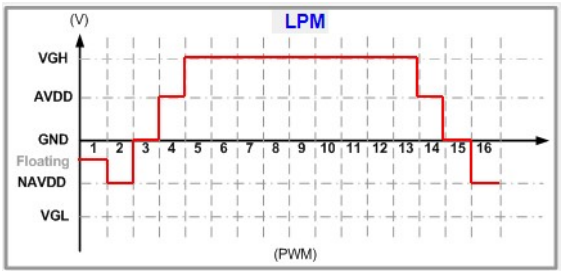
GPCLPU0~15[2:0]	Gate EQ Voltage
000	Floating
001	VGL
100	GND
101	NAVDD
110	AVDD
111	VGH

Default HPM Update EQ Setting.

LPM PWM	Default Parameter	Voltage
GPCLPU0	000	Floating
GPCLPU1	101	NAVDD
GPCLPU2	100	GND
GPCLPU3	110	AVDD
GPCLPU4	111	VGH
GPCLPU5	111	VGH
GPCLPU6	111	VGH
GPCLPU7	111	VGH
GPCLPU8	111	VGH
GPCLPU9	111	VGH
GPCLPU10	111	VGH

	GPCLPU11	111	VGH
	GPCLPU12	111	VGH
	GPCLPU13	110	AVDD
	GPCLPU14	100	GND
	GPCLPU15	101	NAVDD

Default LPM Update EQ Waveform as below



Default Value (D7 to D0)	1st Parameter=0x05h 2nd parameter=0x46h 3rd parameter=0x77h 4th parameter=0x77h 5th parameter=0x77h 6th parameter=0x77h 7rd parameter= 0x76h 8th parameter=0x45h

8.2.6 SOUEQ (B7h): Source EQ Enable

B7H	SOUEQ (Source EQ Enable)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SOUEQ	0	↑	1	1	0	1	1	0	1	1	1	(B7h)
1st parameter	1	↑	1	0	0	0	SOUEQ	0	0	1	1	
Description	**SOUEQ** "0": Disable Source EQ. "1": Enable Source EQ.											
Default Value (D7 to D0)	0x13h											

8.2.7 PNLSET (B8h): Panel Setting

B8H	PNLSET (Panel Setting)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PNLSET	0	↑	1	1	0	1	1	1	0	0	0	(B8h)
Parameter	1	↑	1	0	DOTINV[1]	DOTINV[0]	0	DPSCN[1]	DPSCN[0]	LAY[1]	LAY[0]	

Description

-This command is used to set the gate scan and panel layout.

DOTINV[1:0]:

DOTINV [1:0]	Column/Dot Inversion
00	Column inversion
01	1-Dot inversion
10	2-Dot inversion

DPSCN[1:0]: Display Gate Scan Mode Select

DPSCN [1:0]	Gate Scan Mode
00	Two Line Interval
01	One Line Interval
10	Frame interval

LAY[1:0]: Panel Layout Select

LAY [1:0]	Panel Layout
00	Two Line Interlace
01	One Line Interlace
10	Non Interlace

Default Value (D7 to D0): 0x0Ah

8.2.8 GAMAMS (B9h): Gamma Mode Setting

B9H	GAMAMS (Gamma Mode Setting)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMAMS	0	↑	1	1	0	1	1	1	0	0	1	(B9h)
Parameter	1	↑	1	0	0	GAMA	0	0	0	0	0	

Description

-This command is used to control gamma mode

-GAMA : Gamma Mode Setting

“0” = 4GS

“1” = Mono (Default)

Default Value (D7 to D0)	0x20h

8.2.9 CLRAM (BBh): Enable Clear RAM

BBH	CLRAM (Enable Clear RAM)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CLRAM	0	↑	1	1	0	1	1	1	0	1	1	(BBh)
Parameter	1	↑	1	CLR	1	0	0	1	1	1	1	
Description	-This command is used to clear RAM to 0. CLR=0 ; Enable Clear RAM CLR=1 ; Disable Clear RAM											

8.2.10 GCTRL (C0h): Gate Voltage Control

C0H	GCTRL (Gate Voltage Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GCTRL	0	↑	1	1	1	0	0	0	0	0	0	(C0h)
1st parameter	1	↑	1	0	0	0	VGHA4	VGHA3	VGHA2	VGHA1	VGHA0	
2nd parameter	1	↑	1	0	0	0	VGLA4	VGLA3	VGLA2	VGLA1	VGLA0	

Description

-This command is used to adjust gate voltage.

VGHA[4:0]: VGH Setting.

VGHA[4:0]	VGH (V)
00h	8.0
01h	8.5
02h	9.0
03h	9.5
04h	10.0
05h	10.5
06h	11.0
07h	11.5
08h	12.0
09h	12.5
0Ah	13.0
0Bh	13.5
0Ch	14.0
0Dh	14.5
0Eh	15.0 (default)
0Fh	15.5
10h	16.0
11h	16.5
12h	17.0

VGLA[4:0]: VGL Setting.

VGLA[4:0]	VGL (V)
02h	-6.0
03h	-6.5
04h	-7.0
05h	-7.5
06h	-8.0
07h	-8.5
08h	-9.0
09h	-9.5
0Ah	-10.0 (default)
0Bh	-10.5
0Ch	-11.0
0Dh	-11.5
0Eh	-12.0
0Fh	-12.5
10h	-13.0
11h	-13.5
12h	-14.0
13h	-14.5
14h	-15.0

Default Value (D7 to D0)	1st Parameter=0x0Eh 2nd parameter=0x0Ah

8.2.11 VSHPCTRL (C1h): Source High Positive Voltage Control

C1H	VSHPCTRL (Source High Positive Voltage Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSHPCTRL	0	↑	1	1	1	0	0	0	0	0	1	(C1h)
1st parameter	1	↑	1	VSHPA1[7]	VSHPA1[6]	VSHPA1[5]	VSHPA1[4]	VSHPA1[3]	VSHPA1[2]	VSHPA1[1]	VSHPA1[0]	
2nd parameter	1	↑	1	VSHPA2[7]	VSHPA2[6]	VSHPA2[5]	VSHPA2[4]	VSHPA2[3]	VSHPA2[2]	VSHPA2[1]	VSHPA2[0]	
3rd parameter	1	↑	1	VSHPA3[7]	VSHPA3[6]	VSHPA3[5]	VSHPA3[4]	VSHPA3[3]	VSHPA3[2]	VSHPA3[1]	VSHPA3[0]	
4th parameter	1	↑	1	VSHPA4[7]	VSHPA4[6]	VSHPA4[5]	VSHPA4[4]	VSHPA4[3]	VSHPA4[2]	VSHPA4[1]	VSHPA4[0]	

Description

-This command is used to adjust source high positive voltage in different mode.

The calculation of VSHPAx is as shown below:

VSHPAx= 3.7+0.02x VSHPAx[7:0]

VSHPA1[7:0] : Source High Positive Voltage Mode1

VSHPA2[7:0] : Source High Positive Voltage Mode2

VSHPA3[7:0] : Source High Positive Voltage Mode3

VSHPA4[7:0] : Source High Positive Voltage Mode4

The suggestion of usable VSHPAx voltage is shown below

VSHPAx[7]	VSHPAx[6]	VSHPAx[5]	VSHPAx[4]	VSHPAx[3]	VSHPAx[2]	VSHPAx[1]	VSHPAx[0]	VSHPAx(V)
0	0	0	0	0	0	0	0	3.70
0	0	0	0	0	0	0	1	3.72
0	0	0	0	0	0	1	0	3.74
:	:	:	:	:	:	:	:	:
0	1	0	0	0	0	0	1	5.00 (default)
:	:	:	:	:	:	:	:	:
0	1	1	1	1	0	1	1	6.16
0	1	1	1	1	1	0	0	6.18
0	1	1	1	1	1	0	1	6.20

Default Value (D7 to D0)

1st Parameter=0x41h

2nd parameter=0x41h

3rd parameter=0x41h

4th parameter=0x41h

8.2.12 VSLPCTRL (C2h): Source Low Positive Voltage Control

C2H	VSLPCTRL (Source Low Positive Voltage Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSLPCTRL	0	↑	1	1	1	0	0	0	0	1	0	(C2h)
1st parameter	1	↑	1	VSLPA1[7]	VSLPA1[6]	VSLPA1[5]	VSLPA1[4]	VSLPA1[3]	VSLPA1[2]	VSLPA1[1]	VSLPA1[0]	
2nd parameter	1	↑	1	VSLPA2[7]	VSLPA2[6]	VSLPA2[5]	VSLPA2[4]	VSLPA2[3]	VSLPA2[2]	VSLPA2[1]	VSLPA2[0]	
3rd parameter	1	↑	1	VSLPA3[7]	VSLPA3[6]	VSLPA3[5]	VSLPA3[4]	VSLPA3[3]	VSLPA3[2]	VSLPA3[1]	VSLPA3[0]	
4th parameter	1	↑	1	VSLPA4[7]	VSLPA4[6]	VSLPA4[5]	VSLPA4[4]	VSLPA4[3]	VSLPA4[2]	VSLPA4[1]	VSLPA4[0]	

Description

-This command is used to adjust source low positive voltage in different mode.

The calculation of VSLPAx is as shown below:

VSLPAx= 0.02x VSLPAx [7:0]

VSLPA1 [7:0] : Source Low Positive Voltage Mode1

VSLPA2 [7:0] : Source Low Positive Voltage Mode2

VSLPA3 [7:0] : Source Low Positive Voltage Mode3

VSLPA4 [7:0] : Source Low Positive Voltage Mode4

The suggestion of usable VSLPAx voltage is shown below

VSLPAx[7]	VSLPAx[6]	VSLPAx[5]	VSLPAx[4]	VSLPAx[3]	VSLPAx[2]	VSLPAx[1]	VSLPAx[0]	VSLPAx(V)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.02
0	0	0	0	0	0	1	0	0.04
:	:	:	:	:	:	:	:	:
0	1	1	0	0	0	1	0	1.00 (default)
:	:	:	:	:	:	:	:	:
0	1	1	0	0	0	0	1	1.96
0	1	1	0	0	0	1	0	1.98
0	1	1	0	0	0	1	1	2.00

Default Value (D7 to D0)

1st Parameter=0x32h

2nd parameter=0x32h

3rd parameter=0x32h

4th parameter=0x32h

8.2.13 VSHNCTRL (C4h): Source High Negative Voltage Control

C4H	VSHNCTRL (Source High Negative Voltage Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSHNCTRL	0	↑	1	1	1	0	0	0	1	0	0	(C4h)
1st parameter	1	↑	1	VSHNA1[7]	VSHNA1[6]	VSHNA1[5]	VSHNA1[4]	VSHNA1[3]	VSHNA1[2]	VSHNA1[1]	VSHNA1[0]	
2nd parameter	1	↑	1	VSHNA2[7]	VSHNA2[6]	VSHNA2[5]	VSHNA2[4]	VSHNA2[3]	VSHNA2[2]	VSHNA2[1]	VSHNA2[0]	
3rd parameter	1	↑	1	VSHNA3[7]	VSHNA3[6]	VSHNA3[5]	VSHNA3[4]	VSHNA3[3]	VSHNA3[2]	VSHNA3[1]	VSHNA3[0]	
4th parameter	1	↑	1	VSHNA4[7]	VSHNA4[6]	VSHNA4[5]	VSHNA4[4]	VSHNA4[3]	VSHNA4[2]	VSHNA4[1]	VSHNA4[0]	

Description

-This command is used to adjust source high negative voltage in different mode.

The calculation of VSHNAx is as shown below:

VSHNAx= -2.5-0.02x VSHNAx[7:0]

VSHNA1[7:0] : Source High Negative Voltage Mode1

VSHNA2[7:0] : Source High Negative Voltage Mode2

VSHNA3[7:0] : Source High Negative Voltage Mode3

VSHNA4[7:0] : Source High Negative Voltage Mode4

The suggestion of usable VSHNAx voltage is shown below

VSHNAx[7]	VSHNAx[6]	VSHNAx[5]	VSHNAx[4]	VSHNAx[3]	VSHNAx[2]	VSHNAx[1]	VSHNAx[0]	VSHNAx(V)
0	0	0	0	0	0	0	0	-2.50
0	0	0	0	0	0	0	1	-2.52
0	0	0	0	0	0	1	0	-2.54
:	:	:	:	:	:	:	:	:
0	1	0	0	0	1	1	0	-3.90 (default)
:	:	:	:	:	:	:	:	:
1	0	0	0	0	1	0	1	-5.16
1	0	0	0	0	1	1	0	-5.18
1	0	0	0	0	1	1	1	-5.20

Default Value (D7 to D0)

1st Parameter=0x46h

2nd parameter=0x46h

3rd parameter=0x46h

4th parameter=0x46h

8.2.14 VSLNCTRL (C5h): Source Low Negative Voltage Control

C5H	VSLNCTRL (Source Low Positive Voltage Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSLNCTRL	0	↑	1	1	1	0	0	0	1	0	1	(C5h)
1st parameter	1	↑	1	VSLNA1[7]	VSLNA1[6]	VSLNA1[5]	VSLNA1[4]	VSLNA1[3]	VSLNA1[2]	VSLNA1[1]	VSLNA1[0]	
2nd parameter	1	↑	1	VSLNA2[7]	VSLNA2[6]	VSLNA2[5]	VSLNA2[4]	VSLNA2[3]	VSLNA2[2]	VSLNA2[1]	VSLNA2[0]	
3rd parameter	1	↑	1	VSLNA3[7]	VSLNA3[6]	VSLNA3[5]	VSLNA3[4]	VSLNA3[3]	VSLNA3[2]	VSLNA3[1]	VSLNA3[0]	
4th parameter	1	↑	1	VSLNA4[7]	VSLNA4[6]	VSLNA4[5]	VSLNA4[4]	VSLNA4[3]	VSLNA4[2]	VSLNA4[1]	VSLNA4[0]	

Description

-This command is used to adjust source low positive voltage in different mode.

The calculation of VSLNAx is as shown below:

VSLNAx=1- 0.02x VSLNAx [7:0]

VSLNA1 [7:0] : Source Low Negative Voltage Mode1

VSLNA2 [7:0] : Source Low Negative Voltage Mode2

VSLNA3 [7:0] : Source Low Negative Voltage Mode3

VSLNA4 [7:0] : Source Low Negative Voltage Mode4

The suggestion of usable VSLNAx voltage is shown below

VSLNAx[7]	VSLNAx[6]	VSLNAx[5]	VSLNAx[4]	VSLNAx[3]	VSLNAx[2]	VSLNAx[1]	VSLNAx[0]	VSLNAx(V)
0	0	0	0	0	0	0	0	1.00
0	0	0	0	0	0	0	1	0.98
0	0	0	0	0	0	1	0	0.96
:	:	:	:	:	:	:	:	:
0	1	0	0	0	1	1	0	-0.40 (default)
:	:	:	:	:	:	:	:	:
1	0	0	0	1	0	1	0	-1.76
1	0	0	0	1	0	1	1	-1.78
1	0	0	0	1	1	0	0	-1.80

Default Value (D7 to D0)

1st Parameter=0x46h

2nd parameter=0x46h

3rd parameter=0x46h

4th parameter=0x46h

8.2.15 VSIKCTRL (C8h): Source Gamma Voltage Control

C8H	VSIKCTRL (Source Gamma Voltage Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSIKCTRL	0	↑	1	1	1	0	0	1	0	0	0	(C8h)
1st parameter	1	↑	1	VSIP[7]	VSIP[6]	VSIP[5]	VSIP[4]	VSIP[3]	VSIP[2]	VSIP[1]	VSIP[0]	
2nd parameter	1	↑	1	VSKP[7]	VSKP[6]	VSKP[5]	VSKP[4]	VSKP[3]	VSKP[2]	VSKP[1]	VSKP[0]	
3rd parameter	1	↑	1	VSIN[7]	VSIN[6]	VSIN[5]	VSIN[4]	VSIN[3]	VSIN[2]	VSIN[1]	VSIN[0]	
4th parameter	1	↑	1	VSKN[7]	VSKN[6]	VSKN[5]	VSKN[4]	VSKN[3]	VSKN[2]	VSKN[1]	VSKN[0]	

Description

-This command is used to adjust source gamma voltage in positive/negative...

The calculation of VSIP/VSKP/VSIN/VSKN is as shown below:

VSIP= 2.2+0.02x VSIP[7:0]

VSKP= 1.2+0.02x VSKP[7:0]

VSIN= -1-0.02x VSIN[7:0]

VSKN= -0.02x VSKN[7:0]

VSIP [7:0] : Source Positive Gamma Voltage 1

VSKP [7:0] : Source Positive Gamma Voltage 2

VSIN [7:0] : Source Negative Gamma Voltage 1

VSKN [7:0] : Source Negative Gamma Voltage 1

The suggestion of usable **VSIP** voltage is shown below

VSIP [7]	VSIP [6]	VSIP [5]	VSIP [4]	VSIP [3]	VSIP [2]	VSIP [1]	VSIP [0]	VSIP (V)
0	0	0	0	0	0	0	0	2.20
0	0	0	0	0	0	0	1	2.22
0	0	0	0	0	0	1	0	2.24
:	:	:	:	:	:	:	:	:
0	1	0	0	0	1	1	0	3.60 (default)
:	:	:	:	:	:	:	:	:
1	0	0	0	1	0	1	0	4.96
1	0	0	0	1	0	1	1	4.98
1	0	0	0	1	1	0	0	5.00

The suggestion of usable **VSKP** voltage is shown below

VSKP [7]	VSKP [6]	VSKP [5]	VSKP [4]	VSKP [3]	VSKP [2]	VSKP [1]	VSKP [0]	VSKP (V)
0	0	0	0	0	0	0	0	1.20
0	0	0	0	0	0	0	1	1.22
0	0	0	0	0	0	1	0	1.24
:	:	:	:	:	:	:	:	:
0	1	0	0	0	1	1	0	2.60 (default)
:	:	:	:	:	:	:	:	:
1	0	0	0	1	0	1	0	3.96
1	0	0	0	1	0	1	1	3.98
1	0	0	0	1	1	0	0	4.00

The suggestion of usable **VSIN** voltage is shown below

VSIN [7]	VSIN [6]	VSIN [5]	VSIN [4]	VSIN [3]	VSIN [2]	VSIN [1]	VSIN [0]	VSIN (V)
0	0	0	0	0	0	0	0	-1.00
0	0	0	0	0	0	0	1	-1.02
0	0	0	0	0	0	1	0	-1.04
:	:	:	:	:	:	:	:	:
0	1	0	0	0	1	1	0	-2.40 (default)
:	:	:	:	:	:	:	:	:
1	0	0	0	1	0	1	0	-3.76
1	0	0	0	1	0	1	1	-3.78
1	0	0	0	1	1	0	0	-3.80

The suggestion of usable **VSKN** voltage is shown below

VSKN [7]	VSKN [6]	VSKN [5]	VSKN [4]	VSKN [3]	VSKN [2]	VSKN [1]	VSKN [0]	VSKN (V)
0	0	0	0	0	0	0	0	0.00
0	0	0	0	0	0	0	1	-0.02
0	0	0	0	0	0	1	0	-0.04
:	:	:	:	:	:	:	:	:
0	1	0	0	0	1	1	0	-1.40 (default)
:	:	:	:	:	:	:	:	:
1	0	0	0	1	0	1	0	-2.76
1	0	0	0	1	0	1	1	-2.78
1	0	0	0	1	1	0	0	-2.80

Default Value (D7 to D0)	1st Parameter=0x46h 2nd parameter=0x46h 3rd parameter=0x46h 4th parameter=0x46h

8.2.16 VSHLSEL (C9h): Source Voltage Select

C9H	VSHLSEL (Source Voltage Select)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSHLSEL	0	↑	1	1	1	0	0	1	0	0	1	(C9h)
Parameter	1	↑	1	0	0	0	0	0	0	VSHLSEL[1:0]		
Description	-This command is used to switch source voltage. **VSHLSEL [1:0]** / **Source Voltage** 00 / VSHPA1/ VSLPA1/ VSHNA1/ VSLNA1 01 / VSHPA2/ VSLPA2/ VSHNA2/ VSLNA2 10 / VSHPA3/ VSLPA3/ VSHNA3/ VSLNA3 11 / VSHPA4/ VSLPA4/ VSHNA4/ VSLNA4											
Default Value (D7 to D0)	Parameter=0x00h											

8.2.17 ID1SET (CAh): ID1 Setting

CAH	ID1SET (ID1 Code Setting)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ID1SET	0	↑	1	1	1	0	0	1	0	1	0	(CAh)
Parameter	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Description	**ID1[7:0]:** ID1 Setting.											
Default Value (D7 to D0)	Parameter=0x00h											

8.2.18 ID2SET (CBh): ID2 Setting

CBH	ID2SET (ID2 Code Setting)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ID2SET	0	↑	1	1	1	0	0	1	0	1	1	(CBh)
Parameter	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
Description	**ID2[7:0]:** ID2 Setting.											
Default Value (D7 to D0)	Parameter=0x00h											

8.2.19 ID3SET (CCh): ID3 Setting

CCH	ID3SET (ID3 Code Setting)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ID3SET	0	↑	1	1	1	0	0	1	1	0	0	(CCh)
Parameter	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	**ID3[7:0]:** ID3 Setting.											
Default Value (D7 to D0)	Parameter=0x00h											

8.2.20 AUTOPWRCTRL (D0h): Enable Auto Power Down

D0H	AUTOPWRCTRL (Enable Auto Power Down)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
AUTOPWRCTRL	0	↑	1	1	1	0	1	0	0	0	0	(D0h)
Parameter	1	↑	1	AUTOPWR	1	1	1	1	1	1	1	
Description	-This command is used to enable/disable auto power down **AUTOPWR:** "0": Disable Auto Power down. "1": Enable Auto Power down											
Default Value (D7 to D0)	Parameter=0xFFh											

8.2.21 BSTEN (D1h): Booster Enable

D1H	BSTEN (Booster Enable)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BSTEN	0	↑	1	1	1	0	1	0	0	0	1	(D1h)
Parameter	1	↑	1	0	0	0	0	0	0	0	BSTEN	
Description	**BSTEN:** "0": Disable Booster "1": Enable Booster											
Default Value (D7 to D0)	Parameter=0x00h											

8.2.22 NVMLOADCTRL (D6h): NVM Load Control

D6H	NVMLOADCTRL (NVM Load Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMLOADCTRL	0	↑	1	1	1	0	1	0	1	1	0	(D6h)
1st parameter	1	↑	1	0	0	0	1	0	VS_EN	ID_EN	1	
2nd parameter	1	↑	1	0	0	0	0	0	NRDTIME	NRDSLP	0	

Description

-This command is used to control the items load by NVM and NVM Load control.

Bit	NVM Load Item	Value
VS_EN	Source High/Low Voltage	'0' = Disable Source High/Low Voltage Load '1' = Enable Source High/Low Voltage Load
ID_EN	ID1/ID2/ID3	'0' = Disable ID1/ID/ID3 Load '1' = Enable ID1/ID/ID3 Load
NRDTIME	NVM Load Control by Timer	"0": NVM load will not be trigger by Timer. "1": NVM load will be trigger by Timer
NRDSLP	NVM Load Control by Sleep-out	"0": NVM load will not be trigger by sleep Out. "1": NVM load will be trigger by sleep Out.

Default Value (D7 to D0)

1st Parameter=0x17h

2nd parameter=0x00h

8.2.23 OSCSET (D8h): OSC Setting

D8H	OSCSET (OSC Setting)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
OSCEN	0	↑	1	1	1	0	1	1	0	0	0	(D8h)
1st parameter	1	↑	1	OSCEN	0	OSCSW2	0	0	OSCSW1	OSCSW0	0	
2nd parameter	1	↑	1	1	1	1	0	1	0	0	1	

Description

OSCEN (OSC Enable/Disable)

OSCEN	OSC Enable
0	Disable OSC
1	Enable OSC

OSCSW[2:0] (OSC Switch)

OSCSW[2:0]	HPM Frame Rate Max
000	51Hz
111	32Hz

Default Value (D7 to D0)

1st Parameter=0x26h

	2nd parameter=0xE9h

8.2.24 NVMRD (E9h): NVM Data Read

E9H	NVMRD (NVM Data Read)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMRD	0	↑	1	1	1	1	0	1	0	0	1	(E9h)
Parameter	1	↑	1	DO[7]	DO[6]	DO[5]	DO[4]	DO[3]	DO[2]	DO[1]	DO[0]	
Description	-This command is used to read register that load from NVM.											

8.2.25 EXTBCTRL (ECh): EXTB Control

ECH	EXTBCTRL (EXTB Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EXTBCTRL	0	↑	1	1	1	1	0	1	1	0	0	(ECh)
Parameter	1	↑	1	EXTB_CTRL[7:0]								
Description	**EXTB_CTRL[7:0]:** "5Ah": EXTB=H (VDD) "A5h": EXTB=L (VSS)											
Default Value (D7 to D0)	Parameter=0x5Ah											

8.2.26 NVMCTRL1 (F8h): NVM WR/RD Control

F8H	NVMCTRL1 (NVM WR/RD Control)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMCTRL1	0	↑	1	1	1	1	1	1	0	0	0	(F8h)
1st parameter	1	↑	1	0	1	0	1	1	0	1	0	(5Ah)
2nd parameter	1	↑	1	0	1	1	0	1	0	0	1	(69h)
3rd parameter	1	↑	1	1	1	1	0	1	1	1	0	(EEh)
4th parameter	1	↑	1	0	0	0	0	0	PROG	RD	0	
Description	-NVM WR/RD mode select											

Bit	Value
PROG	'1' =Enable Program Mode '0' =Disable Program Mode
RD	'1' = Enable Read Mode '0' = Disable Read Mode

Default Value (D7 to D0)	1st Parameter=0x5Ah 2nd parameter=0x69h 3rd parameter=0xEEh 4th parameter=0x00h

8.2.27 NVMCTRL2 (FAh): NVM Program Setting

FAH	NVMCTRL2 (NVM Program Setting)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMCTRL2	0	↑	1	1	1	1	1	1	0	1	0	(FAh)
1st parameter	1	↑	1	0	0	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]	
2nd parameter	1	↑	1	PIN[7]	PIN[6]	PIN[5]	PIN[4]	PIN[3]	PIN[2]	PIN[1]	PIN[0]	
Description	-NVM program register address and data setting.											
Default Value (D7 to D0)	1st Parameter=0x00h 2nd parameter=0x00h											

8.2.28 NVMRDEN (FBh): NVM Read Enable

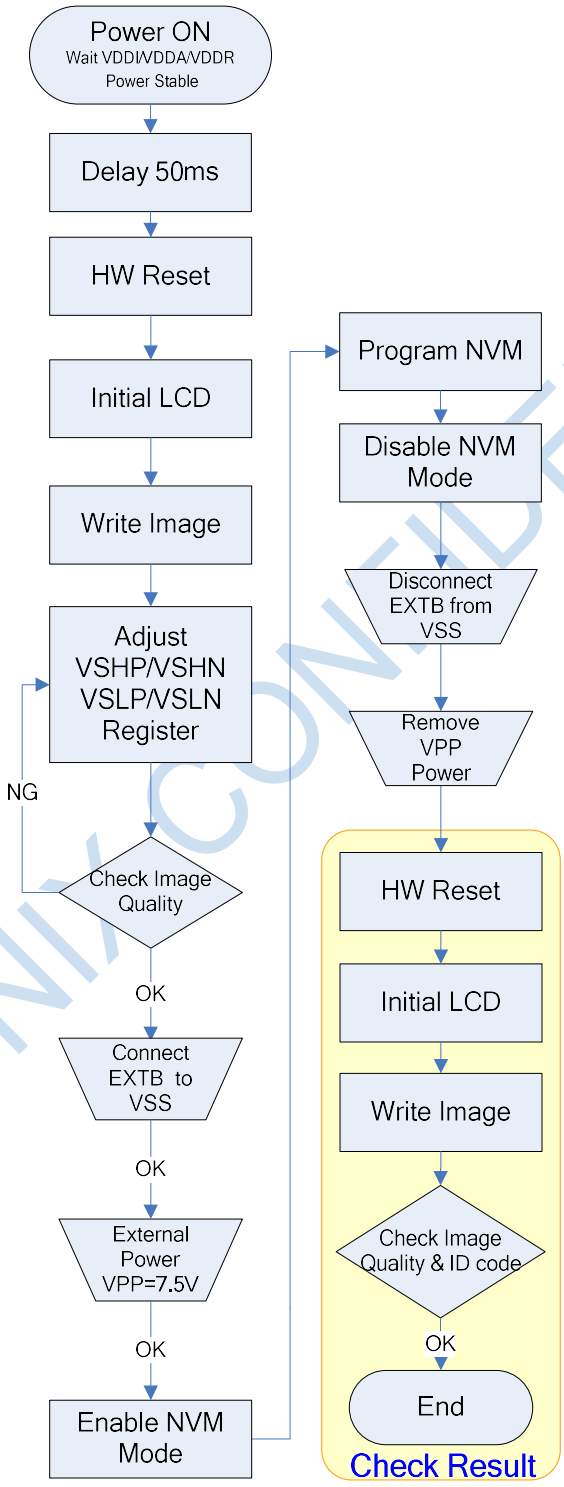
FBH	NVMRDEN (NVM Read Enable)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMRDEN	0	↑	1	1	1	1	1	1	0	1	1	(FBh)
1st parameter	1	↑	1	0	1	0	0	1	0	1	0	(4Ah)
2nd parameter	1	↑	1	1	0	1	0	0	1	0	1	(A5h)
Description	-Enable NVM read mode.											

8.2.29 NVMPROM (FCh): NVM Program Enable

FCH	NVMPROM (NVM Program Enable)											
Inst / Para	A0	RWR	ERD	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMPROM	0	↑	1	1	1	1	1	1	1	0	0	(FCh)
1st parameter	1	↑	1	0	0	1	0	1	0	0	1	(29h)
2nd parameter	1	↑	1	1	0	1	0	0	1	0	1	(A5h)
Description	-Enable NVM program mode.											

9 NVM PROGRAMMING FLOW

NVM Programming Flow



10 ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
I/O Power Supply Voltage	VDDI	- 0.3 ~ +4.0	V
Analog Power Supply Voltage	VDDA	- 0.3 ~ +4.0	V
Reference Power Supply Voltage	VDDR	- 0.3 ~ +4.0	V
LCD Driver Supply Voltage	AVDD	- 0.3 ~ +6.6	V
	VSH-VSL	-0.3 ~ +6.2	V
	VGH-VGL	-0.3 ~ +33.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Table 2 Maximum Ratings

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

11 DC CHARACTERISTICS

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
Analog Power Supply (Normal Mode)	VDDA\VDDR	Analog Power	2.55		3.6	V	
Digital Power Supply (Normal Mode)	VDDI	I/O Supply Voltage	1.65		3.6	V	
Power Supply (1.8V Mode)	VDDA\VDDR VDDI	Single Power	1.7	1.8	1.9	V	
Gate Driver High Voltage	VGH		8.0		17.0	V	Note 1
Gate Driver Low Voltage	VGL		-15.0		-5.0	V	
Gate Driver Supply Voltage		| VGH-VGL |	13.0		32.0	V	Note 2
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	
VCOM Voltage							
VCOM amplitude	VCOM			VSS		V	
Source Driver							
Source High Voltage (Positive)	VSHP		3.7		6.2	V	
Source Low Voltage (Positive)	VSLP		0		2.0	V	
Source High Voltage (Negative)	VSHN		-5.3		-2.5	V	
Source Low Voltage (Negative)	VSLN		-1.8		1.0	V	

Table 3 Basic DC Characteristics

Notes:

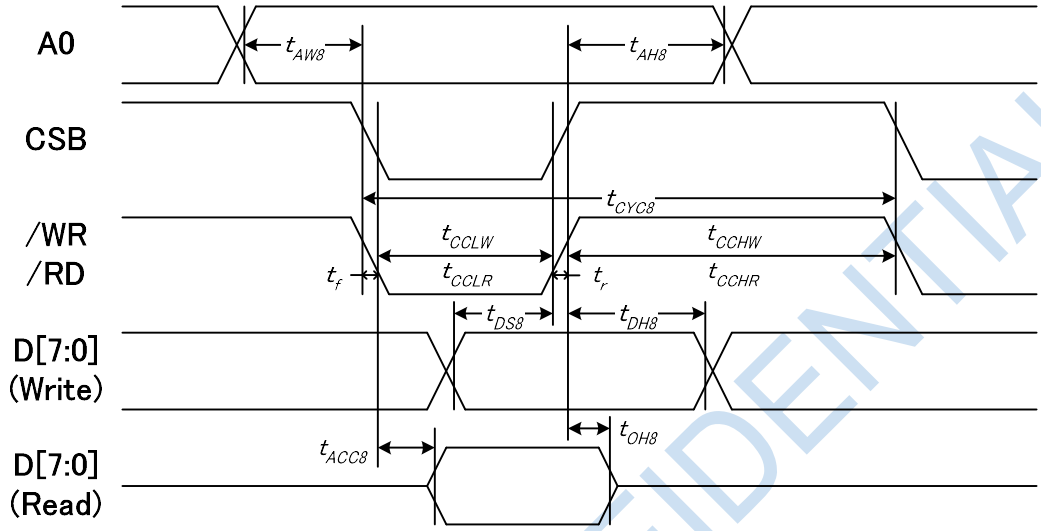
1. When evaluating the maximum and minimum of VGH, VDD=2.8V.

2. The maximum value of |VGH-VGL| can not over 32.0V.

12 AC CHARACTERISTICS

12.1 Interface Timing

12.1.1 System Bus Timing for Parallel 8080 MCU Interface



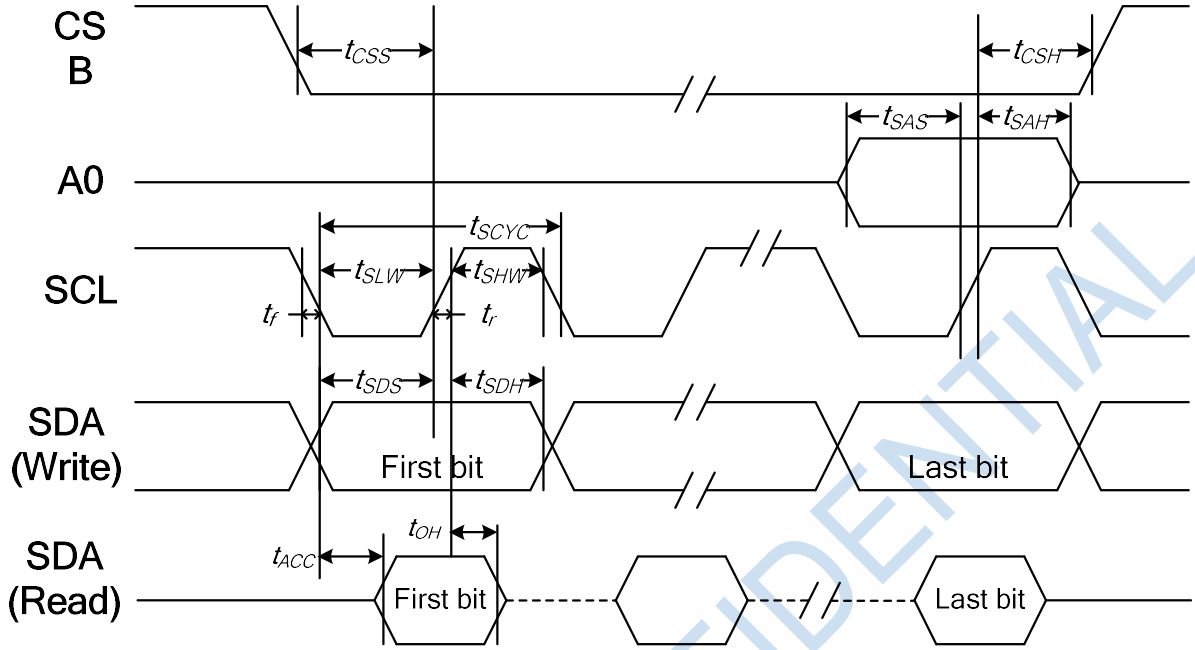
VDDI = 1.8~3.3V, Ta = 25˚C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		20	—	ns
Address hold time		tAH8		0	—	
System cycle time (WRITE)	/WR	tCYC8		160	—	
/WR L pulse width (WRITE)		tCCLW		70	—	
/WR H pulse width (WRITE)		tCCHW		70	—	
System cycle time (READ)	RD	tCYC8		400	—	
/RD L pulse width (READ)		tCCLR		180		
/RD H pulse width (READ)		tCCHR		180		
WRITE Data setup time	D[7:0]	tDS8		15	—	
WRITE Data hold time		tDH8		15	—	
READ access time		tACC8	CL = 30 pF	—	100	
READ Output disable time		tOH8	CL = 30 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDDI as the reference.

12.1.2 System Bus Timing for 4SPI MCU Interface



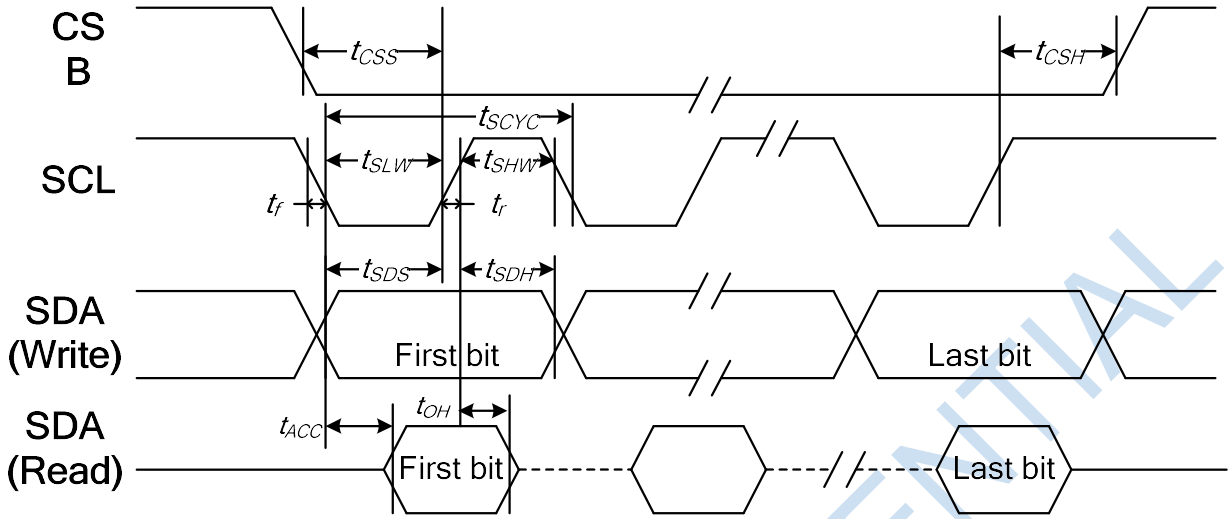
VDDI = 1.8~3.3V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period (Write)	SCL	tSCYC		30	—	ns
Serial clock period (Read)				150		
SCLK “H” pulse width (Write)		tSHW		15	—	
SCLK “H” pulse width (Read)				60		
SCLK “L” pulse width (Write)		tSLW		15	—	
SCLK “L” pulse width (Read)				60		
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		10	—	
Data setup time	SDA (Write)	tSDS		10	—	
Data hold time		tSDH		10	—	
Read data access time	SDA (Read)	tACC	For maximum CL=30p	10	50	
Read data output disable time		tOH	For minimum CL=8p	15	50	
CSB-SCLK time	CSB	tCSS		10	—	
CSB-SCLK time		tCSH		10	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

12.1.3 System Bus Timing for 3SPI MCU Interface



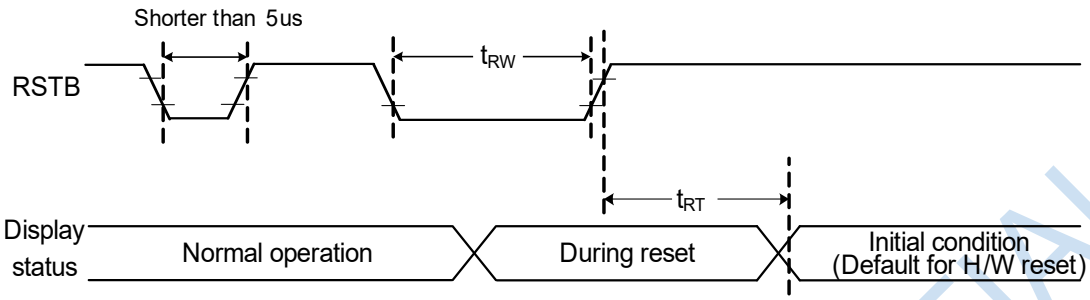
VDDI = 1.8~3.3V, Ta = 25˚C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period (Write)	SCL	tSCYC		30	—	ns
Serial clock period (Read)				150		
SCLK “H” pulse width (Write)		tSHW		15	—	
SCLK “H” pulse width (Read)				60		
SCLK “L” pulse width (Write)		tSLW		15	—	
SCLK “L” pulse width (Read)				60		
Data setup time	SDA (Write)	tSDS		10	—	
Data hold time		tSDH		10	—	
Data setup time	SDA (Read)	tACC	For maximum CL=30p	10	50	
Data hold time		tOH	For minimum CL=8p	15	50	
CSB-SCLK time	CSB	tCSS		10	—	
CSB-SCLK time		tCSH		10	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

12.1.4 Reset Timing



VDDI = 1.8~3.3V, Ta = 25°C

Item	Symbol	Condition	Min.	Max.	Unit
Reset "L" pulse width	tRW		1	—	ms
Reset cancel	tRT	Note1, 5 (sleep-in mode)	—	5	ms
		Note1, 6, 7 (sleep-out mode)	—	120	ms

Notes:

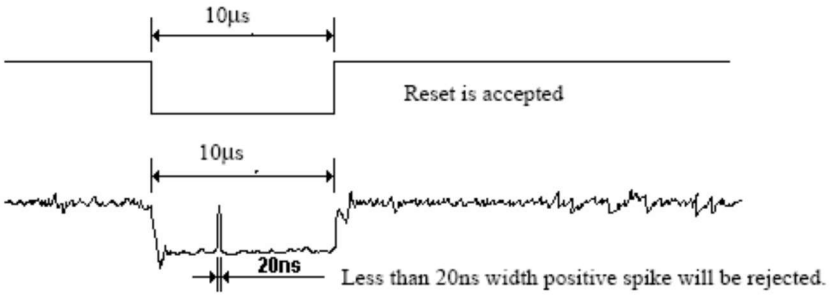
1. The reset cancel includes also required time for loading ID bytes, VSource setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RSTB.

2. Spike due to an electrostatic discharge on RSTB line does not cause irregular system reset according to the table below:

RSTB Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

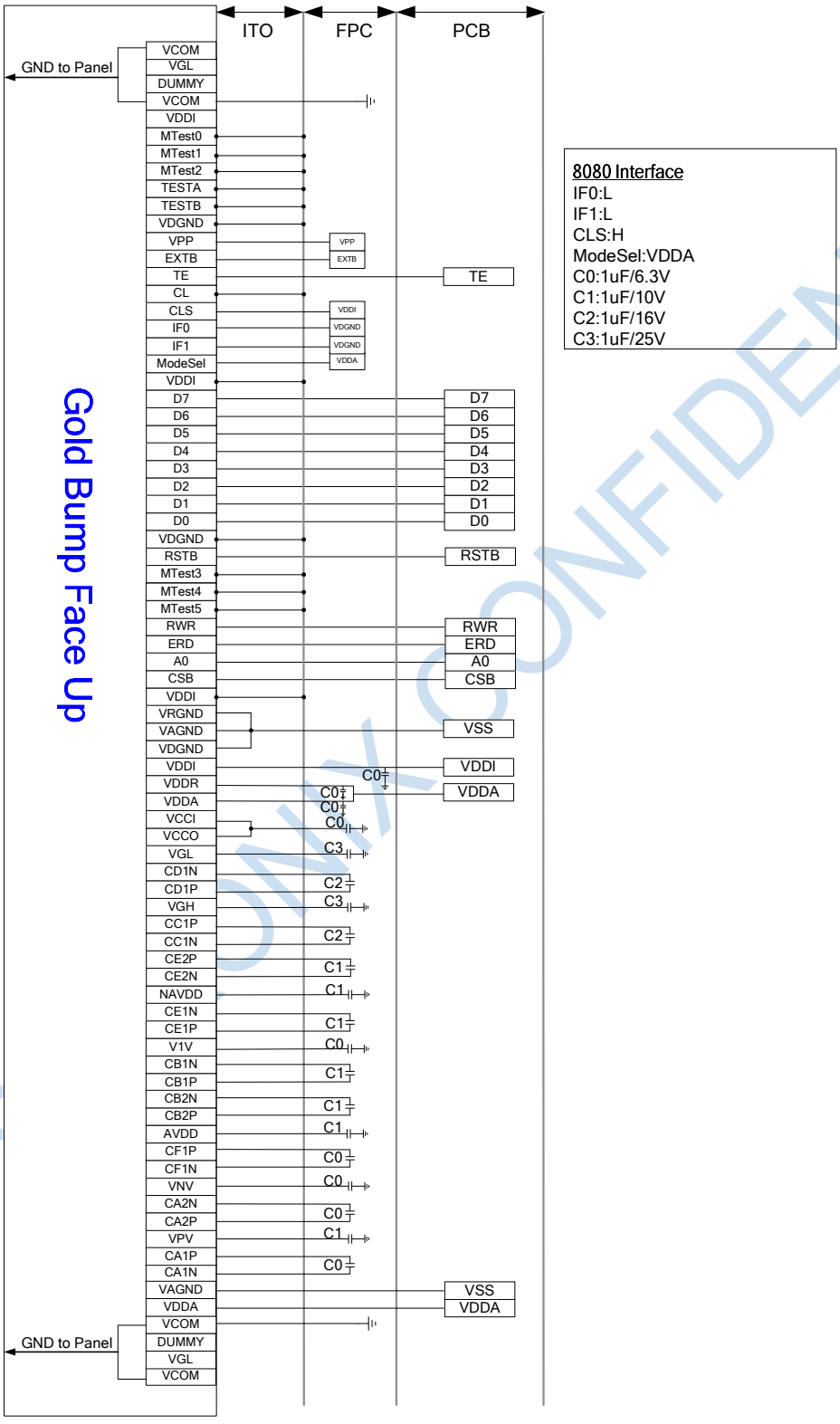
6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RSTB before sending commands. Also Sleep Out command cannot be sent for 120msec.

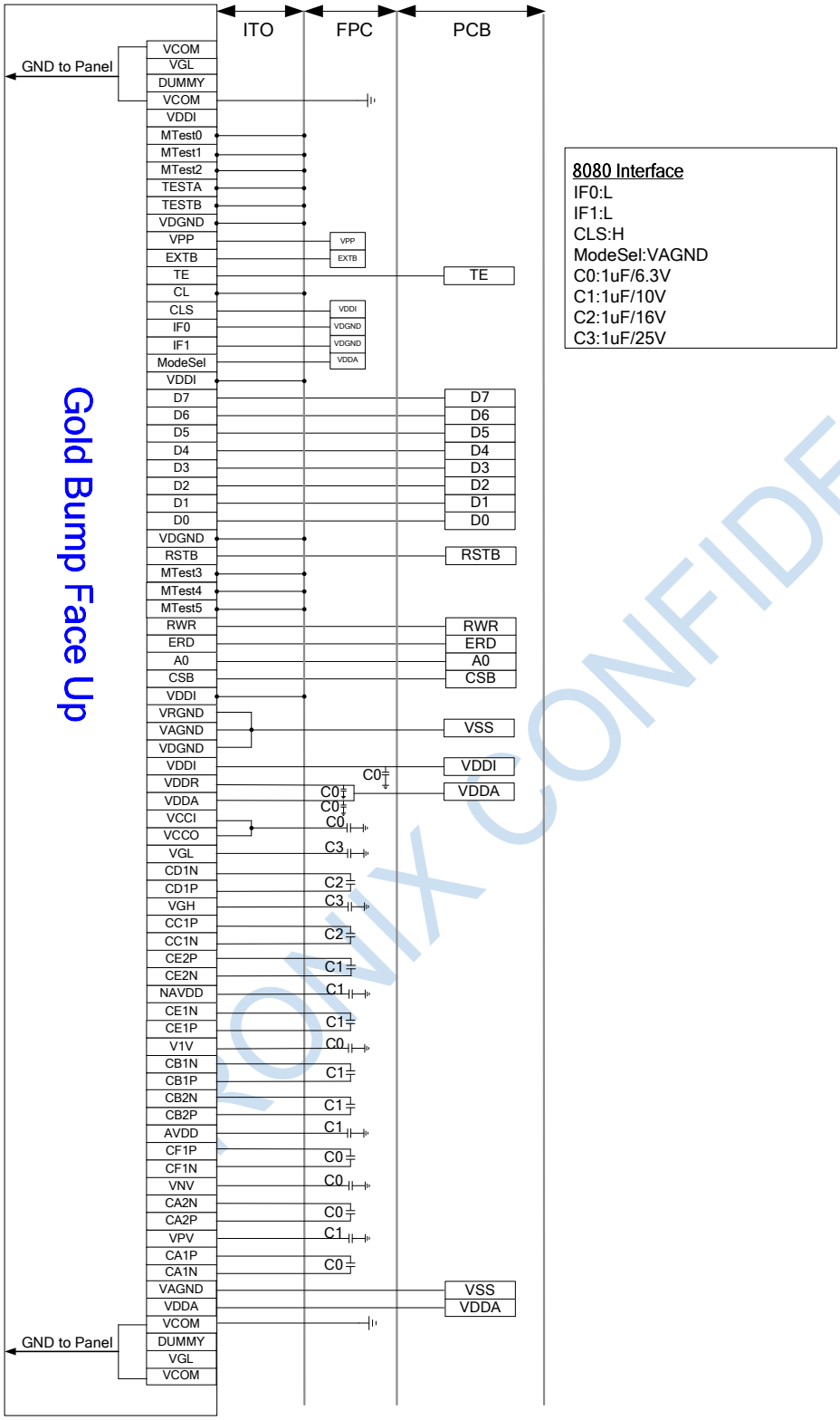
13 APPLICATION NOTE

13.1 Parallel 8080 Interface

13.1.1 VDDA=3.3V

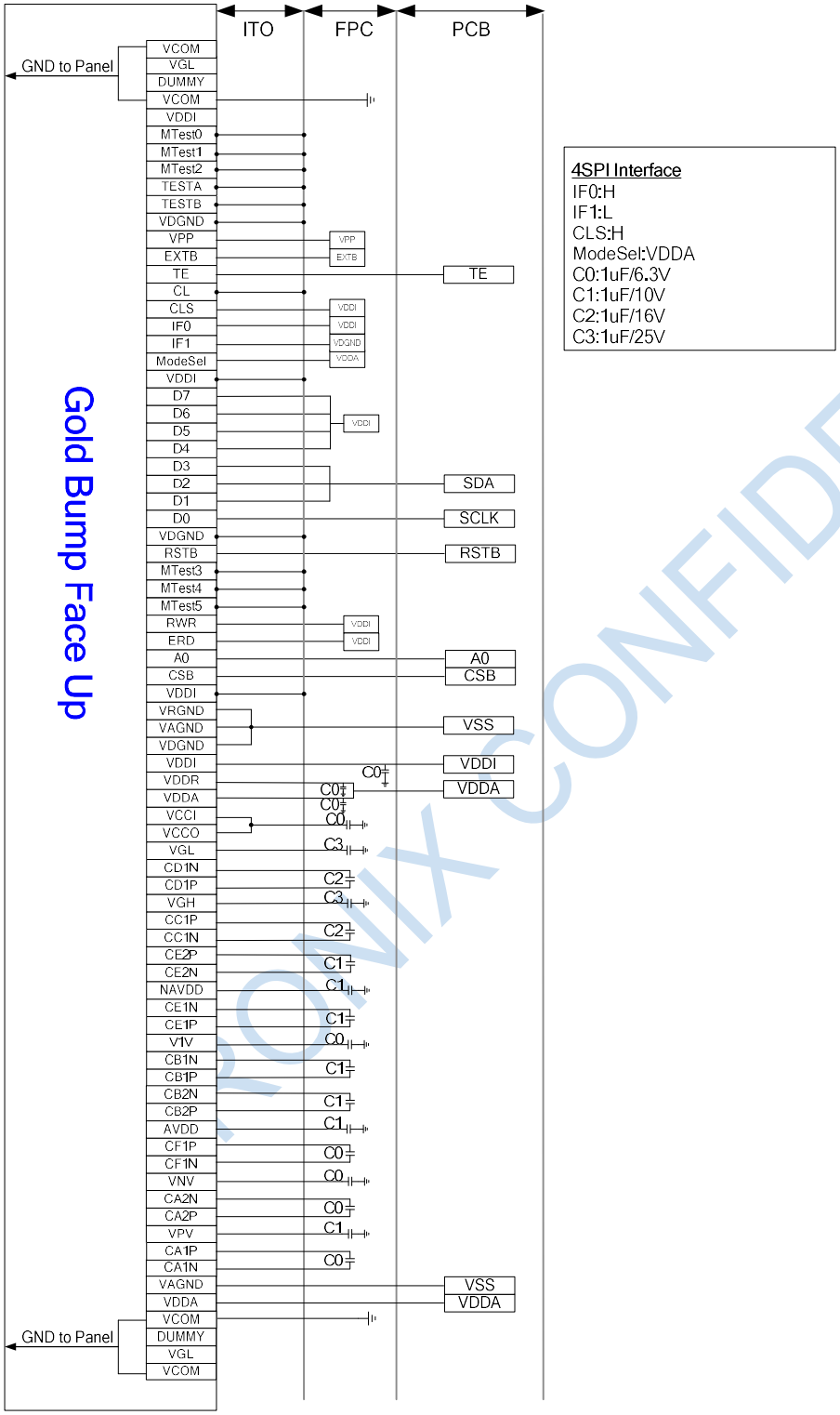


13.1.2 VDDI=VDDA=1.8V

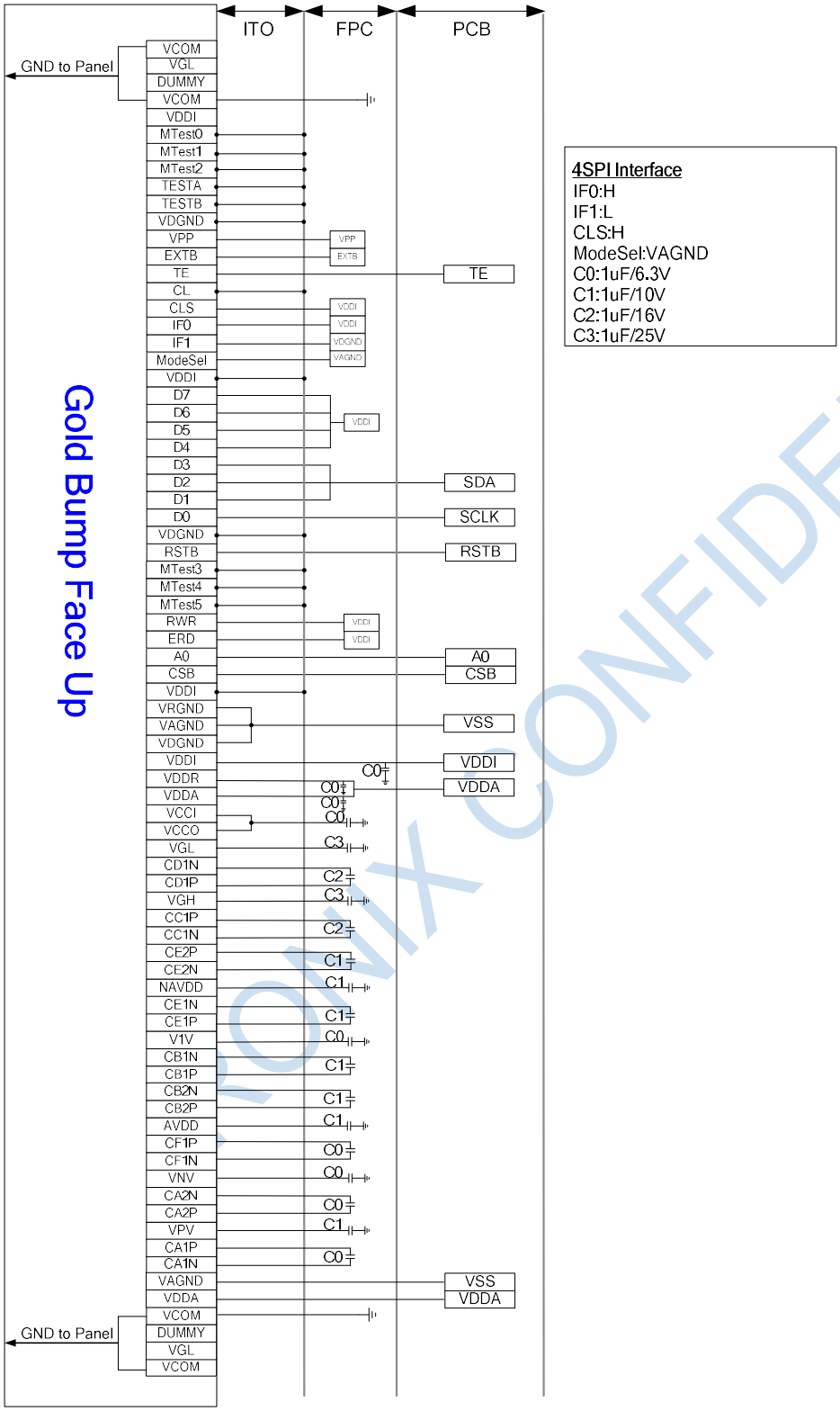


13.2 Single 4-line SPI Interface

13.2.1 VDDA=3.3V

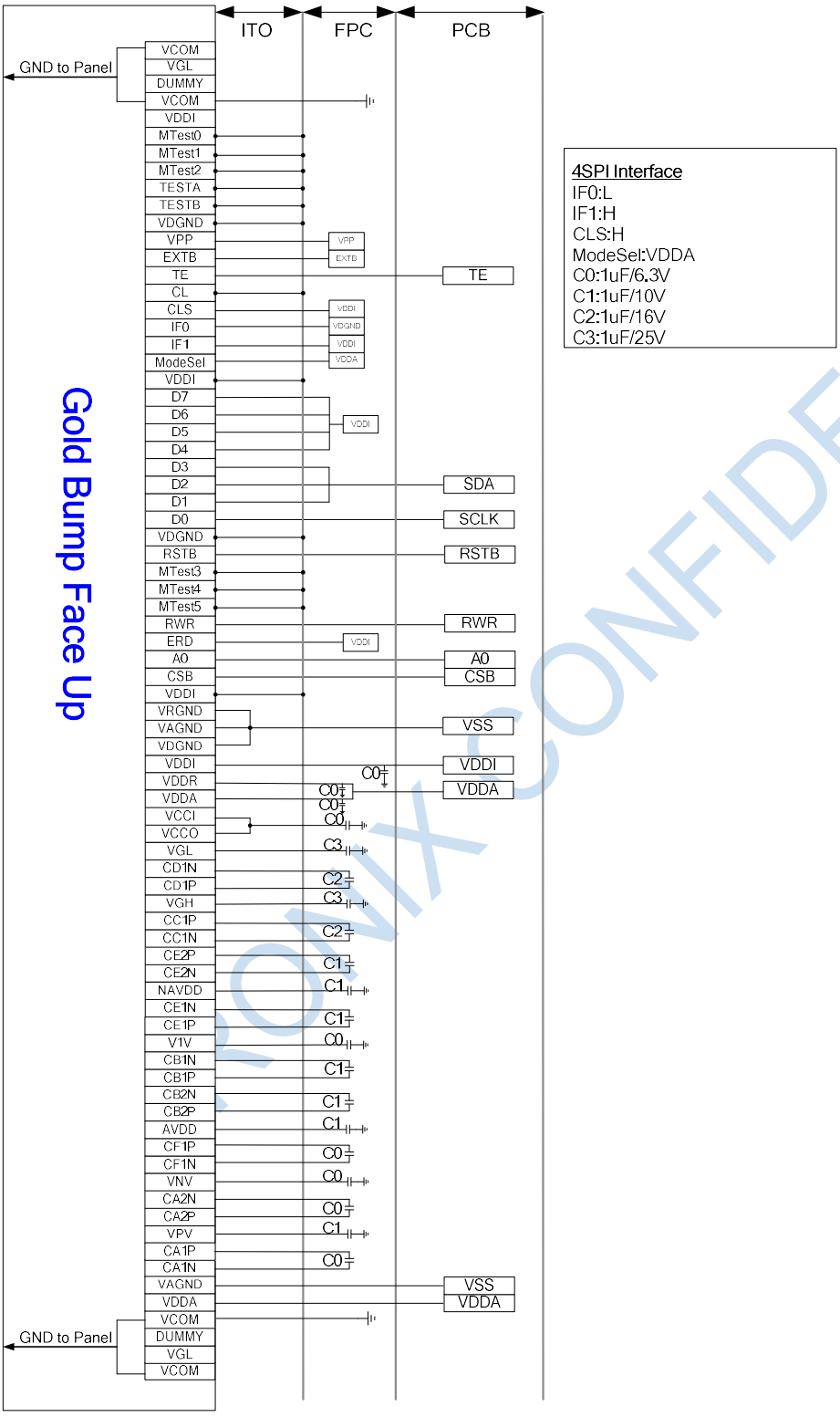


13.2.2 VDDI=VDDA=1.8V

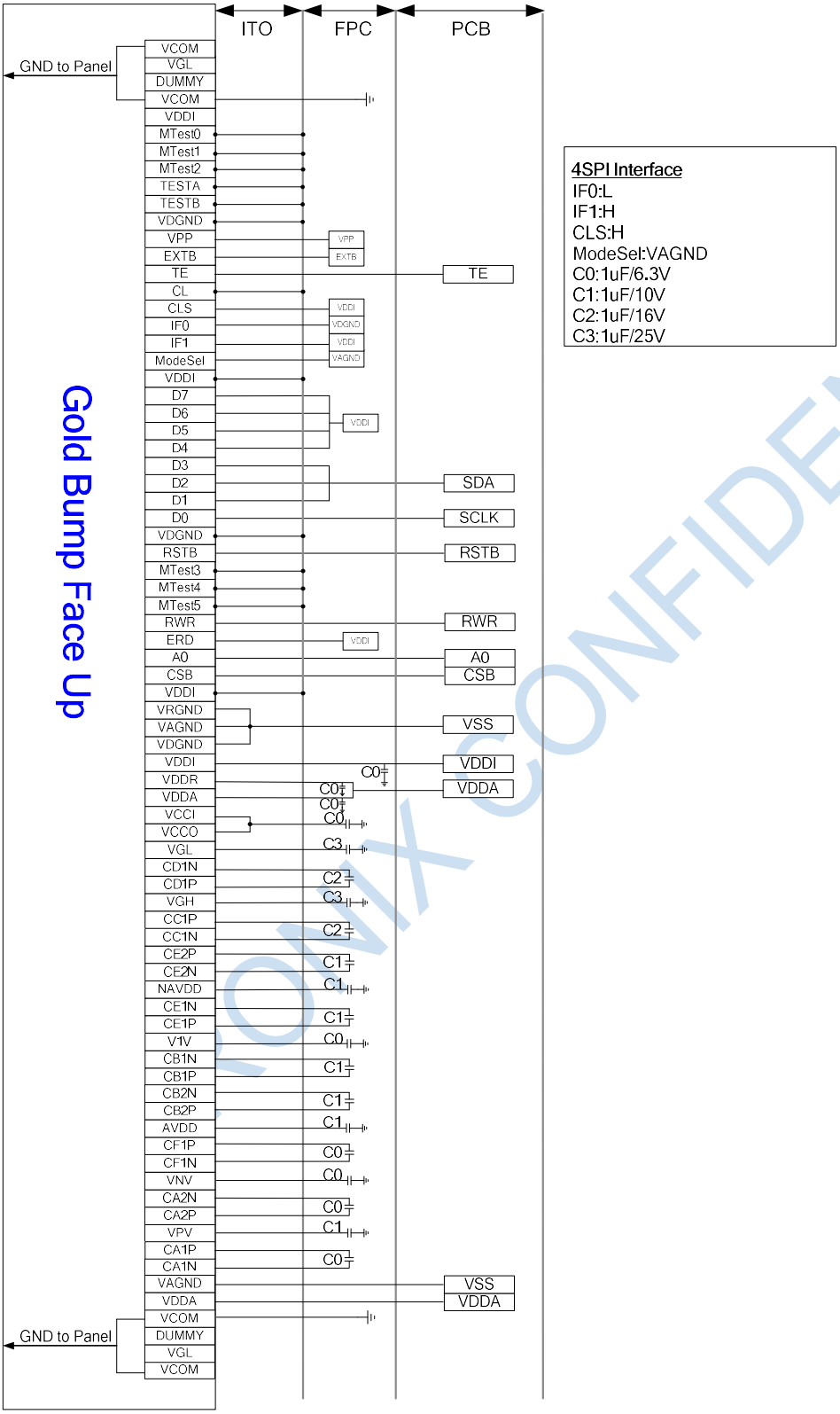


13.3 Dual 4-line SPI Interface

13.3.1 VDDA=3.3V

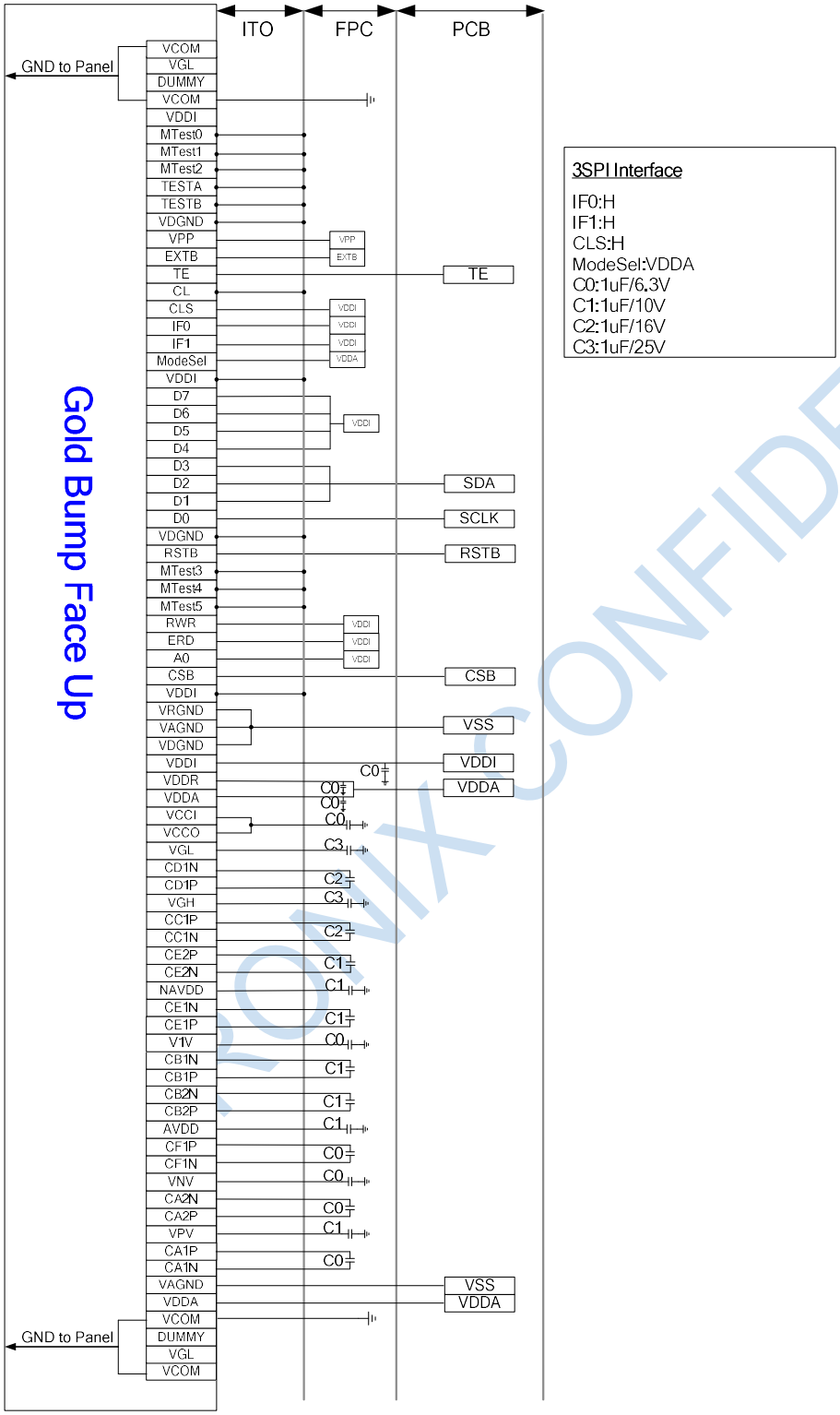


13.3.2 VDDI=VDDA=1.8V

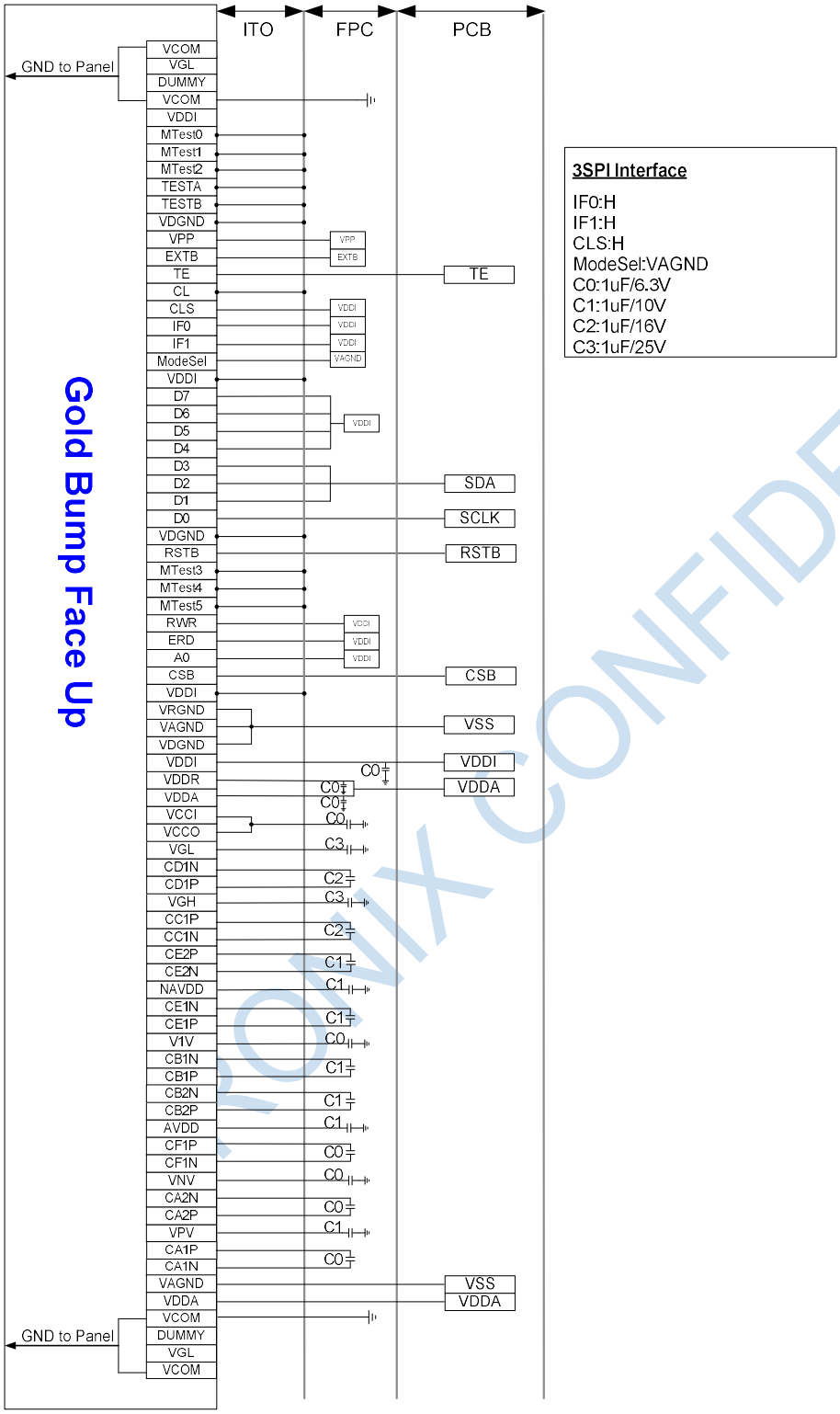


13.4 3-line SPI Interface

13.4.1 VDDA=3.3V



13.4.2 VDDI=VDDA=1.8V



14 REVISION HISTORY

Version	Date	Description
V0.1	2021/03	● Preliminary.
V0.2	2021/04	● Modify Source PAD Arrangement